

PA1

PA2

PA3

PA4

PA5

PA6

PA7

1

2

3

4

5

6

7

Header 7

PULS1

PULS2

Tr\_DO

Tr\_AO

ADC\_KEY

PWM1

PWM2

1

2

3

4

5

6

7

Header 7

PA4

PA5

PA6

PA7

1

2

3

5

7

MEMS\_SCL

MEMS\_SDA

MEMS\_INT1

MEMS\_INT2

2

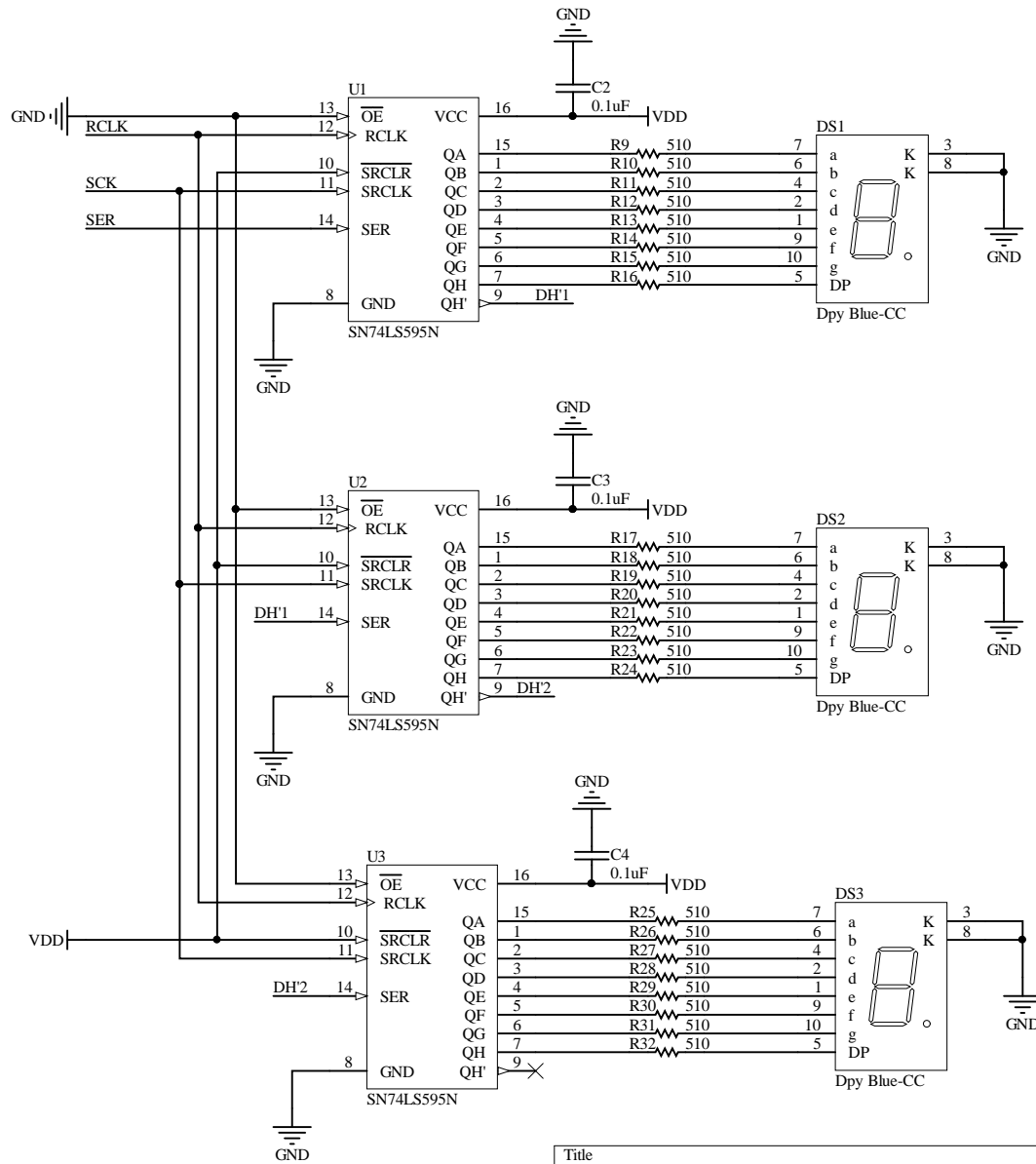
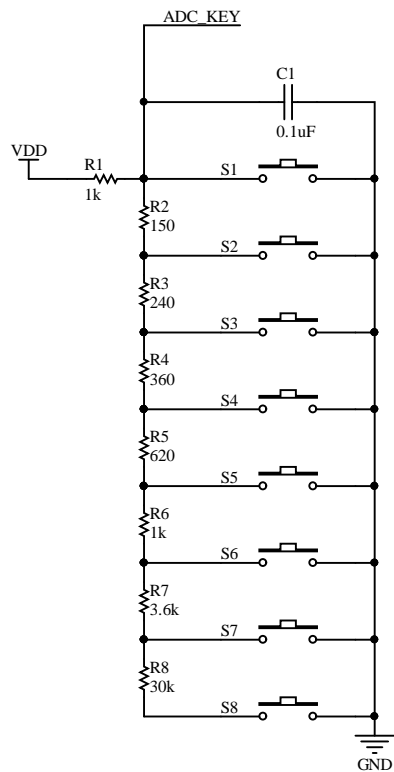
4

6

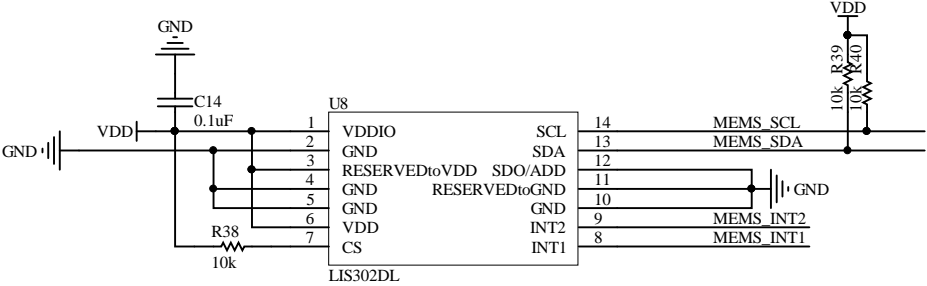
8

Header 4X2

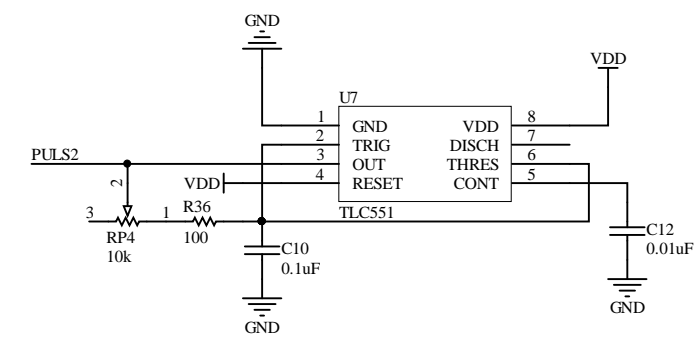
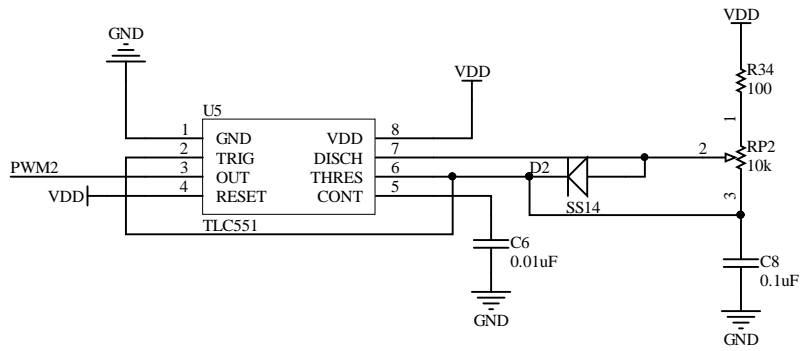
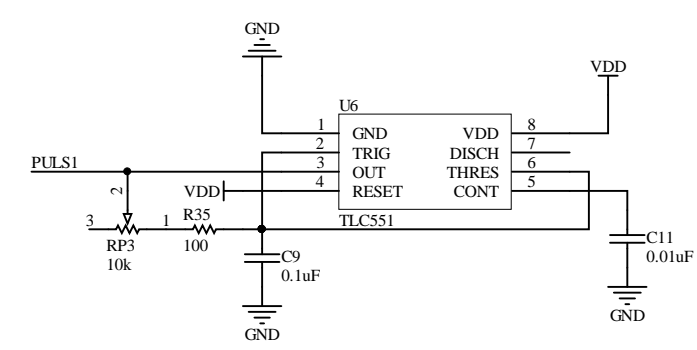
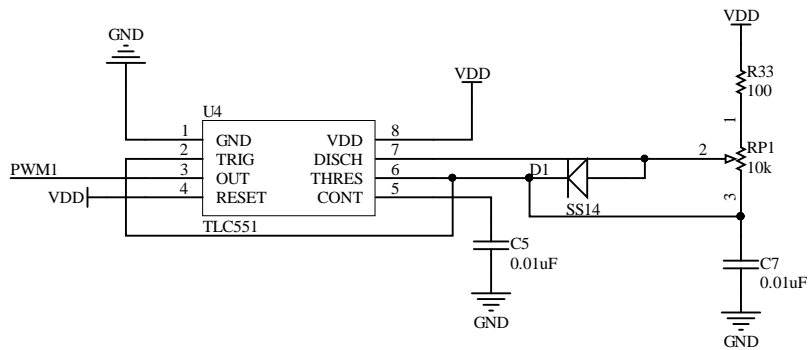
Title		
Size	Number	Revision
A4		
Date:	2021/5/25	Sheet of
File:	E:\PCB-ALL\...\CNTR.SchDoc	Drawn By:



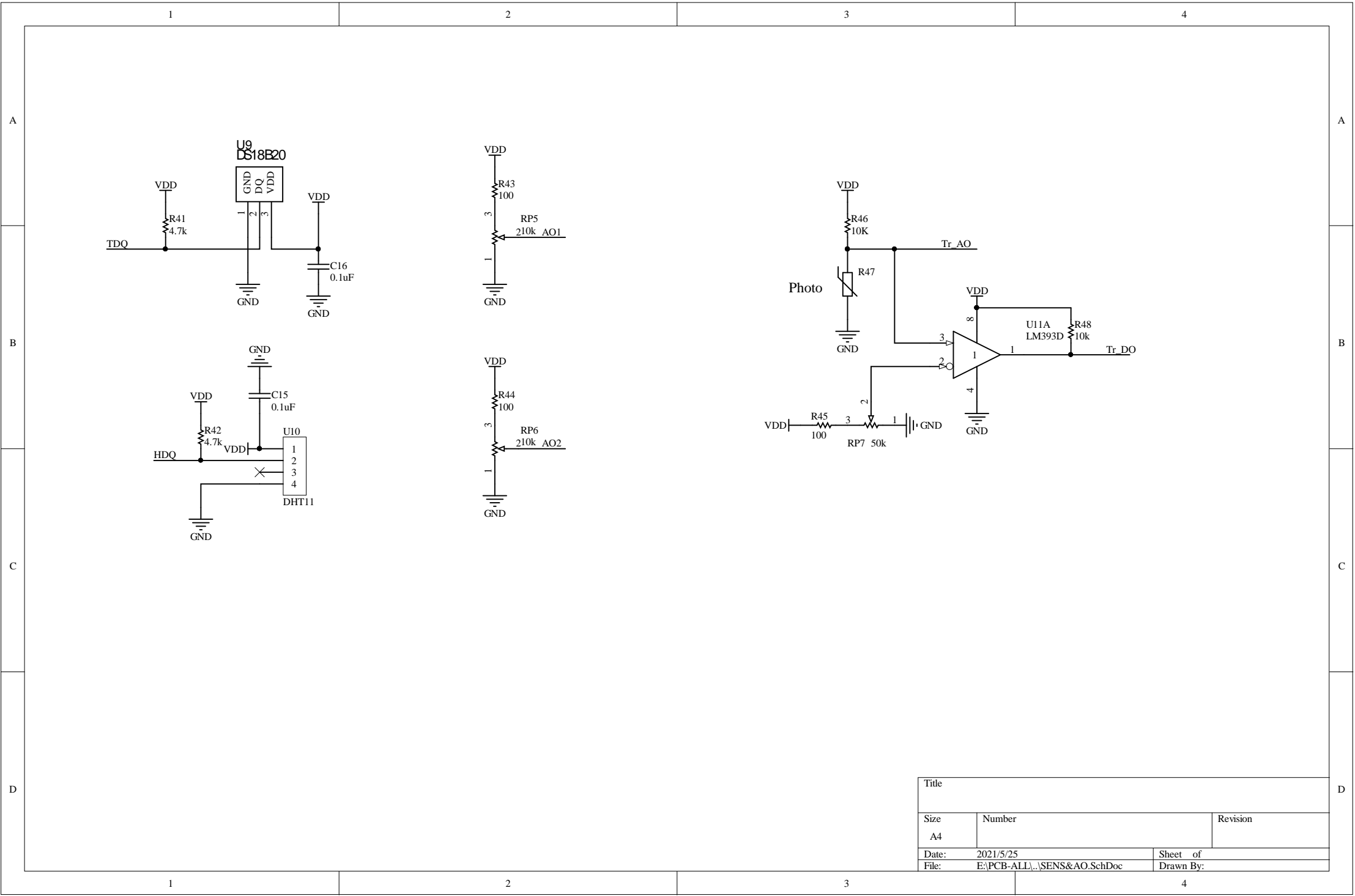
Title		
Size	Number	Revision
A4		
Date:	2021/5/25	Sheet of
File:	E:\PCB-ALL\..\DSPY&KEY.SchDoc	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	2021/5/25	Sheet of
File:	E:\PCB-ALL\...\I2C.SchDoc	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	2021/5/25	Sheet of
File:	E:\PCB-ALL\...\PLUS.SchDoc	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	2021/5/25	Sheet of
File:	E:\PCB-ALL\..\SENS&AO.SchDoc	Drawn By: