ti23_assignment_06_Alabrsh_Panov_Zeitler

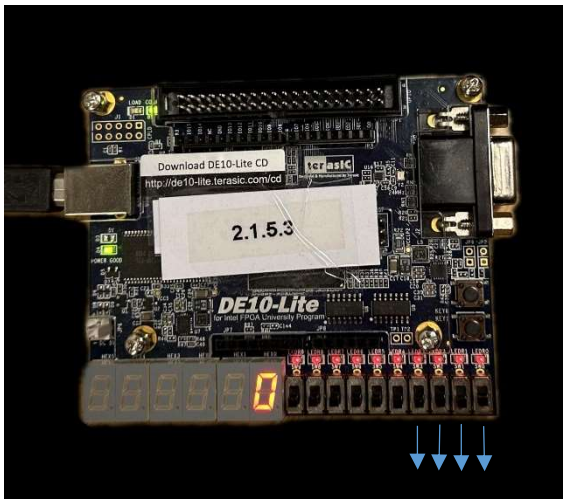
1a) completed truth table of the 7-segment display decoder:

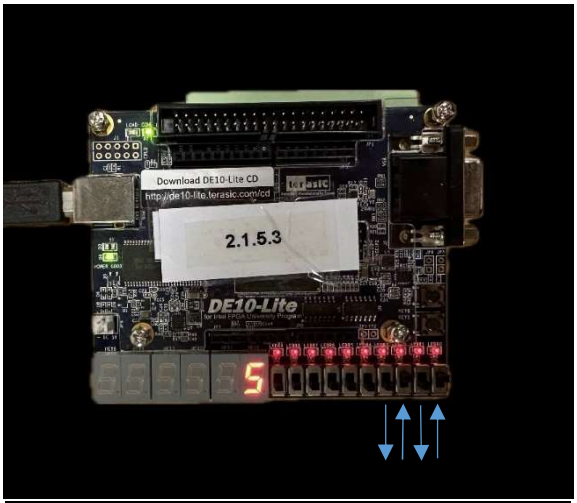
hex number	binary number	binary encoding
0	4'b0000	7'b100_0000
1	4'b0001	7'b111_1001
2	4'b0010	7'b010_0100
3	4'b0011	7'b011_0000
4	4'b0100	7'b001_1001
5	4'b0101	7'b100_0010
6	4'b0110	7'b000_0010
7	4'b0111	7'b111_1000
8	4'b1000	7'b000_0000
9	4'b1001	7'b001_0000
A	4'b1010	7'b000_1000
B	4'b1011	7'b000_0011
C	4'b1100	7'b100_0110
D	4'b1101	7'b010_0001
E	4'b1110	7'b000_0110
F	4'b1111	7'b000_1110

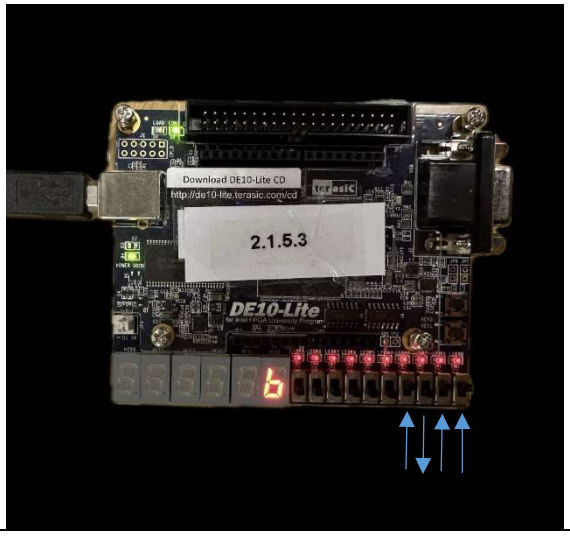
1b) Implemented module decoder → siehe src (decoder.sv)

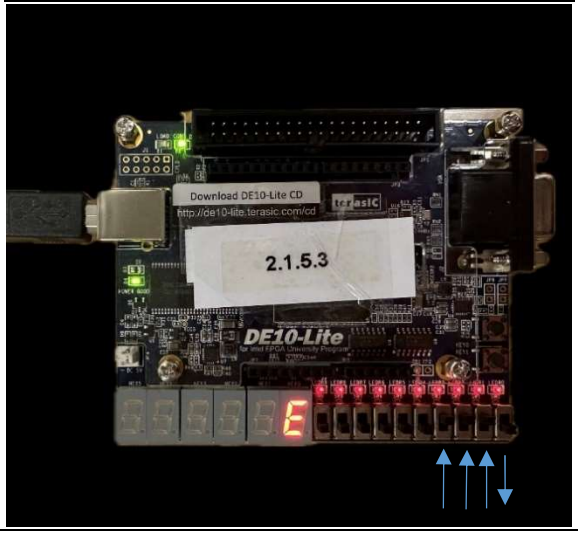
1c) Finished implementation of the module decoder_de10_lite → siehe src (decoder_de10_lite.sv)

1d) Compiled modules in Quartus Prime and programmed the FPGA of a DE10-Lite board.
Verified that the board shows the correct hexadecimal numbers in the display for all
combinations of the switches. Provided evidence for the following hex-numbers 0, 5, B, and E in pictures:







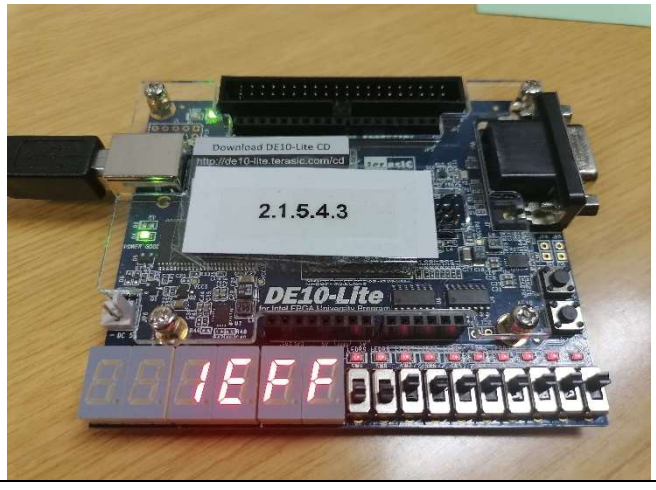


2a) Implemented module that uses 4-Bit ripple carry adder to compute C[4:0] = B[3:0] + A[3:0]
→ siehe src (tiny_calculator.sv)

2b) -Testbench for tiny calculator to check the right outputs for Table2 → siehe src (tiny_calculator_tb.sv)
-Completed Table2:

SW[7:4]	SW[3:0]	HEX3[6:0]	HEX2[6:0]	HEX1[6:0]	HEX0[6:0]
0000	0001	100_0000	111_1001	100_000	111_1001
0010	0110	100_0000	000_0000	010_0100	000_0010
0111	0101	100_0000	100_0110	111_1000	001_0010
1000	1000	111_1001	100_0000	000_0000	000_0000
11111	1111	111_1001	000_0110	000_1110	000_1110

2c) Compiled modules in Quartus Prime and programmed the FPGA of a DE10-Lite board.
Verified that the board shows the correct hexadecimal numbers for the configurations in Table2 (2b).
Provided evidence for each of the five configurations:



Aufgabenbearbeitung:

Aufgabe 1 → Rahaf, Christian, Cora
Aufgabe 2 → Rahaf, Christian, Cora