

## ti23 assignment 09 Alabrsh Panov Zeitler

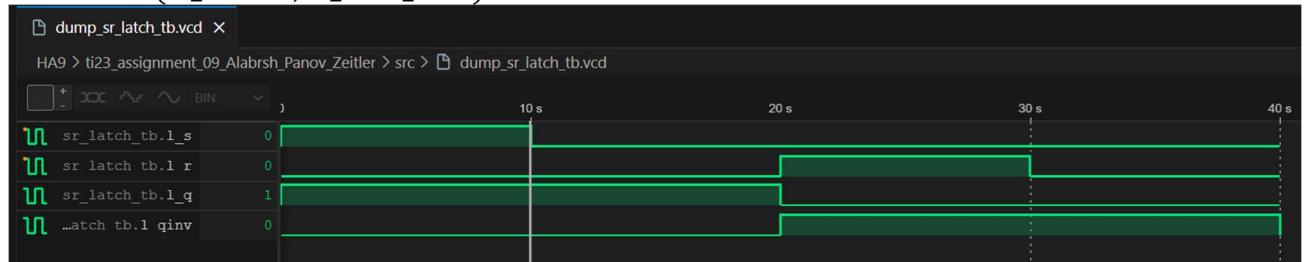
1a) Implemented modules decoder 2:4 and mux with respective testbenches:

→siehe src (mux\_4.sv, mux\_4\_tb.sv)

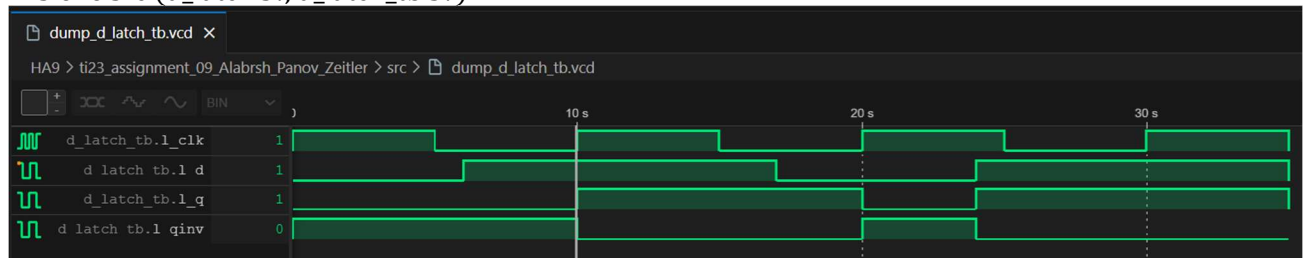
→siehe src (decoder\_2\_4.sv, decoder\_2\_4\_tb.sv)

1b) Implemented register-related modules with respective testbenches and showing waveform:

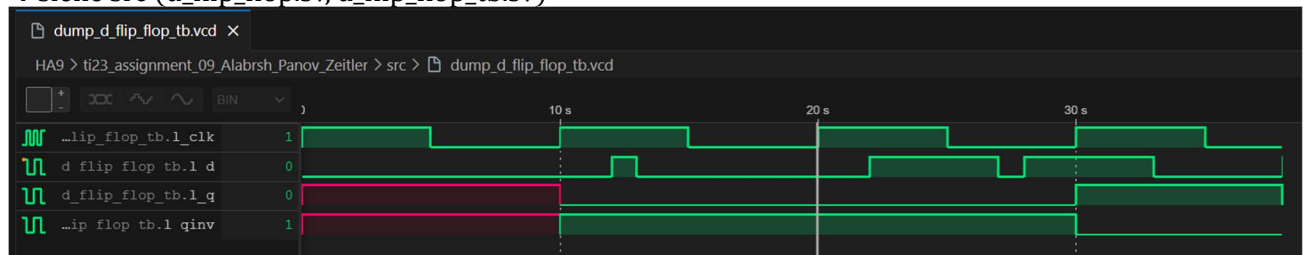
→siehe src (sr\_latch.sv, sr\_latch\_tb.sv)



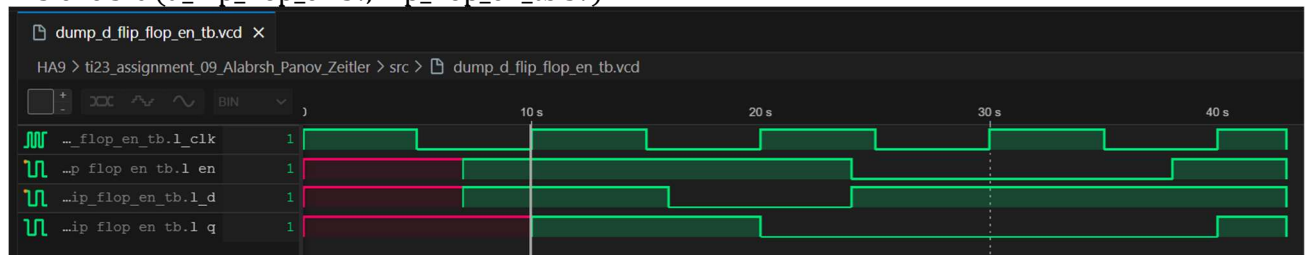
→siehe src (d\_latch.sv, d\_latch\_tb.sv)



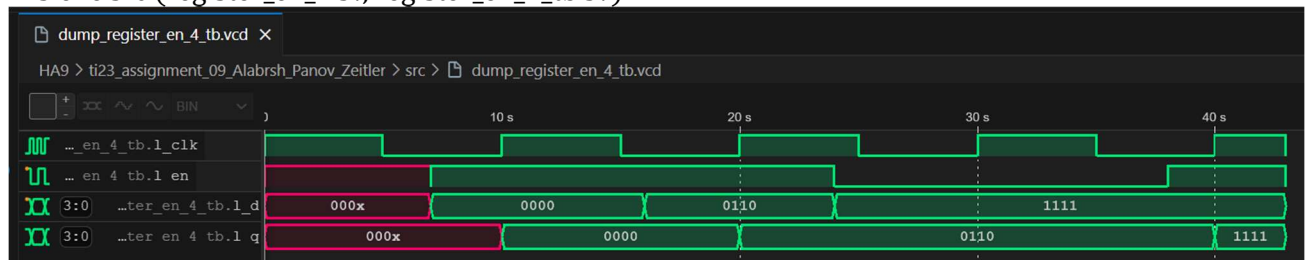
→siehe src (d\_flip\_flop.sv, d\_flip\_flop\_tb.sv)



→siehe src (d\_flip\_flop\_en.sv, flip\_flop\_en\_tb.sv)

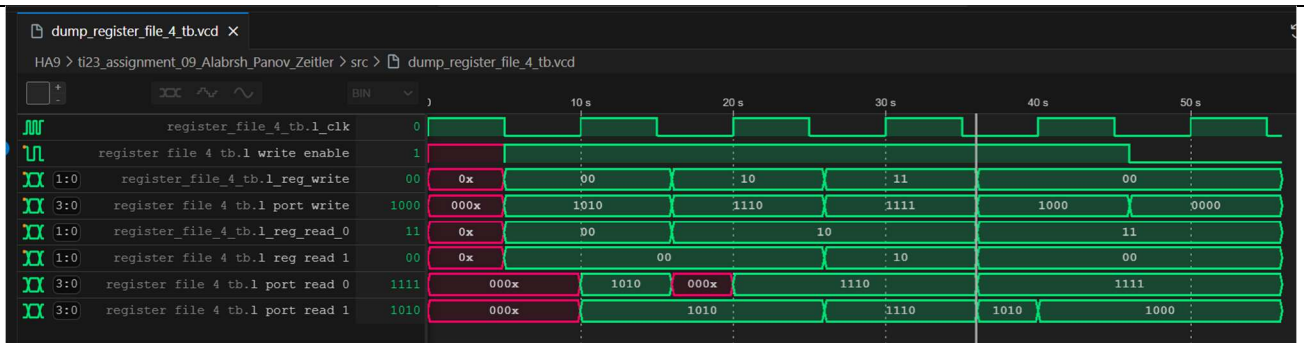


→siehe src (register\_en\_4.sv, register\_en\_4\_tb.sv)



1c) Implemented module register\_file with corresponding testbench and provided the internal register values in the comments of the tb code (floating values, if register was never written) + waveform

→siehe src (register\_file\_4.sv, register\_file\_4\_tb.sv)



1d) Finished top level module register\_file\_de10\_lite with testbench and waveform  
 → siehe src (register\_file\_de10\_lite.sv, register\_file\_de10\_lite\_tb.sv)

1e) Explained and illustrated programmed FPGA to teaching personal. Included Scan of tailored coversheet:

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Jena, den 18.12.23

Serie # 9

bearbeitet, eingereicht und vorgeführt von

Nachname	Vorname	Matrikelnummer	Anwesend
Alabrsh	Rahaf	205604	X
Panov	Christian	174038	✓
Zeitler	Cora	199225	✓

Code:

1.0.

Demonstration:

1.0.

Kommentar:

Unterschrift der Lehrperson:

### Aufgabenbearbeitung:

Aufgabe 1a,b,c,d → Christan, Cora, Rahaf / Aufgabe 1e → Christan, Cora