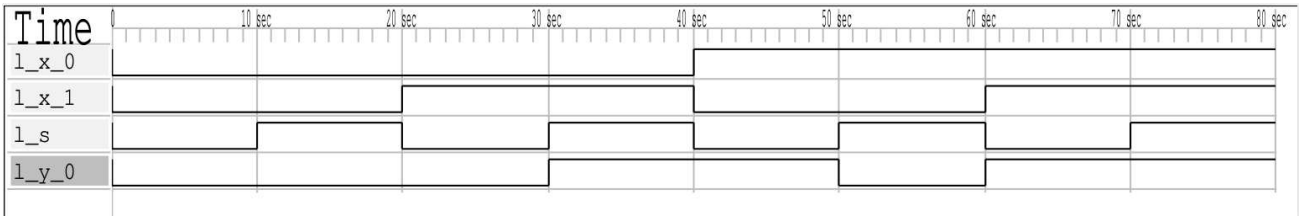
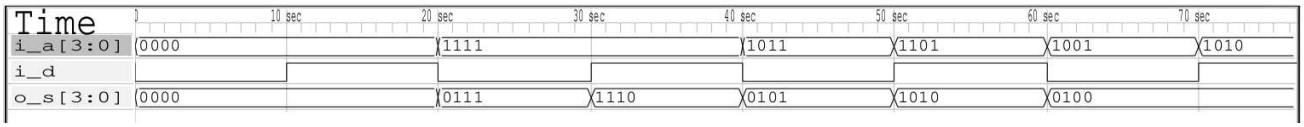
ti23_assignment_05_Alabrsh_Panov_Zeitler

1a)	Implemented 2:1MUX in the module mux21 (circuits pecified by the equation y0 =(¬S∧x0)∨(S∧x1), where S is the selector bit and (x1,x0) is the input data. → siehe src (mux21.sv)
1b)	Test implementation to verify that your module produces the correct outputs for all possible inputs → siehe src (mux21_tb.sv)
1c)	Visualize the waveforms generated by the module as vectorgraphic 
2a) / 2b)	Designed four-bit shifter using 2:1MUX gates and implemented circuit in digital → siehe src (2a_4bit_shifter.dig)
2c)	Completed table | a | d | s | |---|---|---| | 0b0000 | 0b0 | 0b0000 | | 0b0000 | 0b1 | 0b0000 | | 0b1111 | 0b0 | 0b0111 | | 0b1111 | 0b1 | 0b1110 | | 0b1011 | 0b0 | 0b0101 | | 0b1101 | 0b1 | 0b1010 | | 0b1001 | 0b0 | 0b0100 | | 0b1010 | 0b1 | 0b0100 |
2d)	Implemented module → siehe src(shifter_4.sv)
2e)	Visualized waveform (Only show the four-bit inputs i_a, the shift direction d_in, and the four-bit output o_s in that order) 
2f)	Implemented testbench to check the outputs for all inputs in Table (2c) through assert()-statements → siehe src (shifter_4_tb.sv)

Aufgabenbearbeitung:

Aufgabe 1 → Rahaf, Christian, Cora
Aufgabe 2 → Rahaf, Christian, Cora
Aufgabe 3 → Rahaf, Christian, Cora