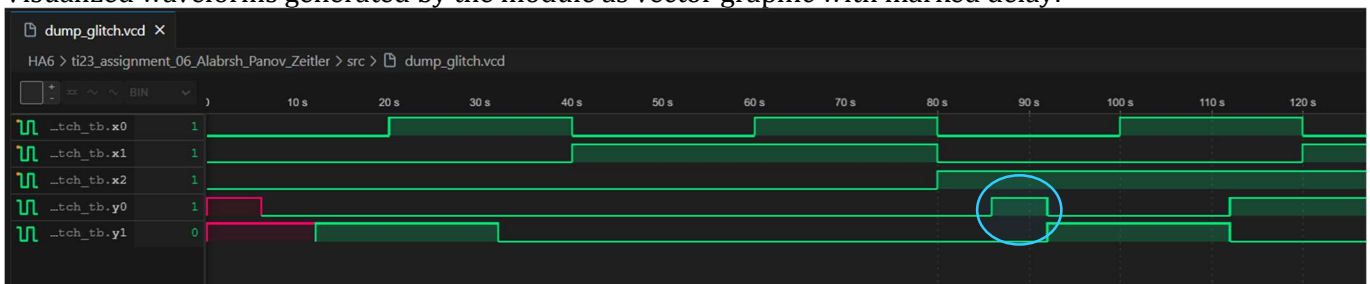
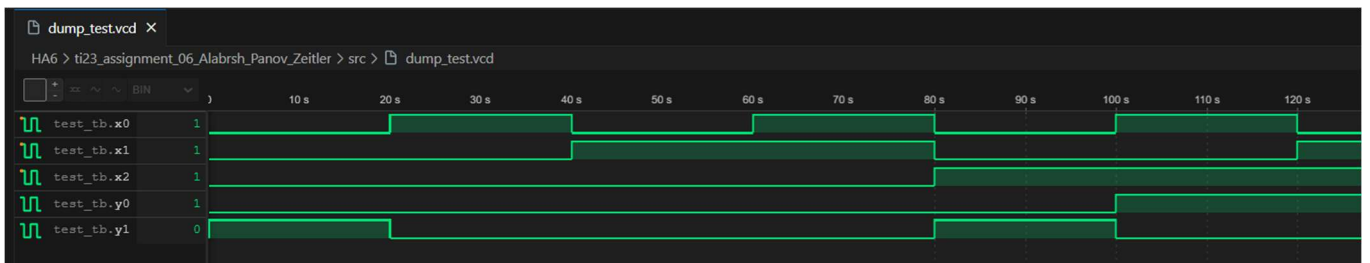
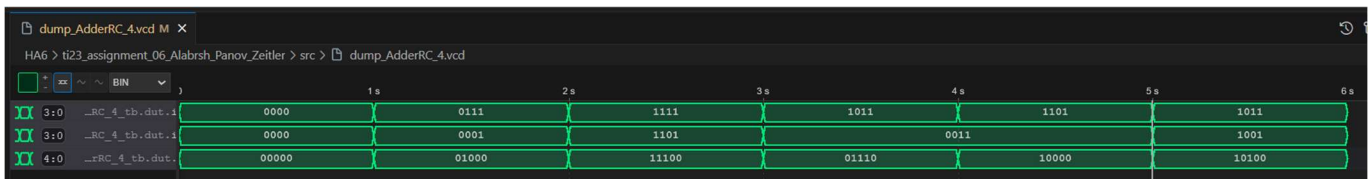


1a)	Implemented circuit in the module with added suitable delays → siehe src (glitch.sv)																					
1b)	Implemented Testbench to illustrate that the circuit exhibits a glitch when its inputs changes → siehe src (glitch_tb.sv)																					
1c)	<p>Visualized waveforms generated by the module as vector graphic with marked delay:</p>  <p>Mit der unteren waveform (dump_test.vcd) verglichen kann man sehen, dass es einen glitch in der oben gezeigten waveform (dump_glitch.vcd) gibt → blau umkreist, nachdem der glitch implementiert wurde in der geforderten Datei aus 1a und 1b.</p> 																					
2a)	Implemented 4-Bit Ripple-Carry Adder, with 4-Bit inputs for the numbers a and b to be added besides one 5-Bit output s with the result of the addition (aufgebaut auf: HalfAdder und FullAdder) → siehe src (AdderRC_4.sv)																					
2b)	<p>Completed table 1:</p> <table><thead><tr><th>a</th><th>b</th><th>s</th></tr></thead><tbody><tr><td>0b0000</td><td>0b0000</td><td><b>0b00000</b></td></tr><tr><td>0b0111</td><td>0b0001</td><td><b>0b01000</b></td></tr><tr><td>0b1111</td><td>0b1101</td><td><b>0b11100</b></td></tr><tr><td>0b1011</td><td><b>0b0011</b></td><td>0b01110</td></tr><tr><td>0b1101</td><td><b>0b0011</b></td><td>0b10000</td></tr><tr><td><b>0b1011</b></td><td>0b1001</td><td>0b10100</td></tr></tbody></table>	a	b	s	0b0000	0b0000	<b>0b00000</b>	0b0111	0b0001	<b>0b01000</b>	0b1111	0b1101	<b>0b11100</b>	0b1011	<b>0b0011</b>	0b01110	0b1101	<b>0b0011</b>	0b10000	<b>0b1011</b>	0b1001	0b10100
a	b	s																				
0b0000	0b0000	<b>0b00000</b>																				
0b0111	0b0001	<b>0b01000</b>																				
0b1111	0b1101	<b>0b11100</b>																				
0b1011	<b>0b0011</b>	0b01110																				
0b1101	<b>0b0011</b>	0b10000																				
<b>0b1011</b>	0b1001	0b10100																				
2c)	Tested implementation to check the outputs for all inputs in Table 1 through assert()-statements. → Siehe src (AdderRC_4_tb.sv)																					
2d)	<p>Visualized waveforms generated by the module for the values given in Table 1 as vector graphic. (Only show the 4-Bit inputs i_a and i_b besides the 5-Bit output o_s of the AdderRC_4 module in that order):</p> 																					

Aufgabenbearbeitung:

Aufgabe 1 → Rahaf, Christian, Cora

Aufgabe 2 → Rahaf, Christian, Cora

Aufgabe 3 → Rahaf, Christian, Cora