CPSC/ECE 3220 – Fall 2017 – Exam 2 Name: _____

Part 1: Word Bank

Write one of the words or terms from the following list into the blank appearing to the left of the appropriate definition. Note that there are more words and terms than definitions. (1.5 pts. each)

affinity scheduling	core map	not recently used	real-time scheduling	TLB hit
base and bound	demand paging	pin (e.g., pin a page)	shadow page table	TLB miss
Belady's anomaly	gang scheduling	preemption	spatial locality	TLB shootdown
checkpoint	I/O-bound task	priority boosting	superpage	working set
compute-bound task	lock ordering	priority donation	temporal locality	zero-copy-I/O
copy-on-write	log	process migration	time quantum	zero-on-reference

1. _____ An ordered sequence of steps saved to persistent storage.

2. _____ The set of memory locations that a program has referenced in the recent past.

3. _____ When a scheduler takes the processor away from one task and gives it to another.

4. _____ Programs tend to reference the same instructions and data that have been recently accessed.

5. _____ Programs tend to reference instructions and data near those that have been recently accessed.

6. _____ A widely used approach to prevent deadlock, where locks are acquired in a pre-determined order.

7. _____ An early system for memory protection where each process is limited to a specific range of physical memory.

8. _____ The ability to take a running program on one system, stop its execution, and resume it on a different machine.

9. _____ A consistent snapshot of the entire state of a process, including the contents of memory and processor registers.

10. _____ To bind a virtual resource to a physical resource, such as a thread to a processor or a virtual page to a physical page.

11. _____ A technique for transferring data across the kernel-user boundary without memory-to-memory copying, e.g., by manipulating page table entries.

12. _____ A scheduling policy where tasks are preferentially scheduled onto the same processor that they had previously been assigned to improve cache reuse.

13. _____ When a thread waits for a lock held by a lower priority thread, the lock holder is temporarily increased to the waiter's priority until the lock is released.

14. _____ Using address translation hardware to run a process without all of its memory physically present. When the process references a missing page, the hardware traps to the kernel, which brings the page into memory from disk.

Part 2: Deadlock

15. Give the four necessary conditions for deadlock. (6 pts.)

True/False. Circle **only one** of T or F. (1.5 pts. each)

Use this table for questions 16-19 for deadlock avoidance questions based on the Banker's algorithm. Treat each question independently, starting each time from the values shown in the table.

threads	max need	allocated	remaining need
A	10	1	9
B	9	5	4
C	8	4	4

Unused units = 5

16. T / F Can safely grant request of thread A for 1 units.

17. T / F Can safely grant request of thread B for 1 unit.

18. T / F Can safely grant request of thread A for 2 units.

19. T / F Can safely grant request of thread B for 2 units.

20. What type of assumptions does the Banker's algorithm make about the threads for which it manages the requests? For example, what assumptions does the algorithm make about the number and lifetimes of the threads? (2 pts.)

[poorly worded – revise if using in future]

21. Based on your answer to question 20, is the Banker's algorithm a good choice for a time-sharing system? (2 pts.)

[poorly worded – revise if using in future]

Part 3: Scheduling

Short-Term/Medium-Term/Long-Term Scheduling. Circle **only one** of S, M, L. (1 pt. each)

22. S / M / L Is called a dispatcher.
23. S / M / L Typically runs after every interrupt.
24. S / M / L Attempts to dynamically maintain a balanced job mix.

FIFO/RR/MFQ/SJF-preemptive. Circle **one or more** of F, R, M, S, as applies. (2 pts. each)

25. F / R / M / S Is preemptive.
26. F / R / M / S Uses time quantums.
27. F / R / M / S Requires future knowledge.
28. F / R / M / S Has minimum average response time for any workload.

29. Given the following list of tasks, arrival times, and service times, calculate the completion (i.e., departure) time and response (i.e., turnaround) time of each task for FIFO scheduling and again for SJF-preemptive scheduling. (12 pts.)

			---------- FIFO ----------		------ SJF-preemptive ------	
Task	Arrival Time	Service Time	Completion Time	Response Time	Completion Time	Response Time
A	0	10	_____	_____	_____	_____
B	1	6	_____	_____	_____	_____
C	3	5	_____	_____	_____	_____

Aging/Boosting. Circle **only one** or A or B. (1 pt. each)

30. A / B Priority increases while waiting.
31. A / B Priority increase value is specified as a parameter to the signal operation for I/O completion.

32. Devise a workload when FIFO is optimal for average response time. (2 pts.)

[revise? Describe the properties of a workload for which FIFO…]

33. Devise a workload when FIFO is pessimal for average response time. (2 pts.)

33. Devise a workload when RR is pessimal for average response time. (2 pts.)

34. Explain the priority inversion problem, and explain how dynamic priority scheduling with aging would solve the problem. (4 pts.)

[need to be specific about the case of priority inversion with bounded locks]

Part 4: Address Translation

Base and Bound/Segmentation/Paging. Circle **one or more** of BB, S, or P, as applies. (1.5 pts. each)

35. BB / S / P Can have external fragmentation.
36. BB / S / P Performs a bounds/limit check on the offset field.
37. BB / S / P Requires loading of one or more privileged CPU registers on a process switch.
38. BB / S / P Process memory image is divided into variable-length regions that match the program structure; each region has a unique identifier field that cannot be changed when adding to the offset field.

39. Consider a simple architecture with paged segments in which three-decimal-digit virtual addresses are used. The segment id is the first decimal digit, the virtual page number is the second decimal digit, and the offset is the last decimal digit. The physical address are two decimal digits: the page frame is the first decimal digit, and the offset is the second decimal digit. E.g., the virtual address 111 would be translated to physical address 51 given the following segment and page table entries. Give the physical addresses for the following virtual addresses. (3 pts.)

Segment Table	**Page Table A**	**Page Table B**
0 = points to page table A, segment length is 3 pages	0 = present, page frame 4	0 = present, page frame 7
1 = points to page table B, segment length is 2 pages	1 = not present	1 = present, page frame 5
X (other values are invalid)	2 = present, page frame 3	X (other values are invalid)
	X (other values are invalid)	

(a) Virtual address 000 is translated to physical address _____.

(b) Virtual address 104 is translated to physical address _____.

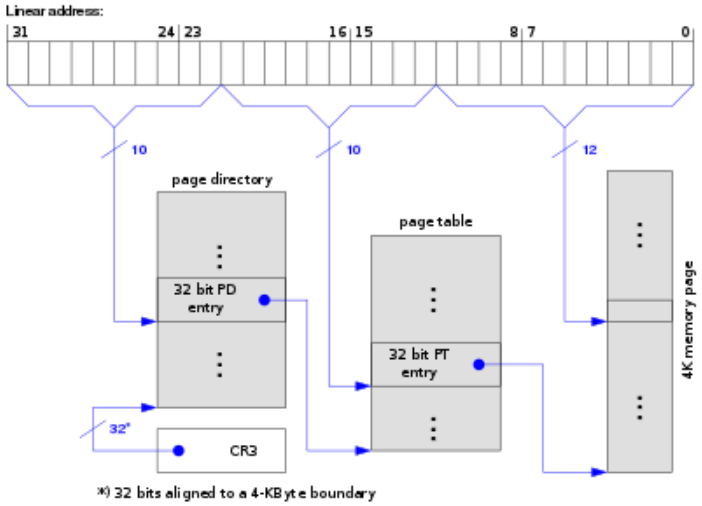
40. Using the diagram format of the textbook (letter means miss, and "+" means hit), show how the system would fault pages into the four frames of physical memory using the LRU replacement policy. (4 pts.)

REF	**A**	**B**	**C**	**D**	**B**	**A**	**E**	**F**	**B**	**F**	**A**	**G**	**E**	**F**	**A**
1															
2															
3															
4															

41. Using the diagram format of the textbook (letter means miss, and "+" means hit), show how the system would fault pages into the four frames of physical memory using the clock replacement policy (i.e., FIFO second chance; when faulted in, each page has its use bit set to 0 so that information about subsequent use can be recorded). (4 pts.)

REF	**A**	**B**	**C**	**D**	**B**	**A**	**E**	**F**	**B**	**F**	**A**	**G**	**E**	**F**	**A**
1															
2															
3															
4															

Answer questions 42-46 using powers of 2 and a memory byte as the addressable unit. (Diagram is from Wikipedia.)



42. What is the name of the paging scheme shown above? (2 pts.)

43. What is the size in bytes of a page table in the paging scheme shown above? (2 pts.)

44. Consider a contiguous data structure of 16 MB. How many pages do you need to store this structure? (2 pts.)

45. How many page directory entries do you need to store the data structure in question 44? (2 pts.)

46. Explain how the paging scheme shown above supports a sparse address space. (3 pts.)

XC. When a processor does a TLB shootdown, must it wait until other processors respond or can it proceed in parallel while other processors are handling the shootdown? Explain your answer. (2 pts.)