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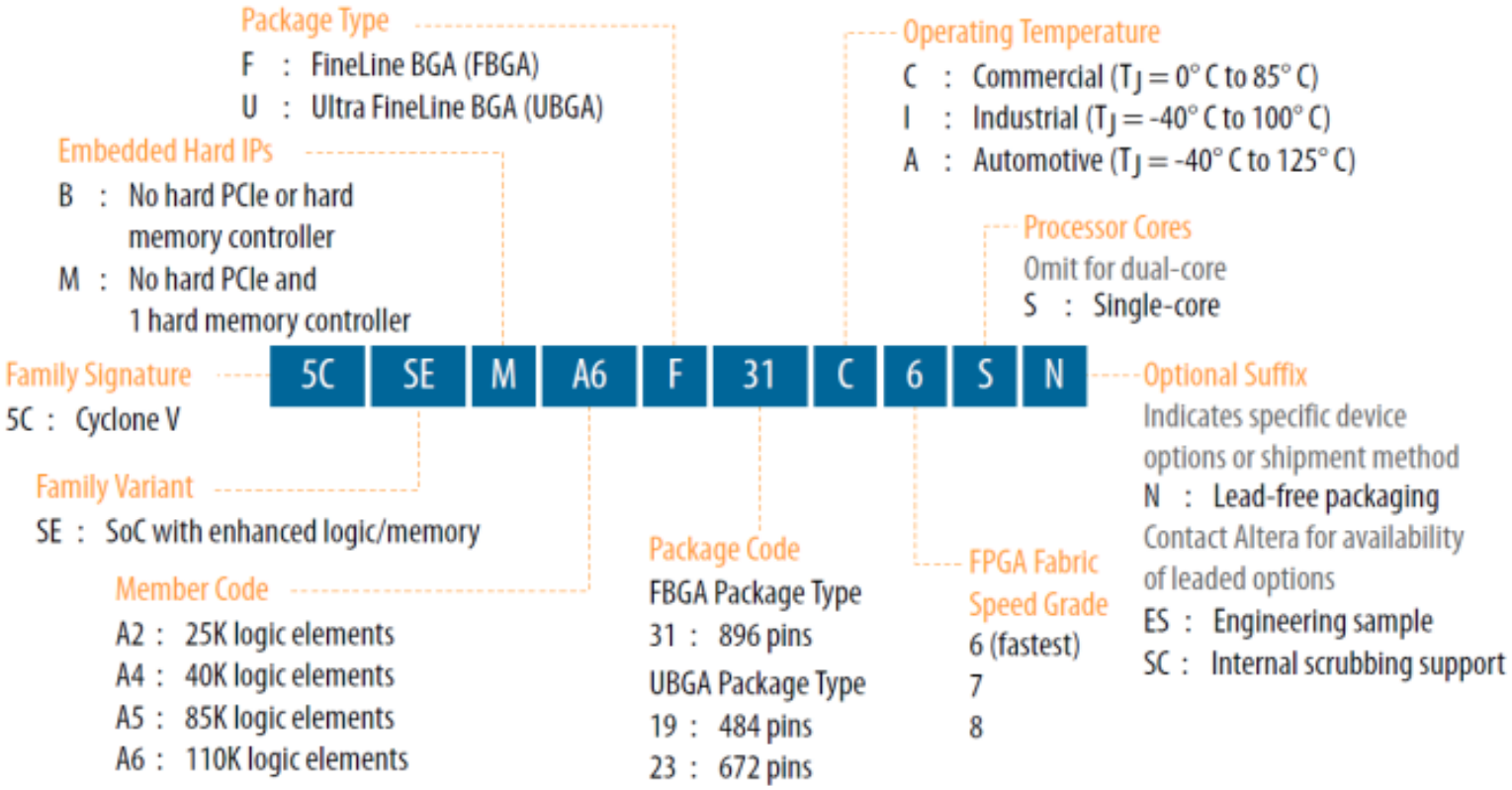
ECE327

Altera Notes

Cyclone V-SE: Low Cost, Low Power

- Low Power
  - Up to 40% lower power consumption
- FPGA Features
  - Up to 110K LEs (Altera's Logic Elements)
  - Up to 5.6 Mb of Embedded RAM
  - Up to 224 18x18 Embedded Multipliers
  - Up to 288 user I/O
- Dedicated ARM Cortex-A9 MPCore Hard Processor
  - Up to 1GB DDR3 RAM
  - Up to 925 MHz Clock Rate
  - Up to 181 user I/O
  - Single or Dual Core

Cyclone V-SE Device Packing Information



Cyclone V-SE General Features

- Contains a two-dimensional row- and column-based architecture to implement custom logic
- Column and row interconnects of varying speeds provide signal interconnects between logic array blocks (LABs), embedded memory blocks, and embedded multipliers
- The logic array consists of LABs, with 16 logic elements (LEs) in each LAB
  - An LE is a small unit of logic providing efficient implementation of user logic functions (LUTs, FFs, etc.)
  - LABs are grouped into rows and columns across the device

Cyclone V-SE General Features (continued)

- Global clock network and up to six phase-locked loops (PLLs) for FPGA and 3 PLLs for HPS
  - Consists of up to 16 global clock lines that drive throughout the entire device
  - Can provide clocks for all resources within the device, such as input/ output elements (IOEs), LEs, embedded multipliers, and embedded memory blocks
  - Global clock lines can also be used for other high fan-out signals
- PLLs provide general-purpose clocking with clock synthesis (can create an internal clock) and phase shifting (delay the clock edge) as well as external outputs

Cyclone V-SE General Features (continued)

- M10K memory blocks are true dual-port memory blocks with 10K bits of embedded SRAM memory plus parity
  - Provide dedicated true dual-port, simple dual-port, or single-port memory up to 40-bits wide (RAM and ROM)
  - Arranged in columns across the device between certain LABs
  - Byte enable
- Single-port RAM: read and write operations share the same address port – only one operation at a time
- Simple dual-port RAM: one read port and one write port – two operations at a time (one read and one write)
- True dual-port RAM: two read/write ports – write to or read from either port (read/write, 2 reads, or 2 writes)
- Common Functions: RAM, ROM, Shift register, FIFO buffer

Cyclone V-SE General Features (continued)

- Each embedded multiplier block
  - Can implement up to either two 9 X 9-bit multipliers, or one 18 X 18-bit multiplier
  - Embedded multipliers are arranged in columns across the device
- Each I/O pin is fed by an IOE located at the ends of LAB rows and columns around the periphery of the device
  - Each IOE contains a bidirectional I/O buffer and three registers for registering input, output, and output-enable signals

Type	I/O Standard
Single-Ended I/O	LVTTL, LVCMOS, SSTL, HSTL, PCI, and PCI-X
Differential I/O	SSTL, HSTL, LVPECL, BLVDS, LVDS, mini-LVDS, RSDS, and PPDS

Altera Cyclone V-SE Programmable Devices

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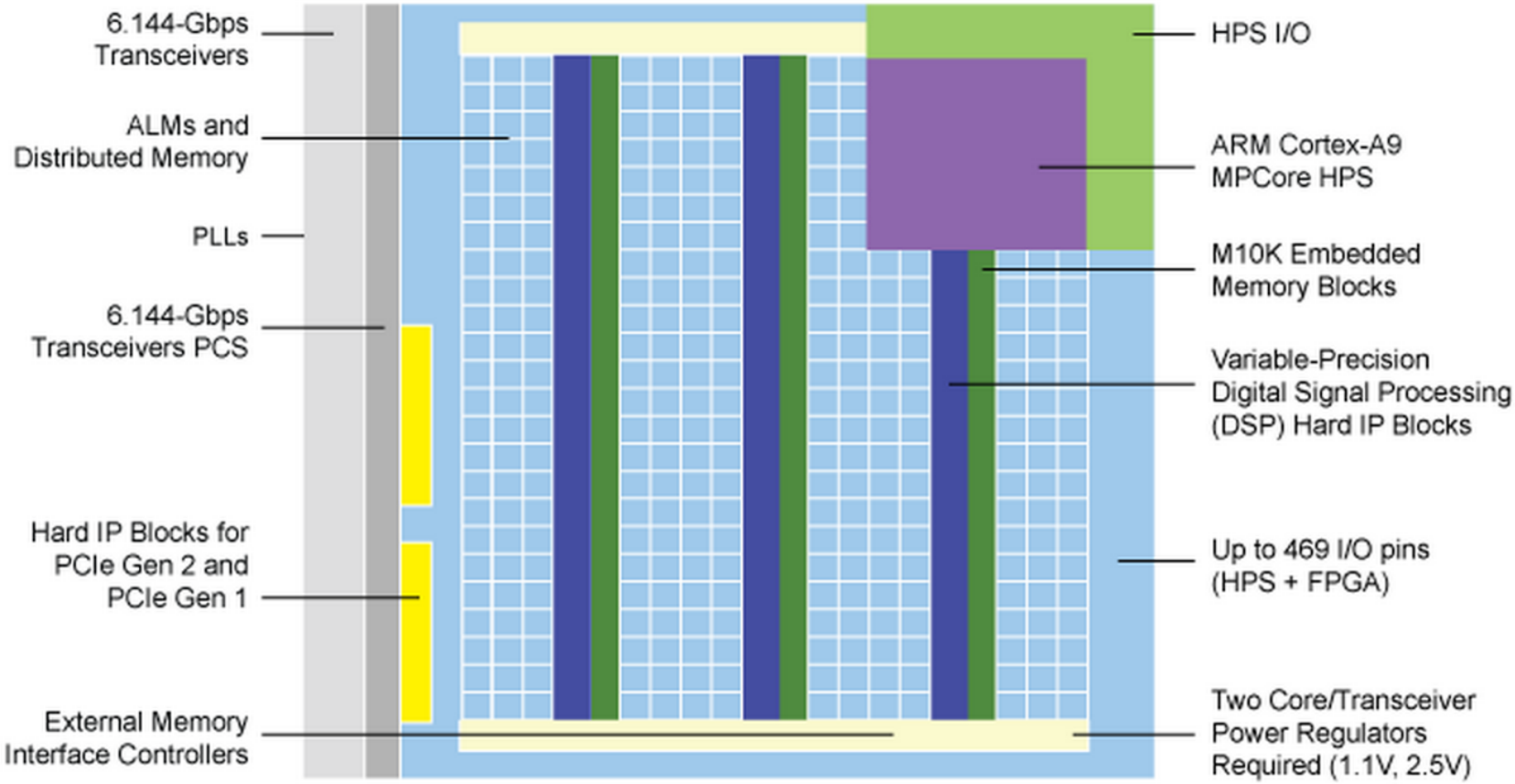
Table 10: Maximum Resource Counts for Cyclone V SE Devices

Resource		Member Code			
		A2	A4	A5	A6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,434	15,094	32,075	41,509
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6
HPS PLL		3	3	3	3
FPGA GPIO		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
ARM Cortex-A9 MPCore Processor		Single- or dual-core	Single- or dual-core	Single- or dual-core	Single- or dual-core

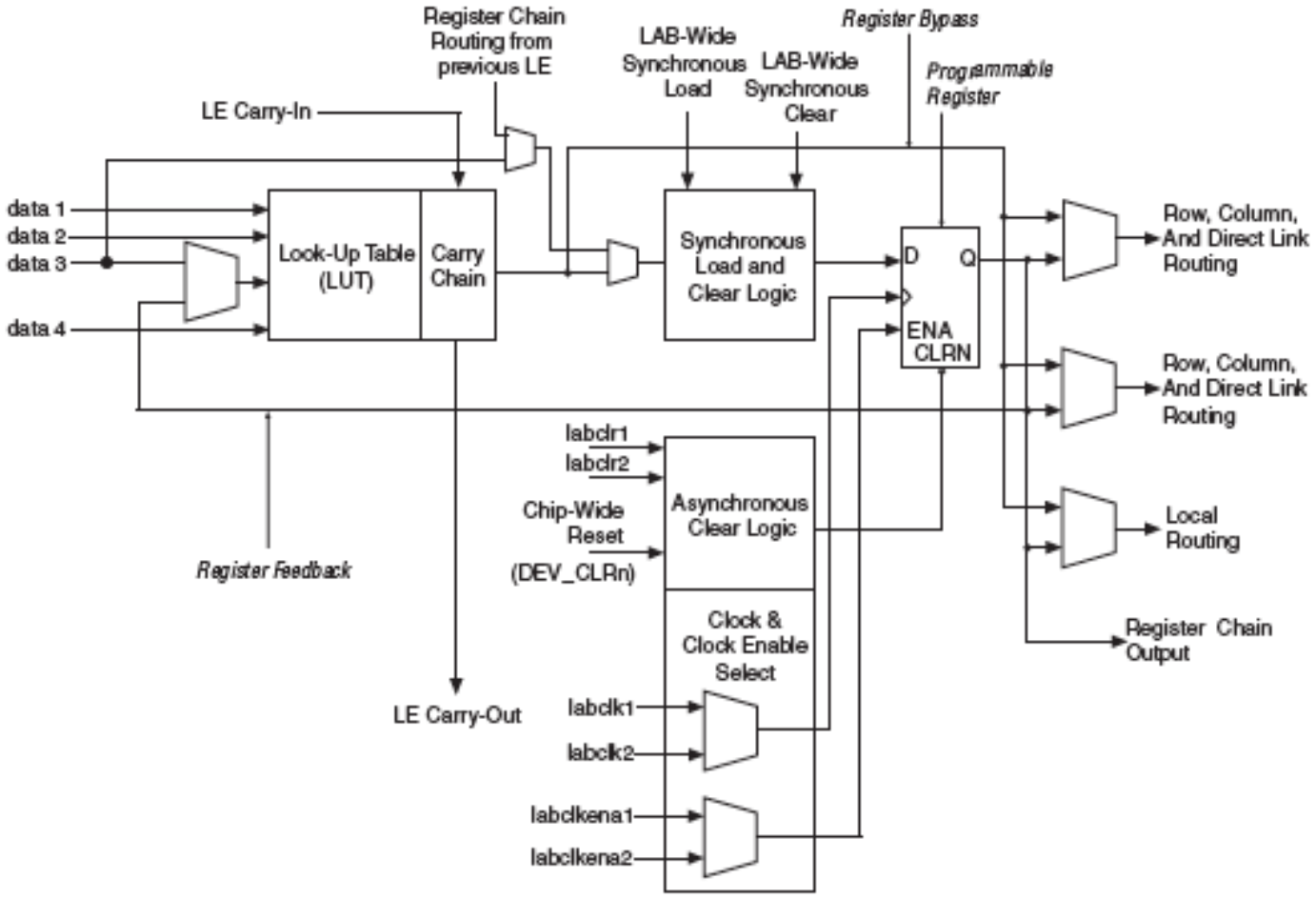
Cyclone V – SE General Device Block Diagram



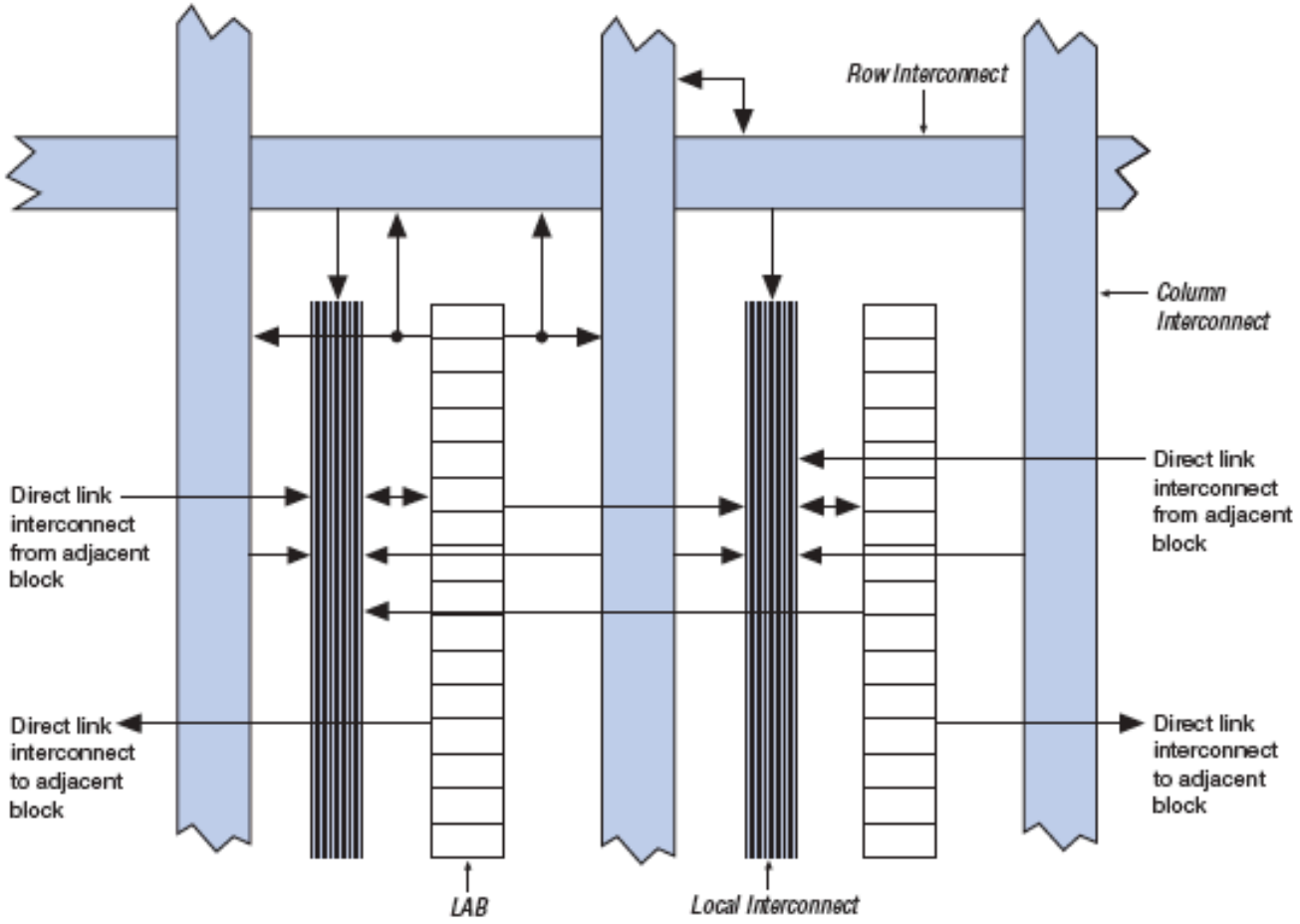
Cyclone V-SE Logic Element (LE)

- A four-input look-up table (LUT) that can implement any function of four variables
- A programmable register
- A carry chain connection
  - A fast interconnect between adjacent LABs
- A register chain connection
  - A fast, registered, connection between adjacent Les
- The ability to drive all types of interconnects (routing)
  - Local, row, column, register chain, and direct link interconnects
- Support for register packing
  - Combining a register with combinational logic in a design
- Support for register feedback
  - Feedback from flip-flop output back into the LUT

Cyclone V-SE Logic Element (LE)



Cyclone V-SE LAB Structure



Cyclone V-SE Basic IOE Structure