CLEMSON UNIVERSITY

# ECE 3270 INTRODUCTION

## Instructor & Website

- Dr. Melissa C. Smith
  - Office Hours: To be announced (Also, by appointment)
    - Riggs 100-G
    - 864-656-2119
    - smithmc@clemson.edu
- Course Website hosted on Canvas

## My Backgroud

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- ASIC and integrated system design for 10+ years at ORNL
- HPC systems and performance 3+ years at ORNL
- Since 2006 at Clemson
  - Current research in Accelerator Computing (GPUs/FPGAs/ Xeon Phi) and Multi-core Computing
  - Application performance optimization
  - Deep Learning and other Machine Learning techniques

## Course Goals

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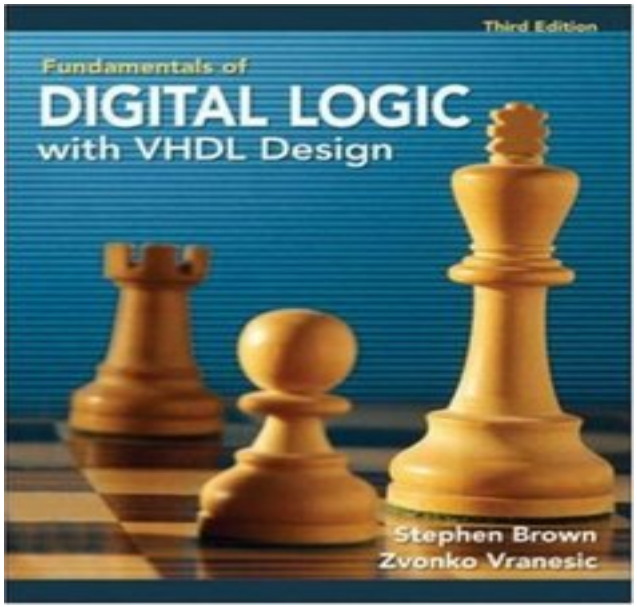
- Digital System Design Principles
- Modern design methodologies (CAD and HDL)
- FPGA Architectures
- Design for FPGA devices
- Design of control and timing circuitry (State Machines)
- Design of high-speed ALUs
- Design for testability
- Synchronous and Asynchronous systems

## Textbook

Fundamentals of Digital Logic with VHDL Design, 3rd Edition




by

Stephen Brown

And Zvonko Vranesic

ISBN: 9780077221430

## Grading

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- Exams: 50% (20% Midterm; 30% Final)
- Homework and Quizzes: 15%
- Projects/Labs: 35%

- All assignments are due at the START of class
- **Students are required to complete <u>ALL projects on time and submit all code to the assign server</u> to receive a passing grade in the course**… NO EXCEPTIONS!!!!

## Academic Honesty

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- Unless told otherwise, labs and homework assignments must be done individually
  - All assignments will be checked for cheating
  - You may discuss assignments, but ALL of the work submitted must be your own
- Any copying of non-trivial code is unacceptable!
  - Non-Trivial = more than a line or so
  - Includes reading someone else's code and then going off to write your own
  - Includes copying code from the Internet!!!!
- Giving/receiving help on an exam is unacceptable!
- Penalties for misconduct:
  - See Student Handbook and links in Syllabus

## Attendance Policy

- If you do not come to class, it will be apparent on exams and quizzes
- Out of respect to the Professor and your classmates,
  → BE ON TIME to class!
  - If you are late and I am giving a quiz, you will receive a Zero
  - I may take photos of class to record attendance
- If you are sick, stay at home!
  - If obviously sick, you will be asked to leave
  - Missed tests cannot be retaken, except with doctor's note

## Tentative Schedule

- See Syllabus

Homework:

- Read Chapters: 1, 2.9, 2.10, 12, & Appendix A

- Complete Lab 0 (Tutorial)