NTSC video generator on Xilinx Spartan 6 series FPGA

Introduction

NTSC(National Television Standard Committee) is an analog color video encoding standard used for broadcasting color or black and white video signals.

It consists of luminance(black and white) and chrominance(color and saturation) information encoded in it. The luminance is encoded as varying voltage between 0.3 volt to 1 volt. 0.3 volt corresponds to black and 1 volt corresponds to white, while any voltage between these two values corresponds to shade of gray. The chrominance is encoded using a color subcarrier of 3.57954 MHz, whose phase difference with a reference color burst gives HUE(color) information while its amplitude gives the saturation information.

Since it is an analog video standard, instead of displaying images on pixel by pixel basis it is displayed one scan line at a time, from left edge to the right from top to bottom.
In order to synchronize the scan lines for proper image positioning, a horizontal blanking signal is used for synchronizing purpose while a vertical blanking signal is used to inform that all the scan line of current frame or filed(odd and even field makes one frame) has been laid and next frame or field starts now. The vertical blanking is used to move the electron beam back at the top left corner so that a new field or frame can be drawn.

Problem analysis

The NTSC video signal varies between 0 volt to 1 volt i.e. 1 volt peak to peak. The FPGA should be able to produce voltage between these levels with fine resolution. It should be considered that these voltage level should exist at the input of the RCA video jack whole input impedance is 75 Ω. So the output impedance of the generator and the input impedance of 75 Ω should be considered while calculating the voltage. The FPGA should produce various voltage levels for a specific period of time to produce the

Horizontal blanking and vertical blanking which is used for synchronization. The time information of a single scan line including the horizontal blanking and active video signal is shown in the diagram below.

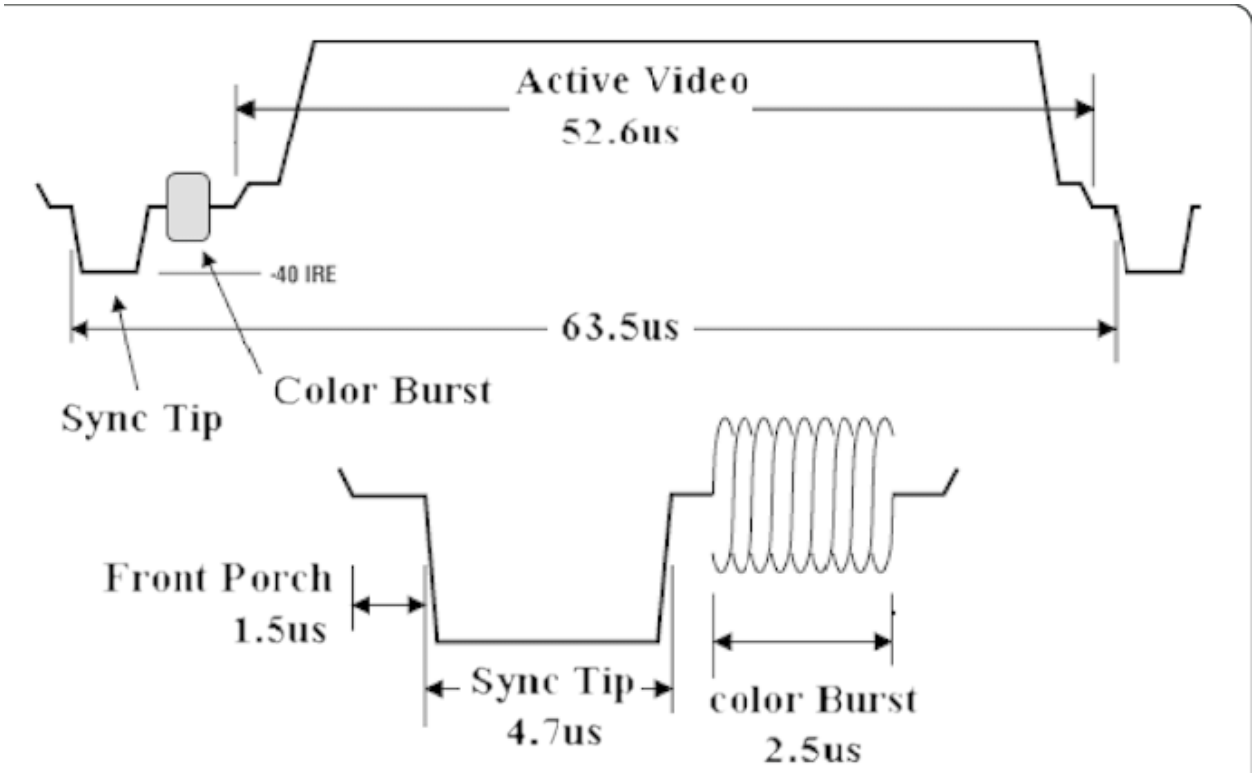


FIG: SCAN LINE TIMING INFORMATION
(https://www.researchgate.net/figure/The-all-white-NTSC-composite-video-signal-19_fig2_259979856)

The NTSC vertical blanking signal produces short pulses during its equalization and vertical sync duration, while it sends an empty video frame for the remaining 10 or 11 frames.
It's depicted in the figure below which is obtained from the analog devices ***ADV7393*** datasheet and manual. Further more information about timing of the vertical blanking can be obtained from the Texas Instruments video amplifier ***OPA361*** datasheet and this ***scienceDirect*** publication.

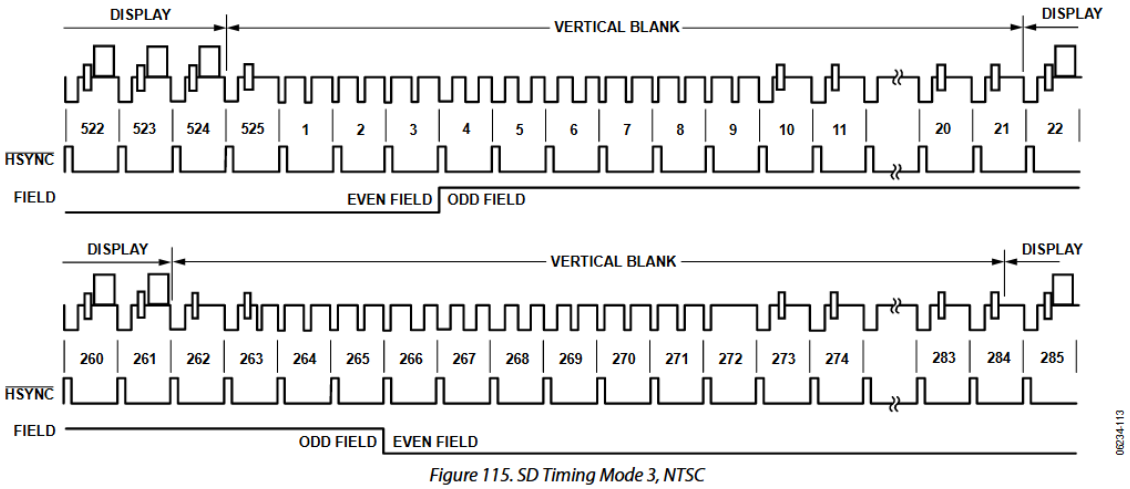


Figure 115. SD Timing Mode 3, NTSC

Fig: Vertical blanking information

Methodology

The NTSC video generator will be implemented on the Xilinx spartan 6 series board which has XC6SLX93TQG114 part. The NTSC signal has various states for each scan line such as Front Porch, Horizontal Sync Tip, Breezeway, Colorburst, Backporch and active video. Different voltage levels are needed at the output for these different states. The voltage level can be produced using the STD_LOGIC_VECTOR output to produce a bus output representing the discrete voltage level in binary and using a R2R ladder network to convert these digital values to discrete analog values. Using this method gives more resolution. The output impedance of the R2R ladder is always R, so R should be selected in such a way that the output will be 1 volt peak for maximum output across the 75Ω input impedance of the RCA jack.

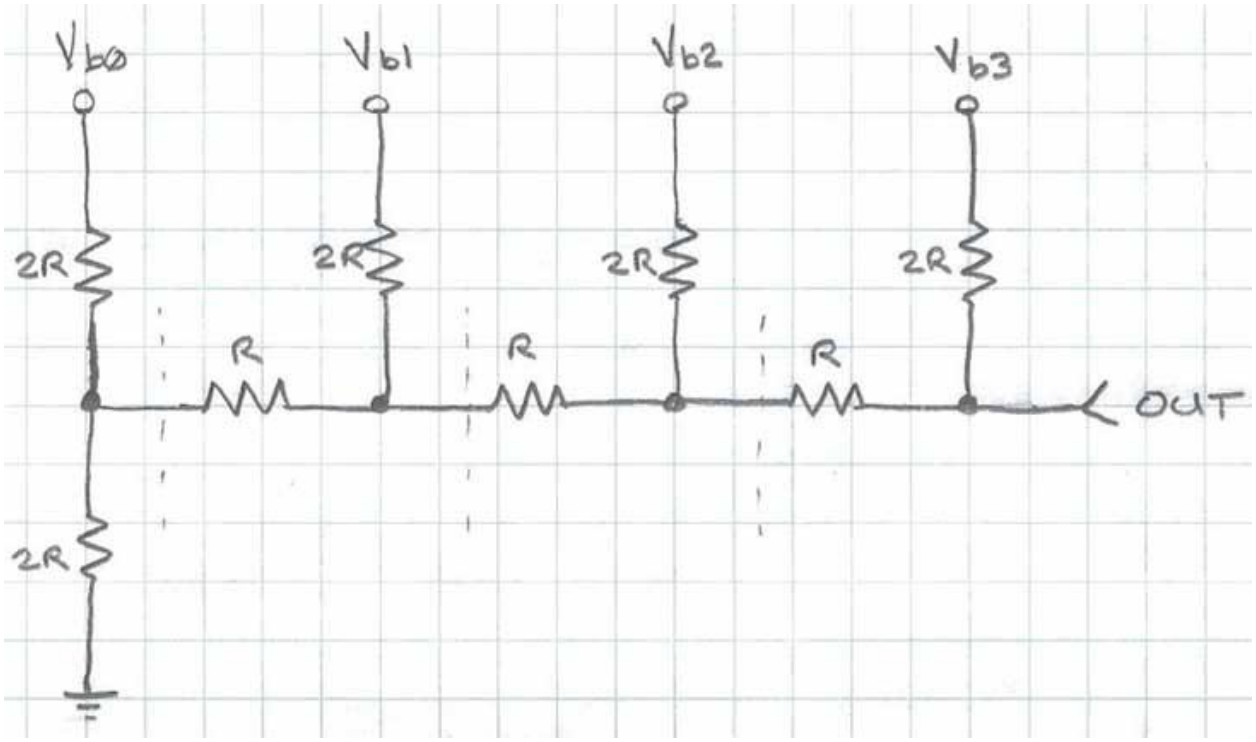


Fig: R2R ladder(https://www.tek.com/en/blog/tutorial-digital-analog-conversion-r-2r-dac)

$1\,volt = 75/(75 + R) \times 3.3\,volt$
$R = 75 \times 3.3 - 75$
$R = 172.5\Omega$

To step from one step to another, a state machine will be used to step from the Front porch to Sync tip, from the Sync tip to Breezeway and so on. The state machine can be easily implemented by using a counter which keeps track of the time that has passed since the change of last state. The counter time can be compared with the time that it takes to complete a particular state such as the front porch which lasts for 1.5µs. For this entire duration FPGA outputs about 285.72 mV(0 IRE) which is the blanking level. Once the timer reaches this time, the state changes to the next state that is Sync tip.

Hence state machines can be implemented within the FPGA to move from one state to another and output specific line levels for a certain time period.
The FPGA board has a 50 MHz external clock, whose time period is 20 nS. Hence the smallest time that can be tracked is 20 nS. Now this clock is used for Counter such that the counter can track time in the multiple of 20nS. For example if the Counter counts to

23 that means (23*20)=460nS has passed. This simple principle can be used to track the time passed for the current state.

The table below shows the counter value, time and IRE level for each line state.

Line State	Time(µs)	Counter equivalent(Time/20ns)	IRE level(mV Level)	FPGA output(binary)
Front Porch	1.5	75	0 (285.72mV)	73(0b01001000)
Sync Tip	4.7	235	-40 (0 mV)	0
Breezeway	0.6	30	0 (285.72mV)	73(0b01001000)
Color Burst	2.5	125	40 IRE p-p(285.72mV p-p)	
Back Porch	1.6	80	0 (285.72mV)	0
Active Video	52.6	2630	Varies according to picture information, 7.5 IRE(339.292 mV) for Black level and 100 IRE(1 V) for white level	From 87(0b01010111) to 255(0b11111111)

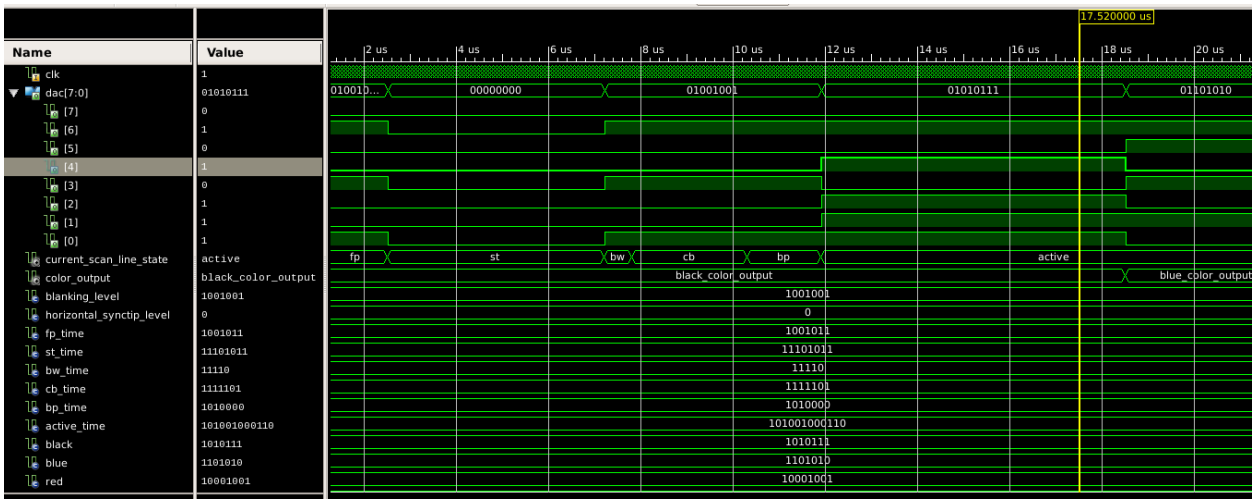
For now the NTSC video signal will only produce Luminance information for test purposes.

To produce the vertical blanking, the same principle can be used to generate the signal. Based on the correct counter value and signal level the vertical blanking can be easily generated.

Testbench Simulation for scan line, horizontal blanking and vertical blanking

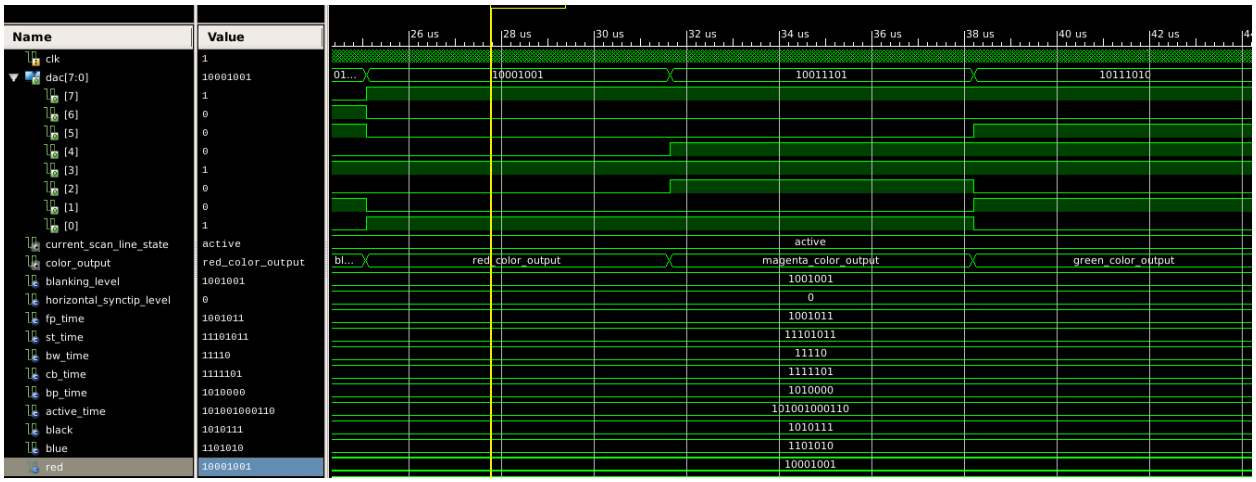
Initial testbench for the scan line and horizontal blanking

Based on the principle stated above, VHDL code and its simulation verifies it. Figure below depicts different sections of scan lines.

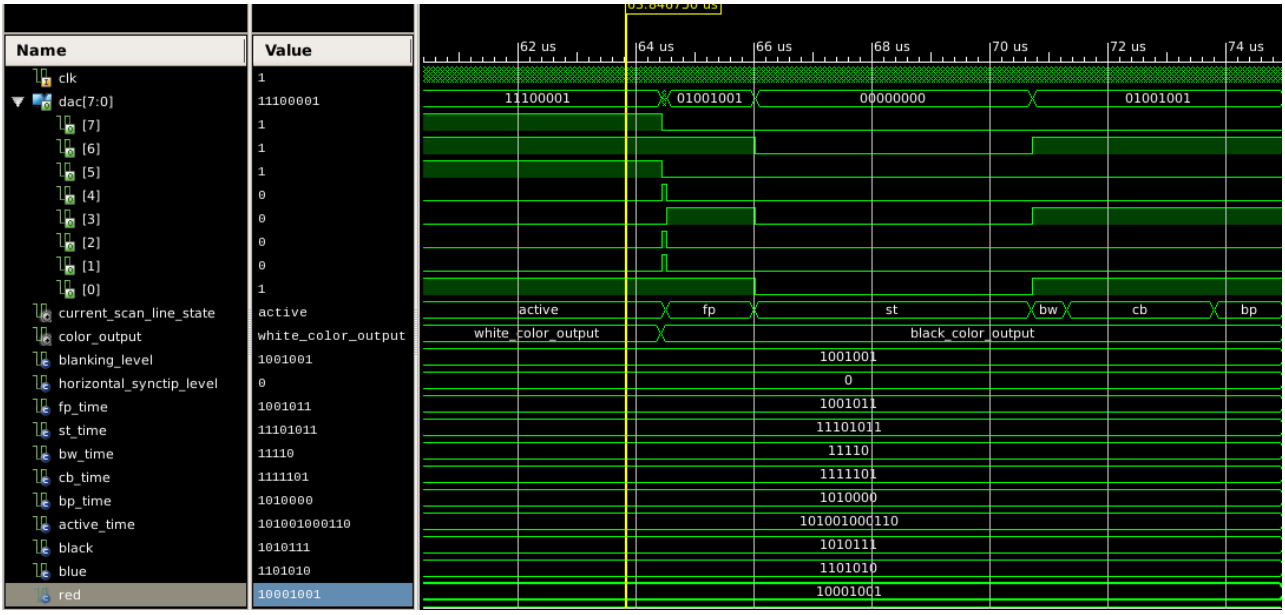


The figure above shows the corresponding signal level output from the FPGA for different states such as the front porch, sync_tip, breeze way, color_burst and back_porch. For now the color burst is not implemented.

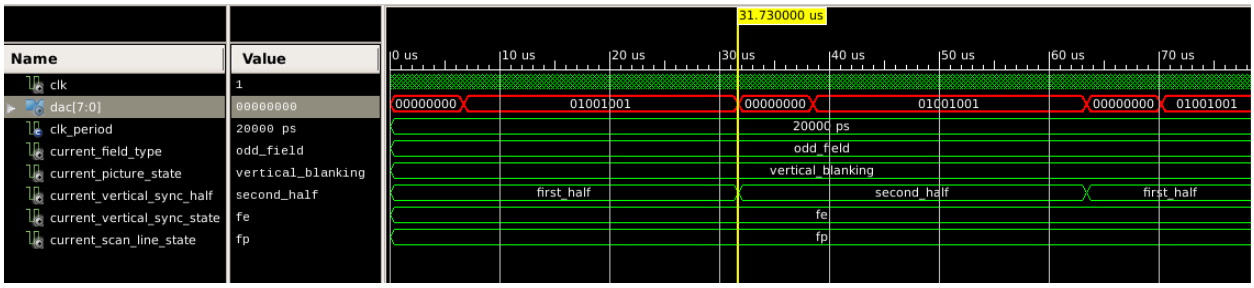
The figure below shows the different signal level output from the FPGA during the ACTIVE video state. Different signal levels correspond to different shades of gray since the chrominance information is missing.



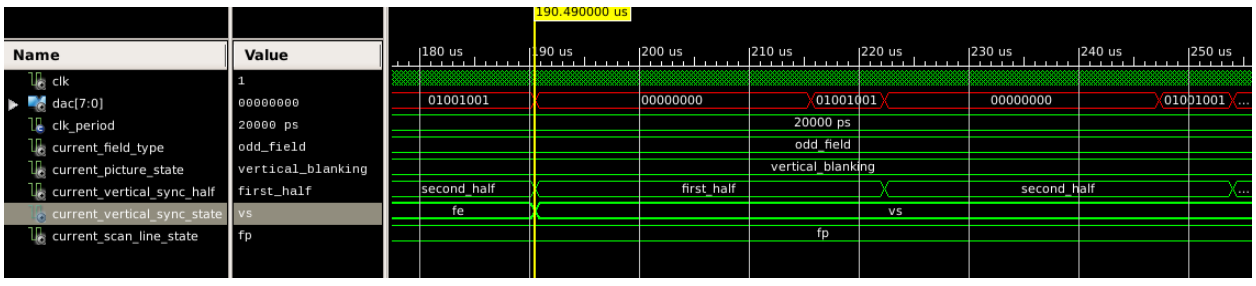
Finally the state wraps back to the horizontal blanking for the next scan line.



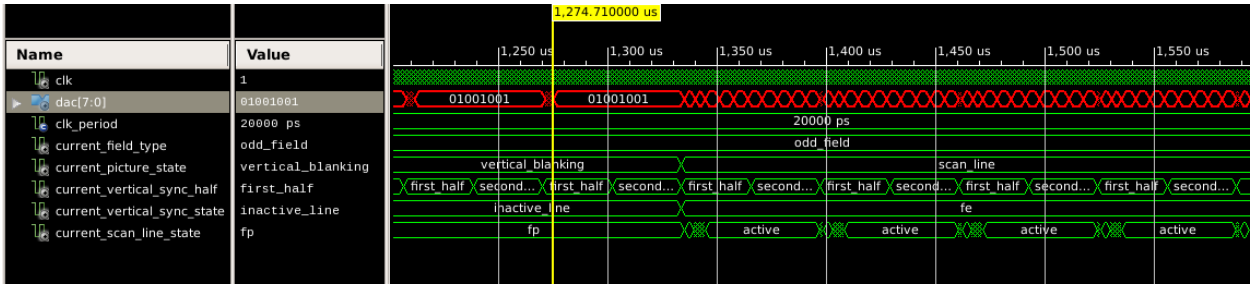
Test bench for the vertical blanking and entire video frame



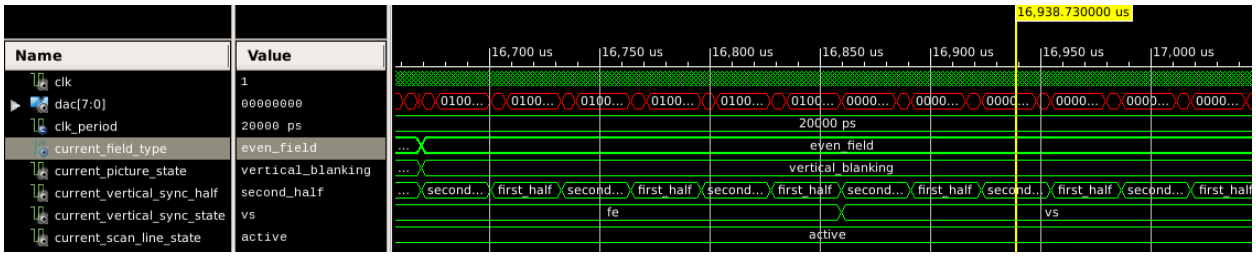
The figure above shows the screenshoot depicting the equalizing pulses produced during the vertical blanking.



The figure above shows the sync pulses outputted by the Fpga during the vertical sync.



The figure above shows the transition from the vertical blanking to drawing the scan line.



The figure above shows the completion of the odd field and starting of the even field.

FPGA pin and used bank

This project utilized one input for the clock which is connected to the onboard crystal oscillator and 8 output for the binary output of corresponding signal level.

It uses pin40, pin41, pin43, pin44, pin45, pin46, pin47 and pin48 located at the bottom bank.

2	IO_L48P_D7_2	P48	BL	
2	IO_L48N_RDWR_B_VREF_2	P47	BL	
2	IO_L49P_D3_2	P46	BL	
2	IO_L49N_D4_2	P45	BL	
2	IO_L62P_D5_2	P44	BL	
2	IO_L62N_D6_2	P43	BL	
2	IO_L64P_D8_2	P41	BL	
2	IO_L64N_D9_2	P40	BL	

Fig:pin description of XC6SLX9 part

Table 1-7: **Spartan-6 FPGA Bank Numbering**

Bank	Locations	Description
0	Top	All devices
1	Right	All devices
2	Bottom	All devices; contains most configuration pins
3	Left	All devices
4	Left, Top	Extra bank in LX75/LX75T, LX100/LX100T, LX150/LX150T in FG(G)676 and FG(G)900 packages
5	Right, Top	Extra bank in LX75/LX75T, LX100/LX100T, LX150/LX150T in FG(G)676 and FG(G)900 packages
101	Top, Left	GTP transceiver bank in all LXT devices
123	Top, Right	GTP transceiver bank in LX45T, LX75T, LX100T, LX150T
245	Bottom, Left	GTP transceiver bank in LX75T, LX100T, LX150T in FG(G)676 and FG(G)900 packages
267	Bottom, Right	GTP transceiver bank in LX75T, LX100T, LX150T in FG(G)676 and FG(G)900 packages

Figure 1-1 through Figure 1-5 visually describe a device view of the FPGA bank numbering.

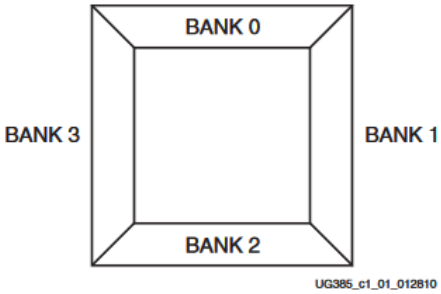
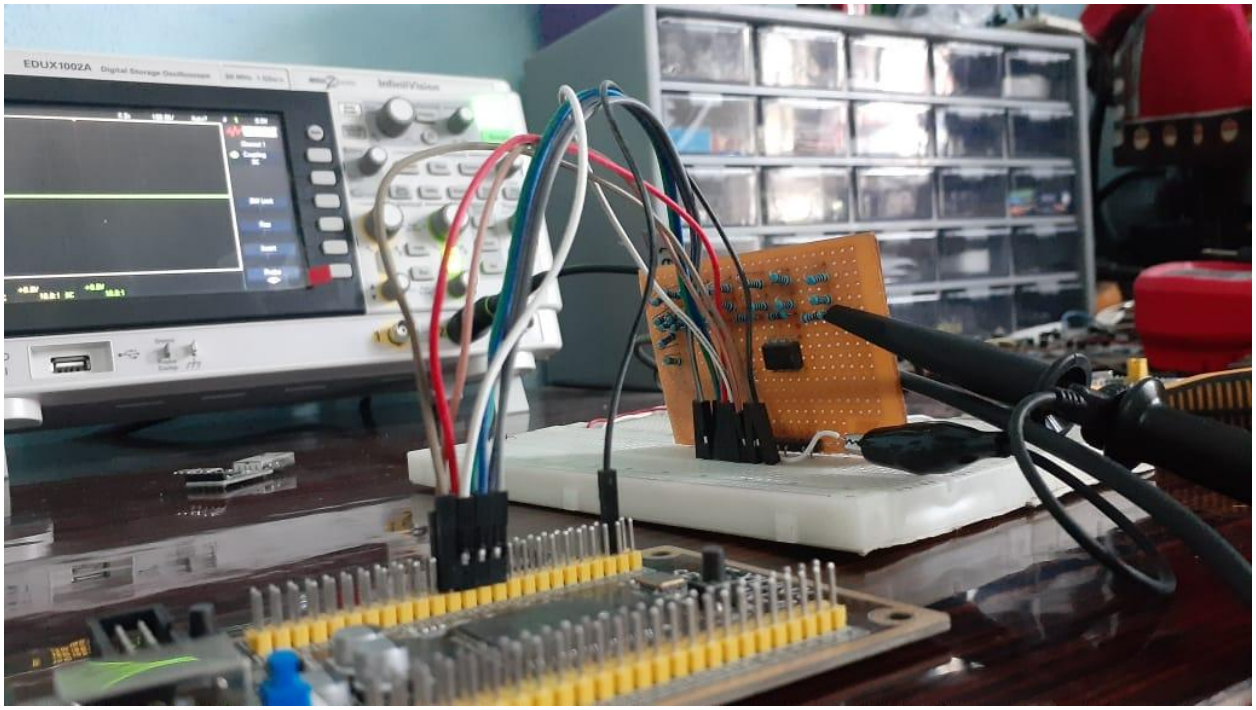


Figure 1-1: **I/O Banks for All LX4, LX9, LX16, LX25, and LX45 Devices and for the LX75, LX100 and LX150 Devices in the CS(G)484 and FG(G)484 Packages**

Test set-up

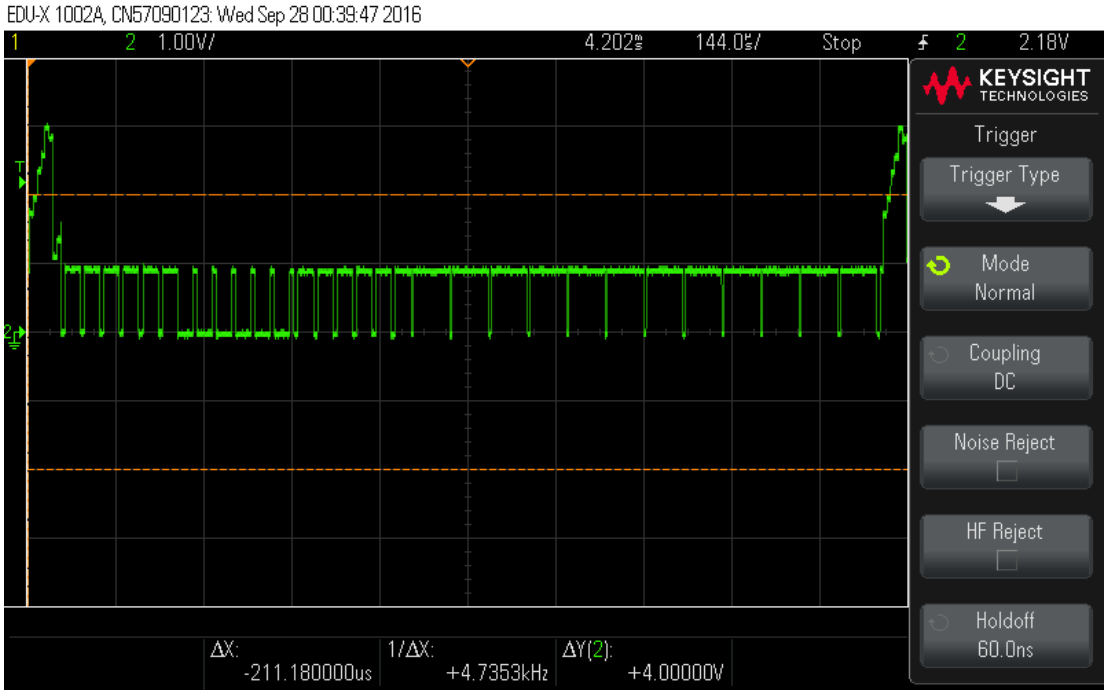
The FPGA is connected to a 8 input R-2R ladder network to convert the digital data from the FPGA to the discrete analog signal levels needed. The network is made of resistor values of 1KΩ and 2KΩ. This is used for test purpose only, this resistance value is not suitable for actually driving the Composite video input which has input impedance of about 75Ω.

The figure below shows the test set-up and FPGA circuit connection. The board connected on the breadboard is the R-2R ladder connected to the FPGA digital pin that outputs 3.3 volts.



Output signal and measurement

The figure below shows the screenshot taken from the oscilloscope, which is probing the R-2R ladder output.



The figure above shows the vertical blanking generated by the FPGA.

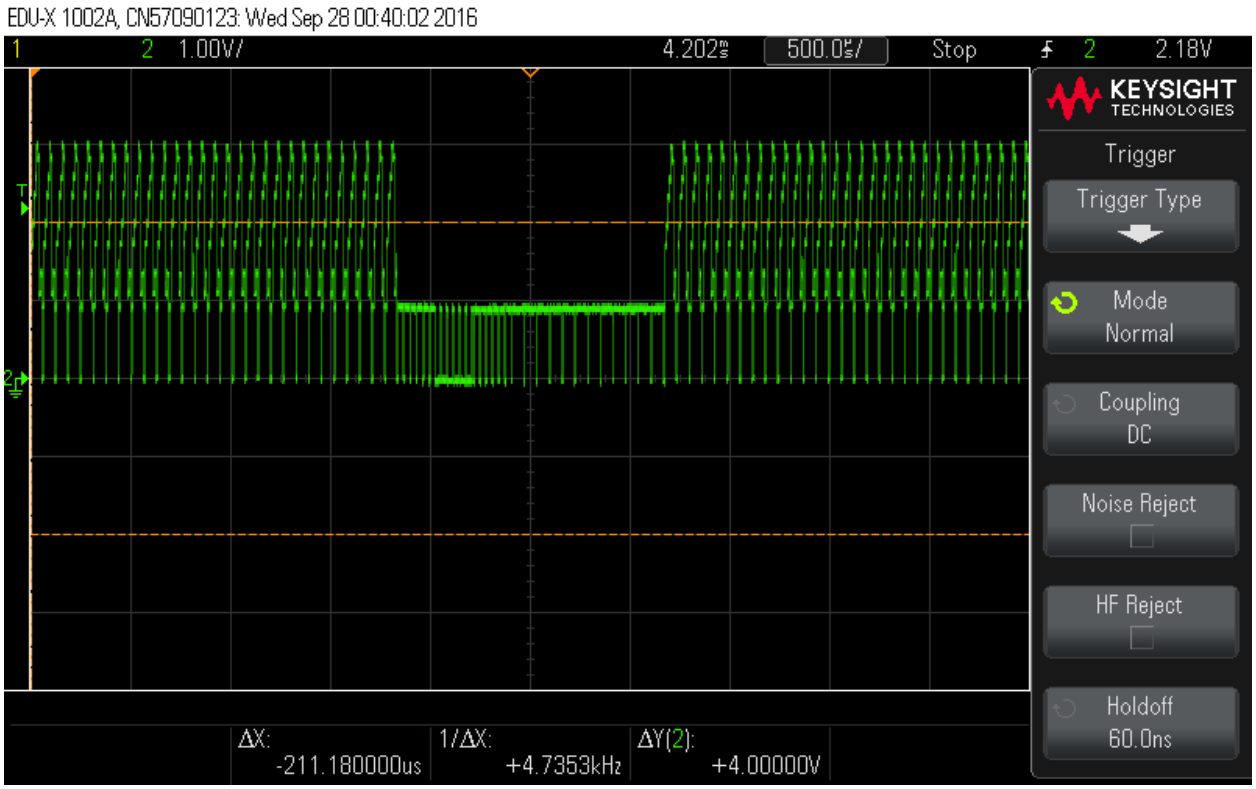
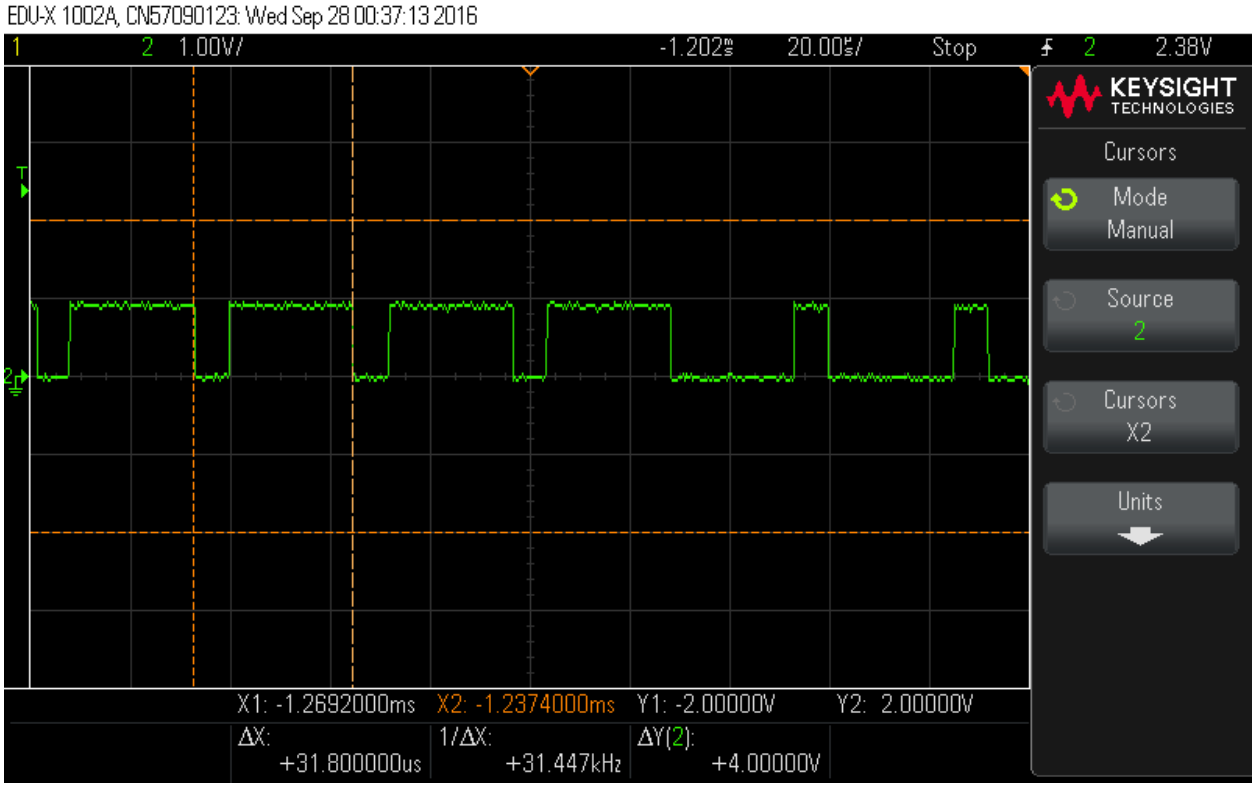
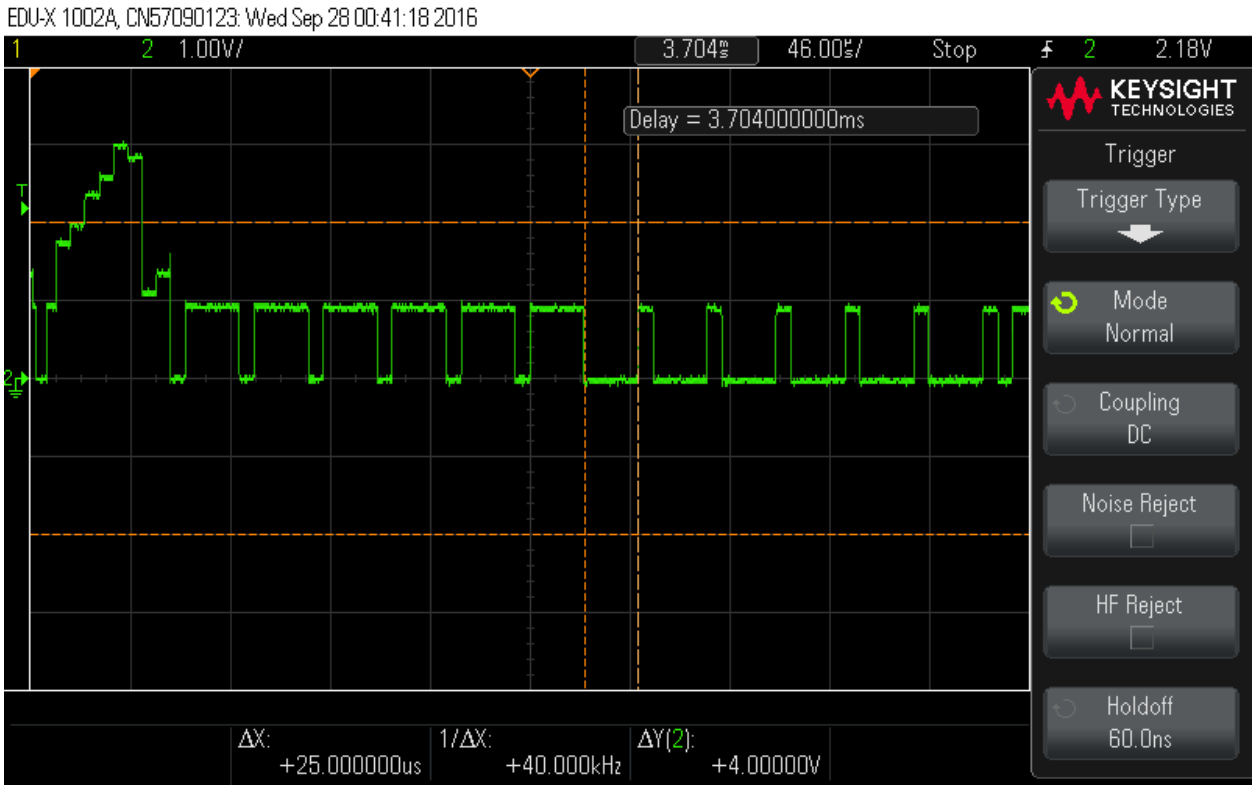


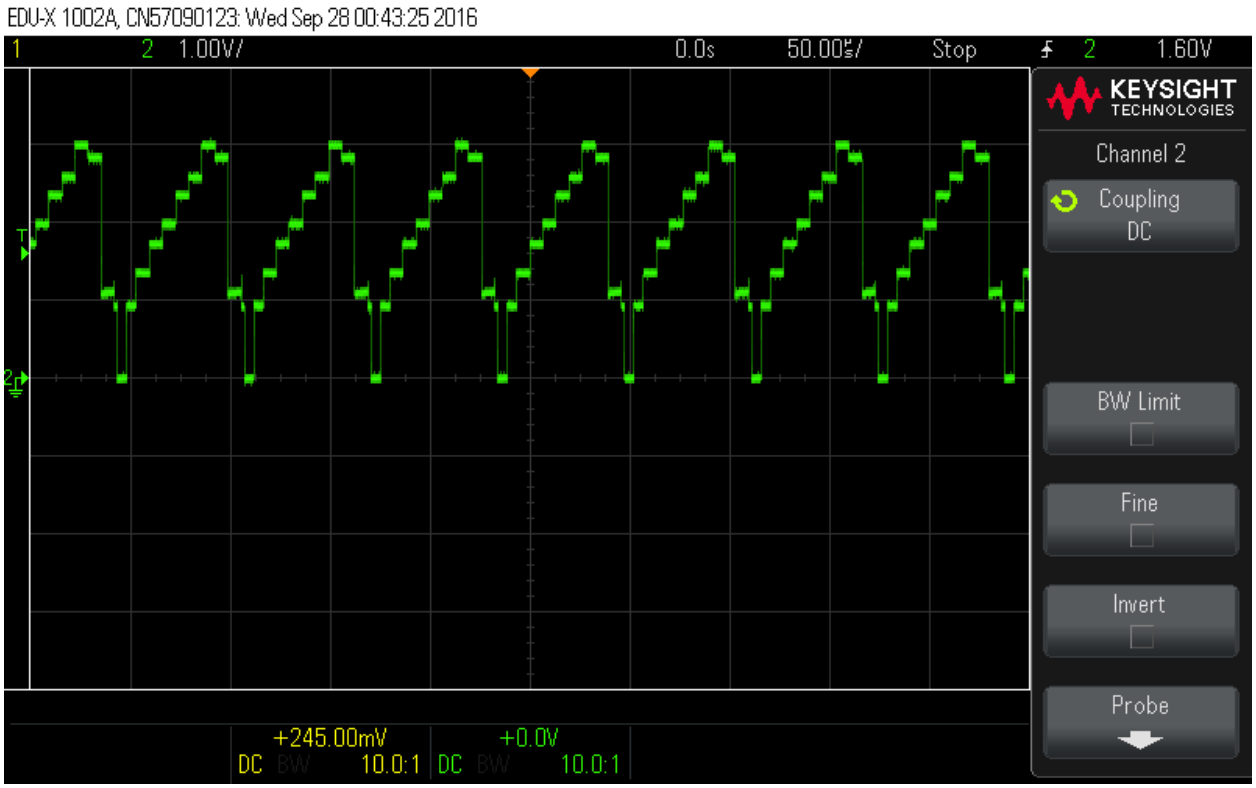
Fig: Vertical blanking and scan line signal



The figure above shows the measurement of the pulse length which verifies with the timing specification of the NTSC vertical blanking.



The figure above shows the timing measurement which verifies the duration for which the output is held to 0 volts during the vertical sync signal.



The figure above shows the measurement of scanline output.

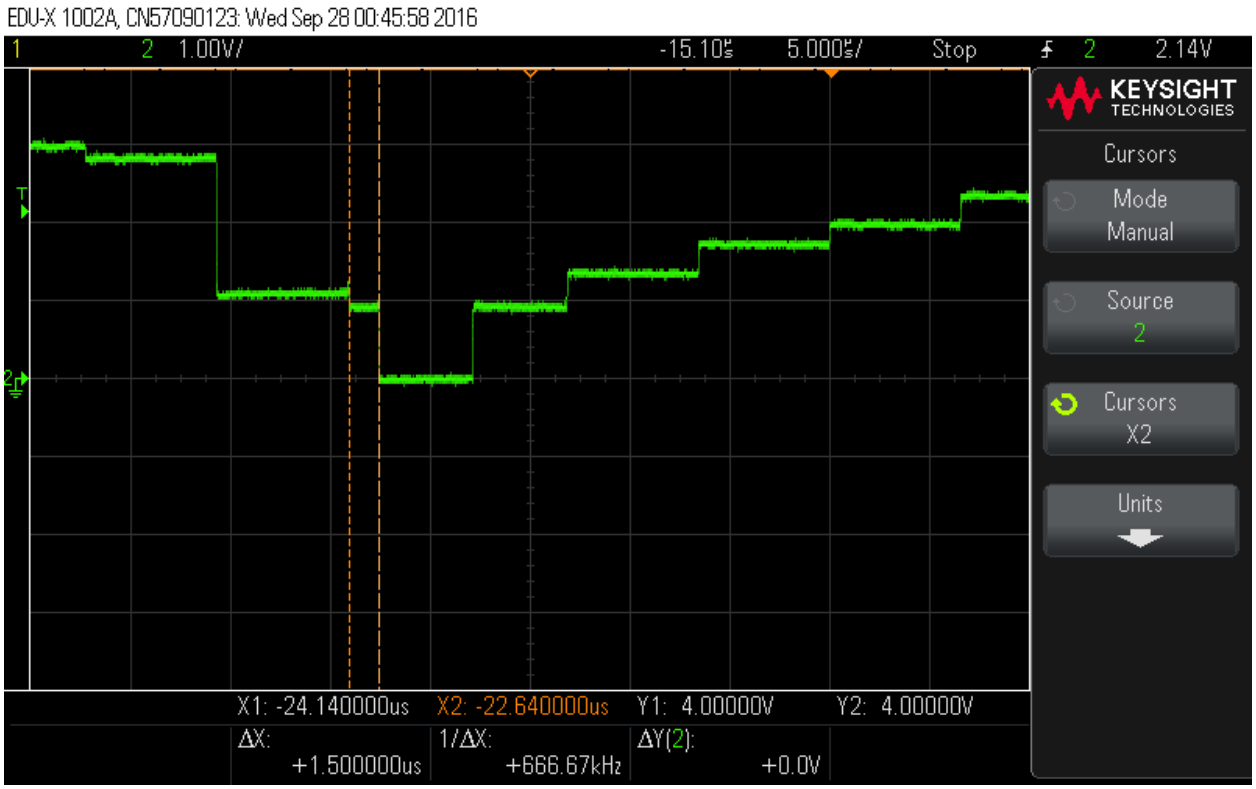
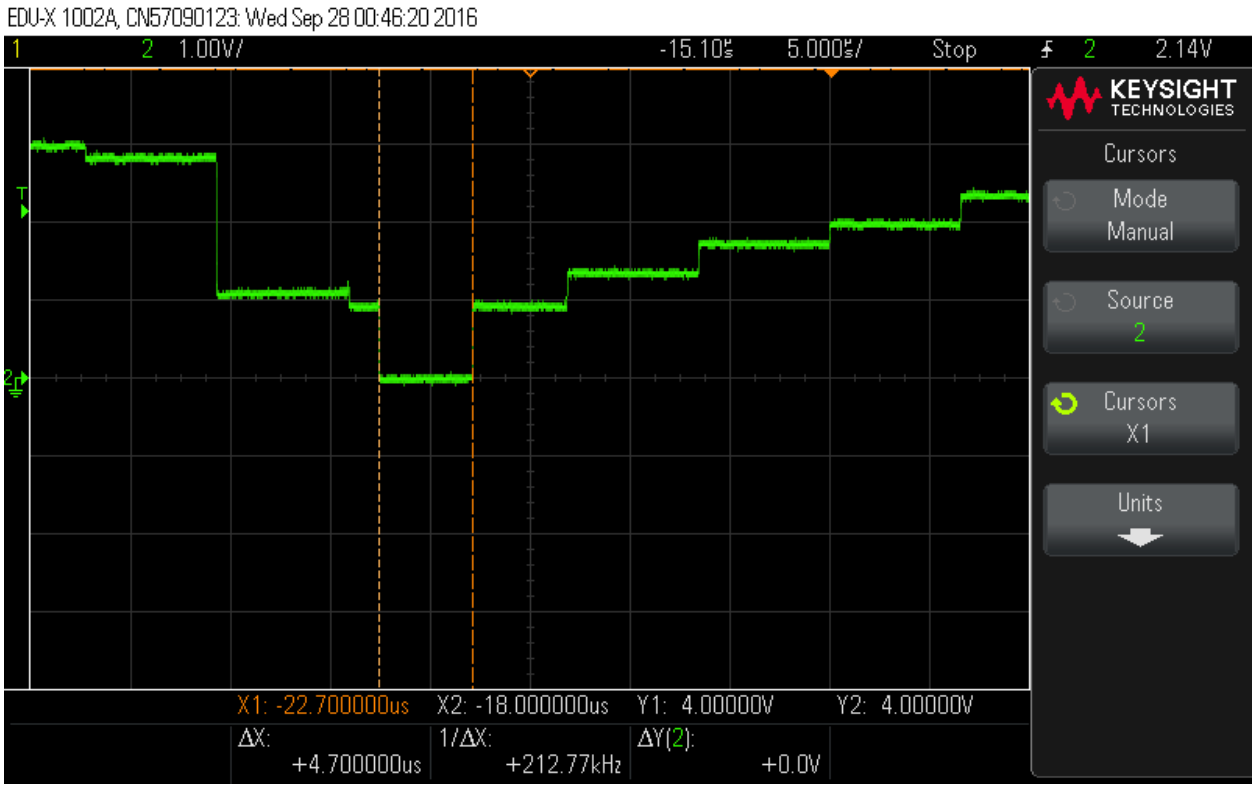


Figure above shows the measurement which verifies the front porch timing specification.



The figure above shows the measurement which verifies the timing specification of the sync_tiip.