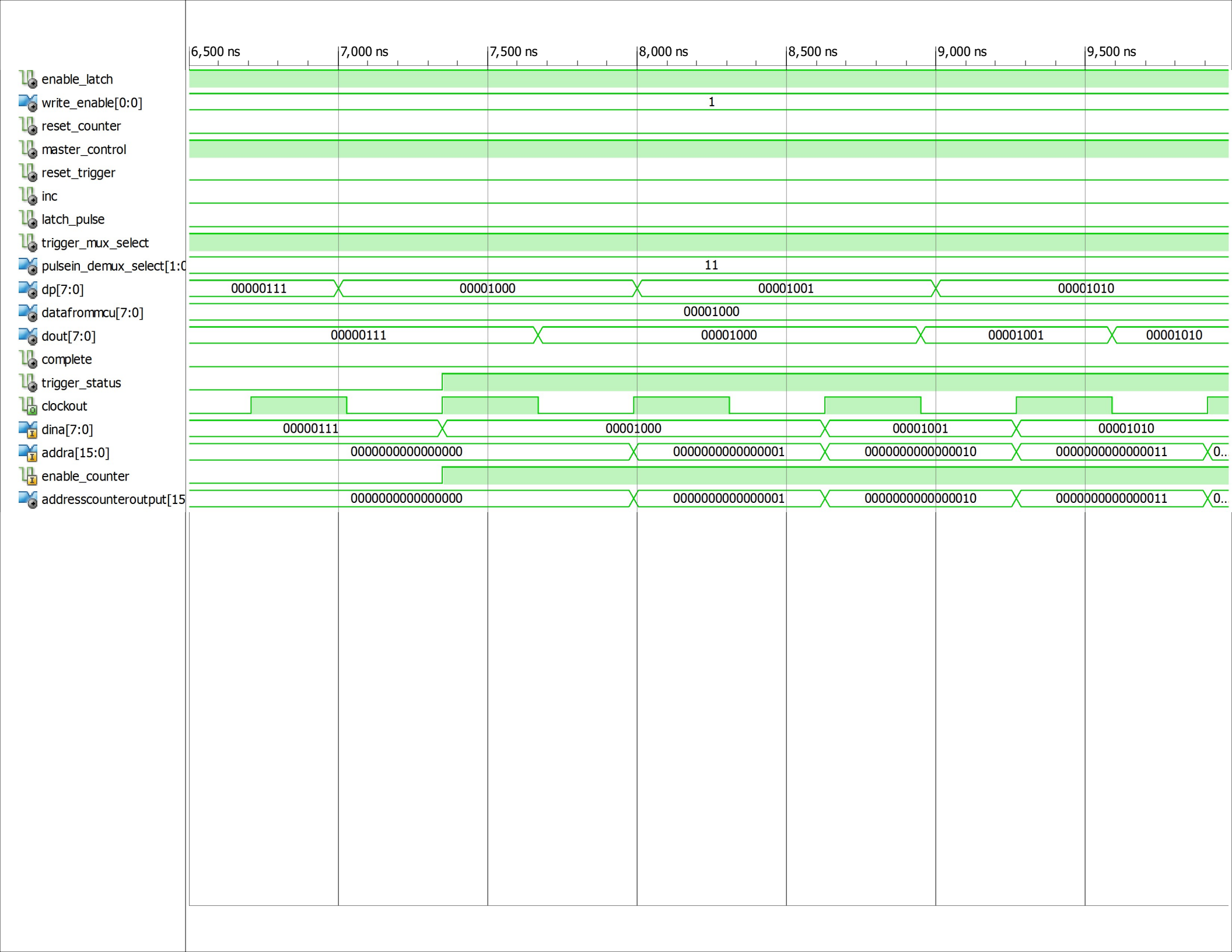
6,500 ns
7,000 ns
7,500 ns
8,000 ns
8,500 ns
9,000 ns
9,500 ns
enable_latch
write_enable[0:0]
1
reset_counter
master_control
reset_trigger
inc
latch_pulse
trigger_mux_select
pulsein_demux_select[1:0]
11
dp[7:0]
00000111
00001000
00001001
00001010
datafrommcu[7:0]
00001000
dout[7:0]
00000111
00001000
00001001
00001010
complete
trigger_status
clockout
dina[7:0]
00000111
00001000
00001001
00001010
addra[15:0]
0000000000000000
0000000000000001
0000000000000010
0000000000000011
enable_counter
addresscounteroutput[15
0000000000000000
0000000000000001
0000000000000010
0000000000000011