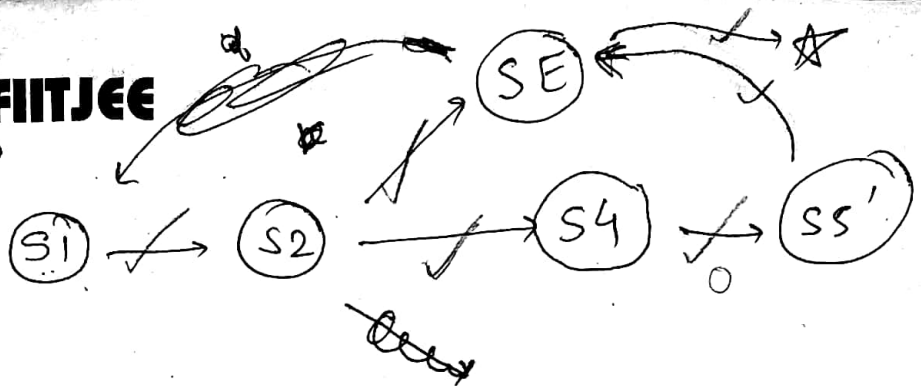
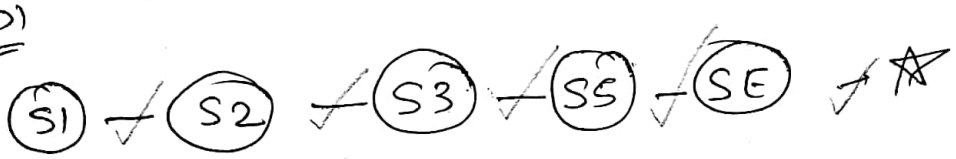
ADD



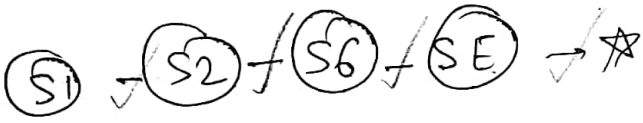
ADD, ADC, NDU, ADI, ND2, NDC

Summing

ADI

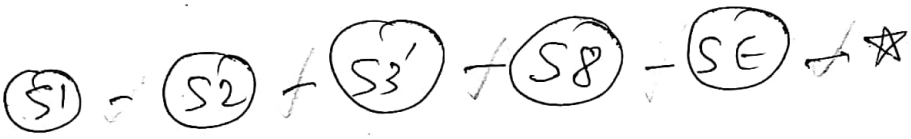


CMI



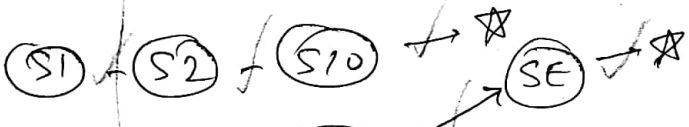
LW

SW

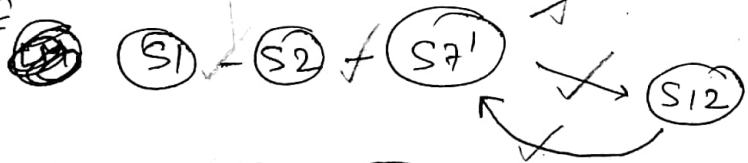


JAL

JLR

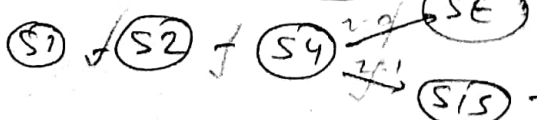


LM



SM

BEQ



S1	𝍸 𝍸	00000
S2	𝍸 𝍸	
S3	I	
S3'	II	
S4	II	
S5'	I	
S5	I	
S6	I	
S8	I	
SE	𝍸 III	
S7	I	
S2	I	
S9	I	
S10	I	
S7'	I	
S12	I	
S13	I	
S14	I	
S15	I	

ADD

FIITJEE

ADC

pc → mem_a, R7
pc → pc+1
mem_d/edb → ir

S1

↓

$ir_{9-10-11}$ → rf_a1
ir_{6-7-8} → rf_a2
rf_d1 → t1
rf_d2 → t2

S2

→ PE Nin

→ ir 0-7 Same with ADC, ADZ, NDZ, NDC, NDU.

↓

t_1 → alu_a
t_2 → alu_b
alu_out → t_1

S4

↓

ir_{3-4-5} → rf_a3
t_1 → rf_d3

S5'

↓

if R7 changed then R7 → PC
ow PC → R7

SE

$r_2 = r_7 + r_0$

$r_4 = r_3 + r_2$

R7

PC → R7

pc → pc+1

R7 ← PC

001 ADMod

	Inv	C use	Z use	C mod	Z mod	ALU	Flags
000	ADD					Add	C Z
100	ADD	X	X	X		Add	—
011	SUB	X	X	X		NAND	Z
010	NAND	X	X	X	0	SUB	Z

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

S2 Add Z

expand pc → pc+1

alu: d == alu b/d

FIITJEE

NDU

rf-a1 { ir 9-10-11 — S2
ir 6-7-8 — S10
PE out — S13

rf-a2 { ir 6-7-8 — S2

-a3 { ir 3-4-5 — S5'
ir 6-7-8 — S5
ir 9-10-11
PE out — S6 S9 S10 S2 S12

-d3 { t1 — S5 S5' ~~S12~~ #
SE9 — S6
R7 ⇒ S9 S10
t2 ⇒ S2 S12 #

Done

-a { PC — S1 S15 S9
t1 — S3 S4 S14 S12 #
t2
+0 — S3' S12 #
S2

-b { +1 — S1 S12 S14
SE6 — S3 S3' S15
t2 — S4 S2
SE9 — S9.
~~+0 — S2~~

rf-d1 { PC ← R7 when

rf-d3

PC { ~~PC+1 (incrementer) S1~~
rf-d1 — S10.
alu out — S9. S15. S1

R7 { ~~PC~~
rf-d1 — ~~S1~~ S10.
alu out — S9. ~~S1~~ S15.
PC — S1

jab bhi R7 main change aata toh same connection PC ke saath bhi hai, so no need for internal connection.

5 instructions

Done

t1 { rf-d1 — S2
alu-out — S3 S4 S14 S12 #
~~mem-d~~ — S7' #

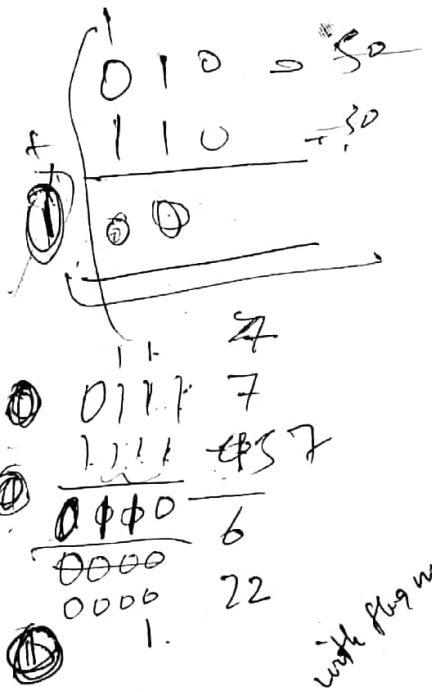
t2 { rf-d2 — S2
alu out — S3' ~~S12~~ #
mem-d — S7 S7' #
rf-d1 — S13

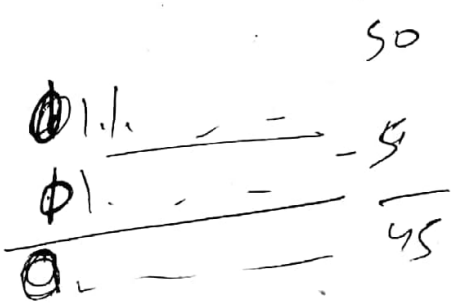
Rf-d3 → PC if Rf-a3=="111"

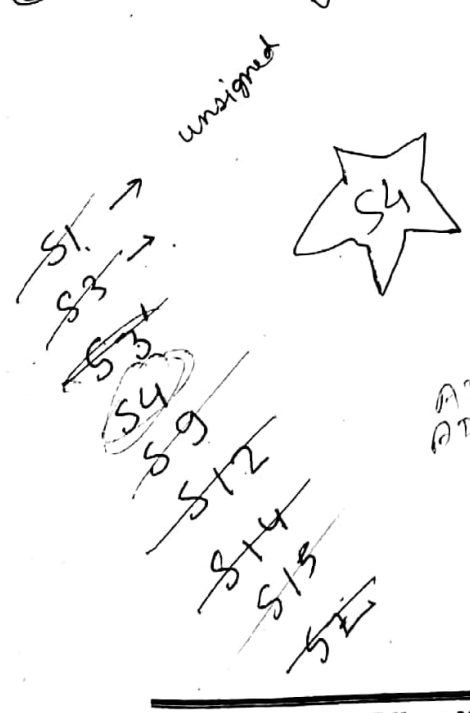
NDC

FIITJEE

NDZ







unsigned with flag mod } Add-neutals

unsigned with no flag mod

S1, S9, S15, S3, S12, S14

Signed ADD with both mod

S3, S4*

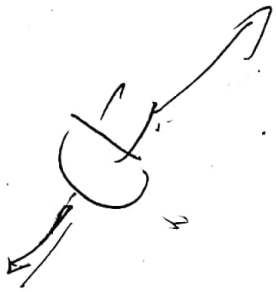
Signed ADD with only zero mod

S2

AND with zero

S4*

ADI



pc → mem_a
pc → pc + 1
mem_d/edb → ir

S1

↓

$ir_{9-10-11}$ → rf_a1
ir_{6-7-8} → rf_a2 → Useless
rf_d1 → t1
rf_d2 → t2 → Useless.

S2

↓

t1 → alu_a
ir_{0-5} → SE6 → alu_b
alu_out → t1

S3

↓

ir_{6-7-8} → rf_a3
t1 → rf_d3

S5

↓

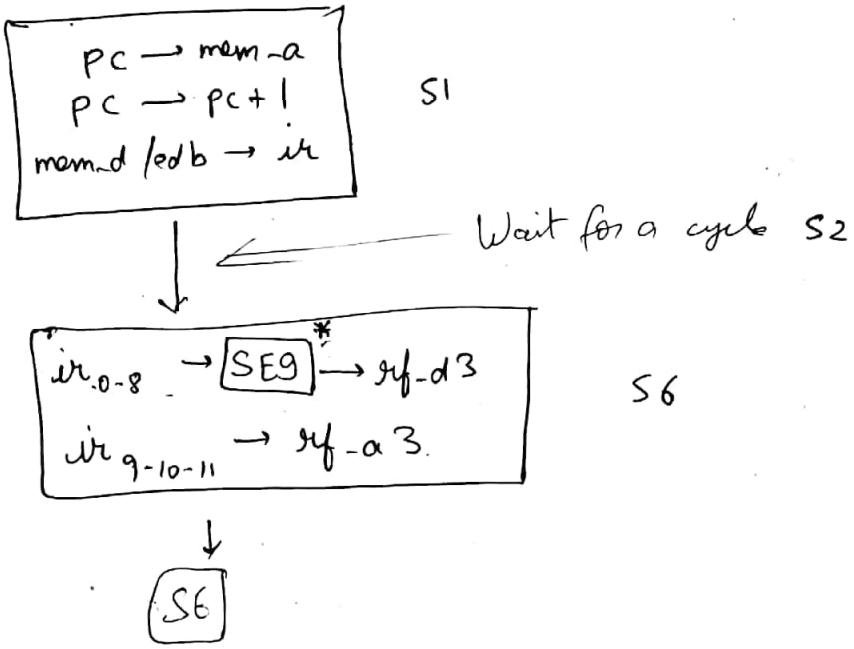
SE

x	y	z	
alu_a	alu_b	ans	C
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$\bar{x}\bar{y}z$

$\bar{x}\bar{y}z + xy\bar{z}$

LHI



LW

pc → mem_a
pc → pc + 1
mem_d/edb → ir

S1

↓

$ir_{9-10-11}$ → rf_a1 → Useless
ir_{6-7-8} → rf_a2
rf_d1 → t1 → Useless
rf_d2 → t2

S2.

↓

ir_{0-5} → SE 6 → alu_a
t2 → alu_b
alu_out → t2

S3'

↓

~~t2~~ t2 → Mem_a → WR = 0
mem_d → ~~rf_d3~~, ~~t2~~
~~$ir_{9-10-11}$ → rf_a3~~

S7

↓

Parallel
t2 → alu_a
t0 → alu_b
} To mod Zero flag

t2 → rf_d3
$ir_{9-10-11}$ → rf_a3

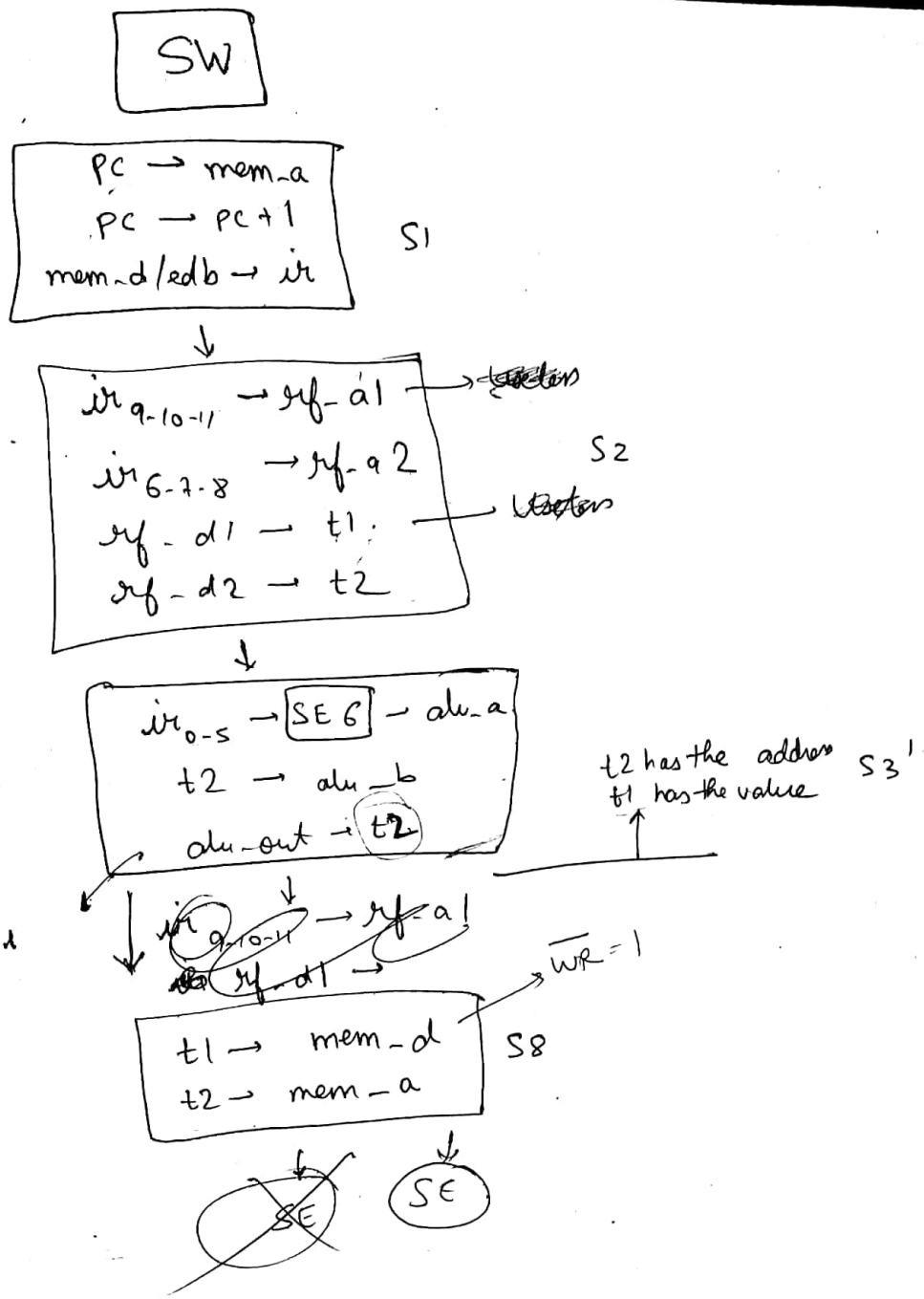
S2

↓

SE

ir

SW



FIITJEE

JAL

pc → mem_a, t1

R7

pc → mem_a, t1, R7

pc → pc + 1

mem_d/edb → ir

S1

S2

SB

Blank

S2

isko data

R7 → rf_d3

ir 9-10-11 → rf_a3

S9.

ir 0-8 → SE9 → alu_a

pc → alu_b

alu_out → pc, R7

JLR

PC → mem_a, R7.
PC → PC+1 ← Useless S1
mem_d/edb → ir

↓ ← Blank S2.

ir_{6-7-8} → rf_a1
R7 → rf_d3
$ir_{9-10-11}$ → rf_a3
rf_d1 → PC, R7
S10

~~SE~~

———— × ————

$ir_{9-10-11}$ → rf_a2.
rf_d2 → t_2
ir_{0-7} → PEin
S11

t_1 → rf_d3
PEout → rf_a3
t_2 → alu_a
t_1 → alu_b
alu_out → t_2
if (PE==0) {S7}
else (SE)
S12.

PEout → rf_a1
rf_a1 → t_1
S13.

t_1 → mem_d.
t_2 → mem_a, alu_a
t_1 → alu_b.
alu_out → t_2
if (PE==0) S13
else SE
S14

PC → alu_a.
ir_{0-5} → SE6 → alu_b
alu_out → PC
S15.

FIITJEE

LM

Update all S2

Pc → mem-a, R7

Pc → pc+1

mem-d/edb → ir

S1

ir 9-10-11 → rf-a1

ir 6-7-8 → rf-a2

rf-d2 → t1

rf-d1 → t2

ir 0-7 → PEin

S2

S11 (can be merged with S2)

ir 9-10-11 → rf-a1

ir 6-7-8 → rf-a2

rf-d1 → t1

rf-d2 → t2

ir 0-7 → PE-in

S2.

t1 → mem-a

mem-d → t1

S7'

if PEO != 0 go to S12

else SE

t2 → rf-d3

PEout → rf-a3

t1 → alu-a

t2 + 1 → alu-b

aluout → t2

if (PEO == 0) {S7'}

else {State SE}.

S12

Input to PE → PEO

PEO becomes 1 when all are 0

S7'

t1 → mem-a

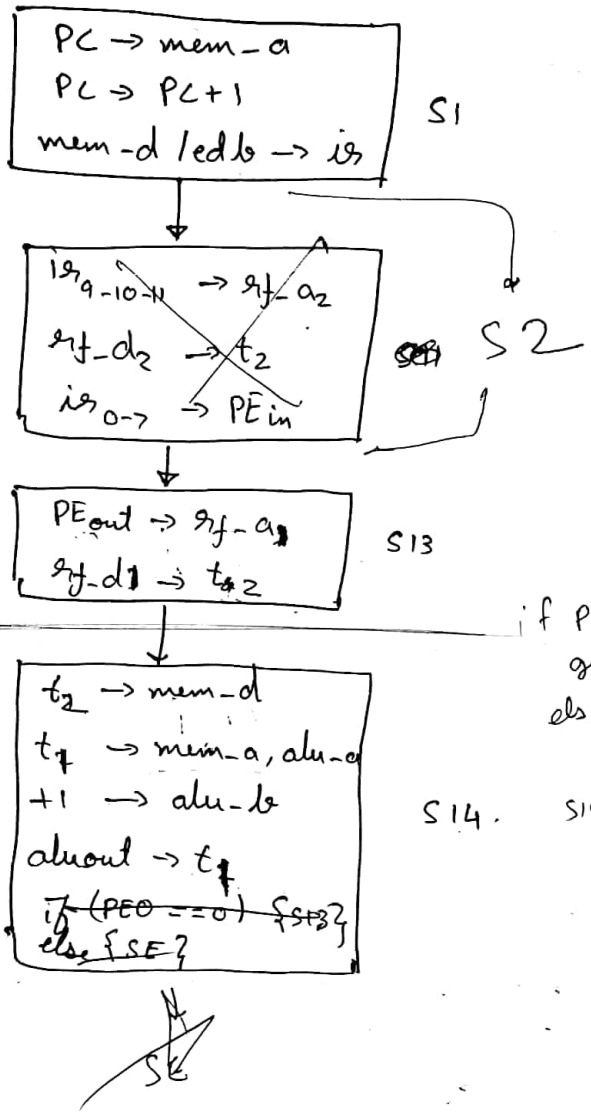
mem-d → t2

if PEO == 1 go to S6

else S12

S12 → S7'

SM



if PEO == 1
go to SE
else goto S14

S14. S14 → S13.

• PEO
write to zero.

r_1, r_2

r_a → memory add

SM 101 00101000
R5 R2

SM r_a, 1011
$r_0 r_1 r_2 r_3$

$[r_a]$

$[R_5] = R_2$

$t_2 = R_2$.

RA 0xAH12

$r_1 = [R_5]$

$[R_5] + ,$

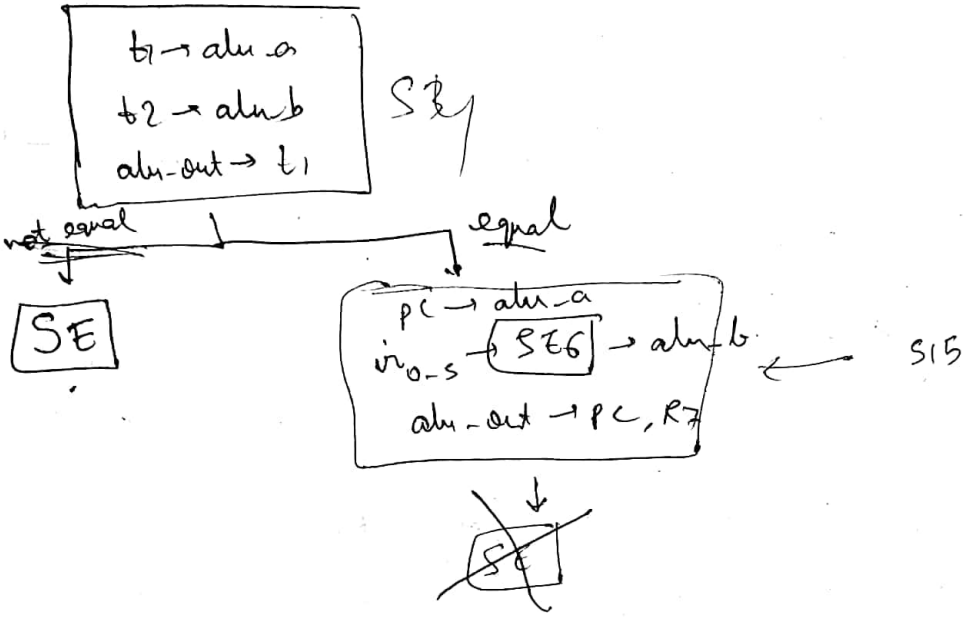
BEQ

S_1

↓

S2

↓



(1) ir_{6-7-8}
(1) ir_{3-4-5}
(1) $ir_{9-10-11}$

$ir_{9-10-11}$ →

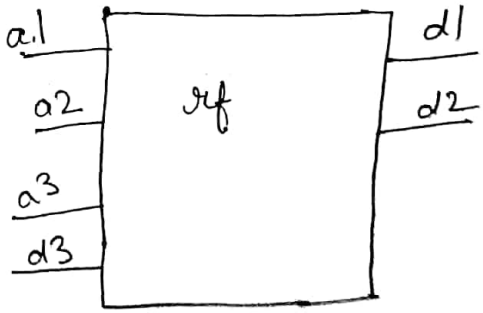
$\left.\begin{matrix}\\\\\end{matrix}\right\}$ $rf\text{-}a_3$

(1) $ir_{9-10-11}$ →
(1) PE_{out} →
(1) ir_{6-7-8} →

$\left.\begin{matrix}\\\\\\\end{matrix}\right\}$ $rf\text{-}a_1$

(1) ir_{6-7-8}

$\left.\begin{matrix}\\\end{matrix}\right\}$ $rf\text{-}a_2$



S1

PC → mem-a, R7

PC → PC+1

mem-d → ir

S2

$ir_{9-10-11}$ → rf-a1

ir_{6-7-8} → rf-a2

rf-d1 → t1

rf-d2 → t2

ir_{0-7} → PE in

S3

t1 → alu-a

ir_{0-5} → SE6 → alu-b

alu-out → t1

S3'

t2 → alu-b alu-a

ir_{0-5} → SE6 → alu-a alu-b

alu-out → t2

S4

t1 → alu-a

t2 → alu-b

alu-out → t1

S5

ir_{6-7-8} → rf-a3

t1 → rf-d3

S5'

ir_{3-4-5} → rf-a3'

t1 → rf-d3'

S6

ir_{0-8} → SE9 → rf-d3

$ir_{9-10-11}$ → rf-a3

S7

t2 → mem-a

mem-d → t2

S8

t1 → mem-d

t2 → mem-a

WE=1

S9

R7 → rf-d3

$ir_{9-10-11}$ → rf-a3

ir_{0-8} → SE9 → alu-a

PC → alu-b

alu-out → PC, R7

S10

ir_{6-7-8} → rf-a1

R7 → rf-d3

$ir_{9-10-11}$ → rf-a3

rf-d1 → PC, R7

S12

t2 → rf-d3 #

PE out → rf-a3

t1 → alu-a #

+1 → alu-b

alu-out → t1 #

S13

PE out → rf-a1

rf-d1 → t2

S14

t2 → mem-d

t1 → mem-a, alu-a

+1 → alu-b

alu-out → t1

S15

PC → alu-a

ir_{0-5} → SE6 → alu-b

alu-out → PC, R7

S7'

t1 → mem-a

mem-d → t2 #

S2

t2 → alu-a, alu-b

+0 → alu-b, alu-a

t2 → rf-d3

$ir_{9-10-11}$ → rf-a3

S1

PC → mem-a

PC → R7

PC → alu-a

+1 → alu-b

alu-out → PC

mem-d → ir

t1 S14 S7'

PC S1

mem-a ← t2 S2 S8

mem-d ← t1 S14