

# MIPS reference card

<b>add</b>	rd, rs, rt	Add	rd = rs + rt	R 0 / 20	<b>registers</b>											
<b>sub</b>	rd, rs, rt	Subtract	rd = rs - rt	R 0 / 22	\$0 \$zero											
<b>addi</b>	rt, rs, imm	Add Imm.	rt = rs + imm±	I 8	\$1 \$at											
<b>addu</b>	rd, rs, rt	Add Unsigned	rd = rs + rt	R 0 / 21	\$2-\$3 \$v0-\$v1											
<b>subu</b>	rd, rs, rt	Subtract Unsigned	rd = rs - rt	R 0 / 23	\$4-\$7 \$a0-\$a3											
<b>addiu</b>	rt, rs, imm	Add Imm. Unsigned	rt = rs + imm±	I 9	\$8-\$15 \$t0-\$t7											
<b>mult</b>	rs, rt	Multiply	{hi, lo} = rs * rt	R 0 / 18	\$16-\$23 \$s0-\$s7											
<b>div</b>	rs, rt	Divide	lo = rs / rt; hi = rs % rt	R 0 / 1a	\$24-\$25 \$t8-\$t9											
<b>multu</b>	rs, rt	Multiply Unsigned	{hi, lo} = rs * rt	R 0 / 19	\$26-\$27 \$k0-\$k1											
<b>divu</b>	rs, rt	Divide Unsigned	lo = rs / rt; hi = rs % rt	R 0 / 1b	\$28 \$gp											
<b>mfhi</b>	rd	Move From Hi	rd = hi	R 0 / 10	\$29 \$sp											
<b>mflo</b>	rd	Move From Lo	rd = lo	R 0 / 12	\$30 \$fp											
<b>and</b>	rd, rs, rt	And	rd = rs & rt	R 0 / 24	\$31 \$ra											
<b>or</b>	rd, rs, rt	Or	rd = rs   rt	R 0 / 25	hi —											
<b>nor</b>	rd, rs, rt	Nor	rd = ~(rs   rt)	R 0 / 27	lo —											
<b>xor</b>	rd, rs, rt	eXclusive Or	rd = rs ^ rt	R 0 / 26	PC —											
<b>andi</b>	rt, rs, imm	And Imm.	rt = rs & imm0	I c	c0 \$13 c0_cause											
<b>ori</b>	rt, rs, imm	Or Imm.	rt = rs   imm0	I d	c0 \$14 c0_epc											
<b>xori</b>	rt, rs, imm	eXclusive Or Imm.	rt = rs ^ imm0	I e												
<b>sll</b>	rd, rt, sh	Shift Left Logical	rd = rt << sh	R 0 / 0	<b>syscall codes</b>											
<b>srl</b>	rd, rt, sh	Shift Right Logical	rd = rt >> sh	R 0 / 2	<b>for MARS/SPIM</b>											
<b>sra</b>	rd, rt, sh	Shift Right Arithmetic	rd = rt >> sh	R 0 / 3	1 print integer											
<b>sllv</b>	rd, rt, rs	Shift Left Logical Variable	rd = rt << rs	R 0 / 4	2 print float											
<b>srlv</b>	rd, rt, rs	Shift Right Logical Variable	rd = rt >> rs	R 0 / 6	3 print double											
<b>srav</b>	rd, rt, rs	Shift Right Arithmetic Variable	rd = rt >> rs	R 0 / 7	4 print string											
<b>slt</b>	rd, rs, rt	Set if Less Than	rd = rs < rt ? 1 : 0	R 0 / 2a	5 read integer											
<b>sltu</b>	rd, rs, rt	Set if Less Than Unsigned	rd = rs < rt ? 1 : 0	R 0 / 2b	6 read float											
<b>slti</b>	rt, rs, imm	Set if Less Than Imm.	rt = rs < imm±? 1 : 0	I a	7 read double											
<b>sltiu</b>	rt, rs, imm	Set if Less Than Imm. Unsigned	rt = rs < imm±? 1 : 0	I b	8 read string											
<b>j</b>	addr	Jump	PC = PC&0xF0000000   (addr0<< 2)	J 2	9 sbrk/alloc. mem.											
<b>jal</b>	addr	Jump And Link	\$ra = PC + 8; PC = PC&0xF0000000   (addr0<< 2)	J 3	10 exit											
<b>jr</b>	rs	Jump Register	PC = rs	R 0 / 8	11 print character											
<b>jalr</b>	rs	Jump And Link Register	\$ra = PC + 8; PC = rs	R 0 / 9	12 read character											
<b>beq</b>	rt, rs, imm	Branch if Equal	if (rs == rt) PC += 4 + (imm±<< 2)	I 4	13 open file											
<b>bne</b>	rt, rs, imm	Branch if Not Equal	if (rs != rt) PC += 4 + (imm±<< 2)	I 5	14 read file											
<b>syscall</b>		System Call	c0_cause = 8 << 2; c0_epc = PC; PC = 0x80000080	R 0 / c	15 write to file											
<b>lui</b>	rt, imm	Load Upper Imm.	rt = imm << 16	I f	16 close file											
<b>lb</b>	rt, imm(rs)	Load Byte	rt = SignExt(M1[rs + imm±])	I 20												
<b>lbu</b>	rt, imm(rs)	Load Byte Unsigned	rt = M1[rs + imm±] & 0xFF	I 24	<b>exception causes</b>											
<b>lh</b>	rt, imm(rs)	Load Half	rt = SignExt(M2[rs + imm±])	I 21	0 interrupt											
<b>lhu</b>	rt, imm(rs)	Load Half Unsigned	rt = M2[rs + imm±] & 0xFFFF	I 25	1 TLB protection											
<b>lw</b>	rt, imm(rs)	Load Word	rt = M4[rs + imm±]	I 23	2 TLB miss L/F											
<b>sb</b>	rt, imm(rs)	Store Byte	M1[rs + imm±] = rt	I 28	3 TLB miss S											
<b>sh</b>	rt, imm(rs)	Store Half	M2[rs + imm±] = rt	I 29	4 bad address L/F											
<b>sw</b>	rt, imm(rs)	Store Word	M4[rs + imm±] = rt	I 2b	5 bad address S											
<b>ll</b>	rt, imm(rs)	Load Linked	rt = M4[rs + imm±]	I 30	6 bus error F											
<b>sc</b>	rt, imm(rs)	Store Conditional	M4[rs + imm±] = rt; rt = atomic ? 1 : 0	I 38	7 bus error L/S											
<b>pseudo-instructions</b>					8 syscall											
<b>bge</b>	rx, ry, imm	Branch if Greater or Equal	R <table><tr><td>6 bits</td><td>5 bits</td><td>5 bits</td><td>5 bits</td><td>5 bits</td><td>6 bits</td></tr><tr><td>op</td><td>rs</td><td>rt</td><td>rd</td><td>sh</td><td>func</td></tr></table>	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	op	rs	rt	rd	sh	func	9 break
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits											
op	rs	rt	rd	sh	func											
<b>bgt</b>	rx, ry, imm	Branch if Greater Than				a reserved instr.										
<b>ble</b>	rx, ry, imm	Branch if Less or Equal	I <table><tr><td>6 bits</td><td>5 bits</td><td>5 bits</td><td>16 bits</td></tr><tr><td>op</td><td>rs</td><td>rt</td><td>imm</td></tr></table>	6 bits	5 bits	5 bits	16 bits	op	rs	rt	imm			b coproc. unusable		
6 bits	5 bits	5 bits	16 bits													
op	rs	rt	imm													
<b>blt</b>	rx, ry, imm	Branch if Less Than				c arith. overflow										
<b>la</b>	rx, label	Load Address	J <table><tr><td>6 bits</td><td>26 bits</td></tr><tr><td>op</td><td>addr</td></tr></table>	6 bits	26 bits	op	addr			F: fetch instr.						
6 bits	26 bits															
op	addr															
<b>li</b>	rx, imm	Load Immediate				L: load data										
<b>move</b>	rx, ry	Move register				S: store data										
<b>nop</b>		No Operation														