Name: _____

# CIS 351 Sample M2 Problem

15 October 2025

## M2: Cache Mechanics

Consider a 512KB, 8-way set associative cache with 16 byte blocks.

(a) Show how 32-bit addresses are divided into offset, index, and tag fields. You must show your work.

(b) Compute the total size of this cache (including metadata). Assume pseudo-LRU replacement. Give your answer in bytes. Show your work.

(c) Sketch this cache.

Click here for solutions: `m2_sample_solutions.pdf`