Name: _____

CIS 351 Sample M3 Problem

15 October 2025

M3: Trace Cache Behavior

You have an 128KB, byte addressable, 2-way set associative cache with 16 byte blocks. This cache uses an LRU replacement policy. For the following sequence of addresses, show whether each is a hit or a miss. For each cache miss, tell which bytes were replaced.

Address	Tag	Index	H / M	Tags Replaced	Notes
0x12341110					Cold
0x12341113					Same block
0x12351113					Cold
0x12341113					
0x12361114					
0x12351113					
0x12361114					
0x12341110					
0x12361110					Same block
0x12351113					

Click here for solutions: `m3_sample_solutions.pdf`