CIS 351 Sample M2 Problem Solutions

Sun 19th Oct, 2025

M2: Cache Mechanics

Consider a 512KB, 8-way set associative cache with 16 byte blocks.

(a) Show how 32-bit addresses are divided into offset, index, and tag fields. You must show your work.

Tag, Index, Offset $\longrightarrow$ 16 – 12 – 4

(b) Compute the total size of this cache (including metadata). Assume pseudo-LRU replacement. Give your answer in bytes. Show your work.

The columns after "Correct" are so I can check if the only mistake is forgotten valid and/or LRU bits.

	Correct	No valid	No LRU	No LRU/No Valid
Bits / way	145	144	145	144
Bits / line	1167	1159	1160	1152
Bits / cache	4,780,032	4,747,264	4,751,360	4,718,592
Bytes / cache	597,504.0	593,408.0	593,920.0	589,824.0
KB / cache	583.5KB	579.5KB	580.0KB	576.0KB

(c) Sketch this cache.