CIS 351 Sample ADD3 Problem Solutions

Thu 6th Jan, 2022

ADD4: Carry Select Adder

(a) Sketch the top-level of a 16-bit carry-select adder. I'll check these individually.

(b) Assume that the carry-select pattern is applied at only the top-level, and that the component 8-bit adders are standard ripple-carry adders. Fill in the blanks: The propagation delay of this carry select adder is _____ (more than, exactly, less than) _____ (give a fraction) that of a 16-bit ripple carry adder.

The delay will be *more than* one-half.

(c) Explain your choice of "more than", "exactly", or "less than" for the previous problem.

The 8-bit ripple carry adders will have a propagation delay of half that of a 16-bit ripple carry adder.[1] Those thee adders all run in parallel. After the ripple-carry adders complete, then the muxes must select the final output. These muxes make the total propagation delay slightly longer than half the running time of a 16-bit ripple-carry adder.