CIS 351 Sample SS3 Problem Solutions

Fri 31st Oct, 2025

SS3: Operation of Single Cycle CPU

Answer the questions below with respect to Figure 1.

(a) For each instruction below, list the value on the `RegDest` control wire. *Explain your reasoning.* (The explanation is the important part. Convince me you did more than memorize the table.) Use "X" for "Don't Care" where appropriate.

add	addi	lw	sw	beq	j
1	0	0	X	X	X

`sw`, `beq`, and `j` don't write to a register, so the output of this mux doesn't matter.

(b) What is the purpose of the value on wire `G`? Describe the information it contains when executing a `lw` instruction. (To be clear, I'm looking for the *purpose* of the information, not the specific value.). "This value is not used for this instruction" a valid choice.

This wire contains the number of the register where the loaded data is to be stored

(c) What is the purpose of the value on wire `J`? Describe the information it contains when executing a `j` instruction. (To be clear, I'm looking for the *purpose* of the information, not the specific value.). "This value is not used for this instruction" a valid choice.

This value is not used by the jump instruction. (The jump instruction does not use the ALU.)

(d) What is the width (in bits) of the wire labeled `J`? Explain your reasoning / how you know this.

Wire J is 32 bits wide. It is an input to the 32-bit ALU.

(e) Suppose wire `I` breaks and provides unreliable values. Which of the follwing instructions will continue to function correctly? Explain your reasoning. `add`, `addi`, `lw`, `sw`, `beq`, `j`

`beq` and `add` will break because they use data from two registers. The remaining operations will continue to work correctly because they either (a) send an immediate value to the ALU, or (b) do not use the ALU.

(f) Suppose component `R` breaks and provides unreliable values. Which of the follwing instructions will continue to function correctly? Explain your reasoning. `add`, `addi`, `lw`, `sw`, `beq`, `j`

`sw`, `beq`, and `j` will continue to work correctly. These instructions do not write to a register, so the output of this mux does not matter.

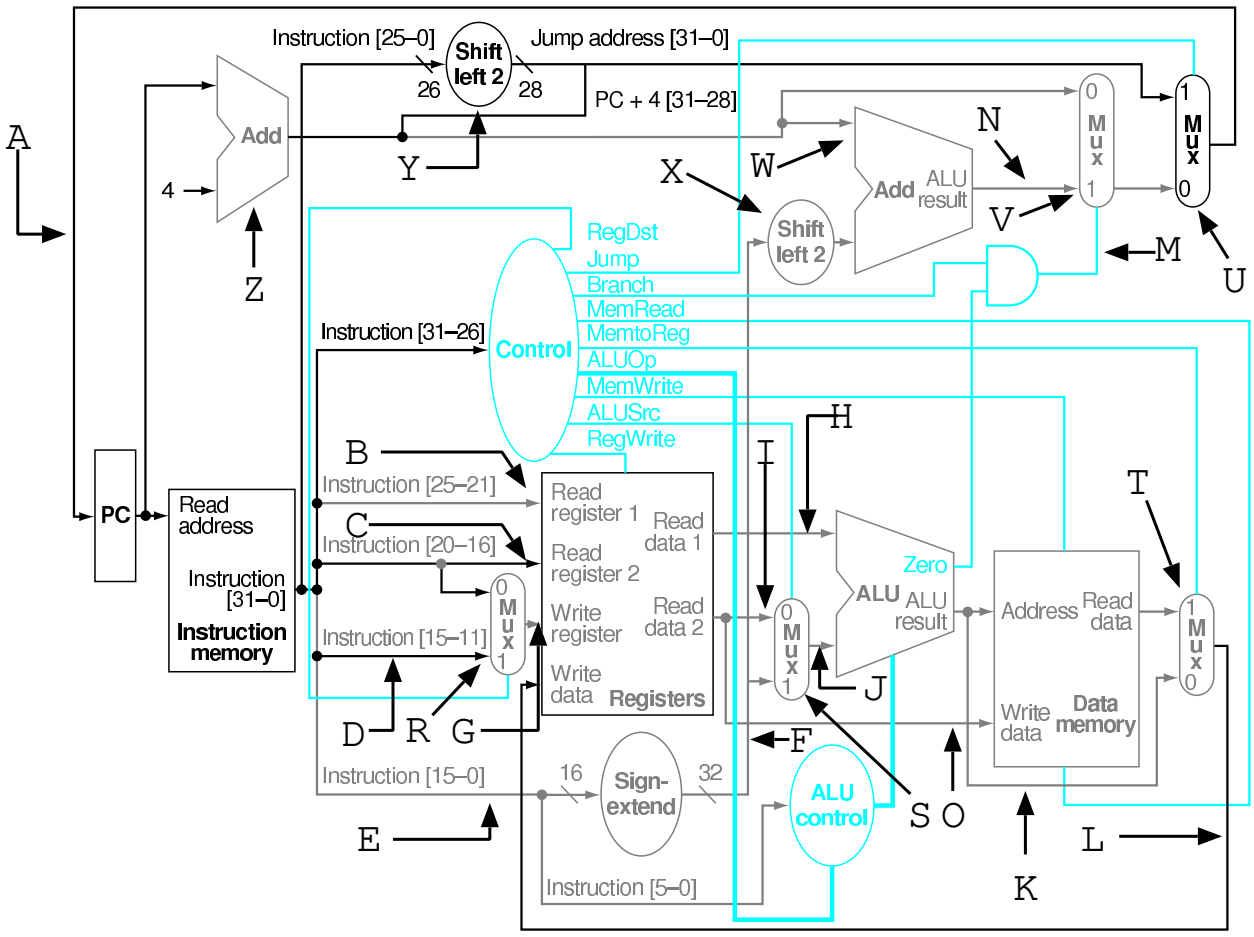

Figure 1: Single Cycle CPU with labeled points