

Name: \_\_\_\_\_

# CIS 351 Sample M4 Problem

15 October 2025

## M4: Effects of Cache Parameters

- (a) Suppose you have a cache configured such that the memory address is broken down into  $t$  tag bits,  $i$  index bits, and  $o$  offset bits. If you were to double the cache size without changing the block size or associativity, how would  $t$ ,  $i$ , and  $o$  change?
- (b) Explain your reasoning for each parameter above (index, offset, and tag).
- (c) How does increasing the cache size affect the number of Cold cache misses? Explain your reasoning.
- (d) How does increasing the cache size affect the number of Conflict misses? Explain your reasoning.

Click here for solutions: [m4\\_sample\\_solutions.pdf](#)