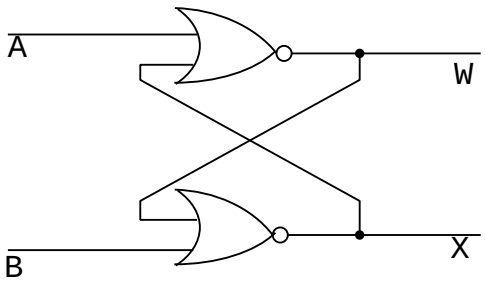
CIS 351 Sample SL1 Problem Solutions

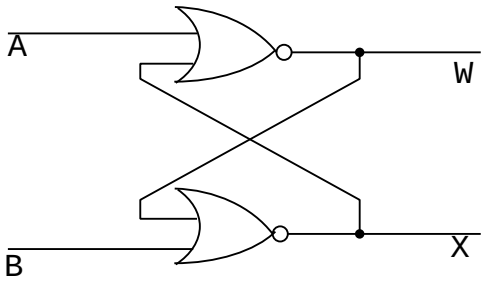
Thu 6th Jan, 2022

SL1: Latches

(a) Complete the characteristic table for the circuit shown below: Note, there is no clock pulse here. Your answers should show the states W and X after they have reached a steady state given A, B, and current value of W. (Remember to trace the circuit until it has reached a *steady state* — a state in which no further transitions will occur.)

A	B	W_{now}	X_{now}	W_{next}	X_{next}
0	0	0	0	rand	rand
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	rand	rand
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0





(Extra copy if you need more scratch space.) NOR latch

(b) The above circuit can be used as a latch (provided you avoid the inputs that lead to random state). What input combinations can be used for "set", "reset", and "hold"? (Hint #1: One or both of the inputs may be "active low". Hint #2: Don't assume that W and X should necessarily hold opposite values — that's why they aren't labeled W and $\bar{W}$.)

A = 0; B = 0 → "Hold"
A = 0; B = 1 → "Set"
A = 1; B = 0 → "Reset"
A = 1; B = 1 → "Don't Use"

(c) Explain how the circuit uses a feedback loop to "remember" the current state. Your explaination should, in part, trace the operation of the "hold" input.

(d) Construct a clocked D latch from the circuit above. Remember, the clocked D latch should set its state to the value of the D input whenever the clock is 1, and hold steady when the clock is 0.