CIS 351 Sample M3 Problem Solutions

Sun 19th Oct, 2025

M3: Trace Cache Behavior

You have an 128KB, byte addressable, 2-way set associative cache with 16 byte blocks. This cache uses an LRU replacement policy. For the following sequence of addresses, show whether each is a hit or a miss. For each cache miss, tell which bytes were replaced.

Offset: 4
Index: 12
Tag: 16

128KB = 2^{17} bytes.
Lines = $\frac{2^{17}}{2*16}$ = 4096. Thus, 12 index bits.
Tag = 32 - (index + offset) = 16.

Address	Tag	Index	H / M	Tags Replaced	Notes
0x12341110	1234	111	M		Cold
0x12341113	1234	111	H		Same block
0x12351113	1235	111	M		Cold
0x12341113	1234	111	H		
0x12361114	1236	111	M	0x1235	
0x12351113	1235	111	M	0x1234	
0x12361114	1236	111	H		
0x12341110	1234	111	M	0x1235	
0x12361110	1236	111	H		Same block
0x12351113	1235	111	M	0x1234	