CIS 351 Sample SS5 Problem Solutions

Fri 31st Oct, 2025

SS5: Single Cycle Design

It would be difficult to add a `swap_register` instruction to the MIPS CPU (i.e, an instruction that takes two registers and swaps their contents). What would be the main difficulty in adding this instruction?

Such an instruction would need to be able to write to two registers at once. The CPU in the book can only write to one register at a time.