CIS 351 Sample M4 Problem Solutions

Sun 19th Oct, 2025

M4: Effects of Cache Parameters

(a) Suppose you have a cache configured such that the memory address is broken down into t tag bits, i index bits, and o offset bits. If you were to double the cache size without changing the block size or associativity, how would t, i, and o change?

(b) Explain your reasoning for each parameter above (index, offset, and tag).

(c) How does increasing the cache size affect the number of Cold cache misses? Explain your reasoning.

> Cold cache misses are misses caused by simply not having loaded the data before. Changing the cache size doesn't affect how/when bytes are loaded for the first time.

(d) How does increasing the cache size affect the number of Conflict misses? Explain your reasoning.

> Conflict misses are caused when two different bytes are mapped to the same cache line. Therefore, one of them is kicked out — even if there is room elsewhere in the cache.
>
> Doubling the cache size will reduce the probability of a conflict miss because fewer bytes in Memory will be mapped to each line in the cache (because there are more cache lines.)