# Control Wires Solutions

March 2, 2016

Fill out the table below showing how each control wire should be set. Mark `X` for "don't care", if it doesn't matter how the control wire is set. For `ALUop`, just write an operation instead of a number (e.g, "add", "sub", etc.)

Use this table with diagrams from the Patterson and Hennessey text:

| Control Wire | `add` | `addi` | `j` | `beq` | `lw` | `sw` |
|---|---|---|---|---|---|---|
| RegDest | 1 | 0 | X | X | 0 | 0 |
| Jump | 0 | 0 | 1 | 0 | 0 | 0 |
| Branch | 0 | 0 | 0 | 1 | 0 | 0 |
| MemRead | 0 | 0 | 0 | 0 | 1 | 0 |
| MemToReg | 0 | 0 | X | X | 1 | X |
| ALUop | "add" | "add" | X | "sub" | "add" | "add" |
| MemWrite | 0 | 0 | 0 | 0 | 0 | 1 |
| ALUSrc | 0 | 1 | X | 0 | 1 | 1 |
| RegWrite | 1 | 1 | 0 | 0 | 1 | 0 |

Use this table with diagrams from the Harris and Harris text:

| Control Wire | `add` | `addi` | `j` | `beq` | `lw` | `sw` |
|---|---|---|---|---|---|---|
| Jump | 0 | 0 | 1 | 0 | 0 | 0 |
| MemToReg | 0 | 0 | X | X | 1 | X |
| MemWrite | 0 | 0 | 0 | 0 | 0 | 1 |
| Branch | 0 | 0 | 0 | 1 | 0 | 0 |
| ALUControl | | | X | "sub" | "add" | "add" |
| ALUSrc | 0 | 1 | X | 0 | 1 | 1 |
| RegDest | 1 | 0 | X | X | 0 | 0 |
| RegWrite | 1 | 1 | 0 | 0 | 1 | 0 |

Design a circuit to compute the value of the `jump` control wire

Design a circuit to compute the value of the `branch` control wire

Design a circuit to compute the value of the `regWrite` control wire