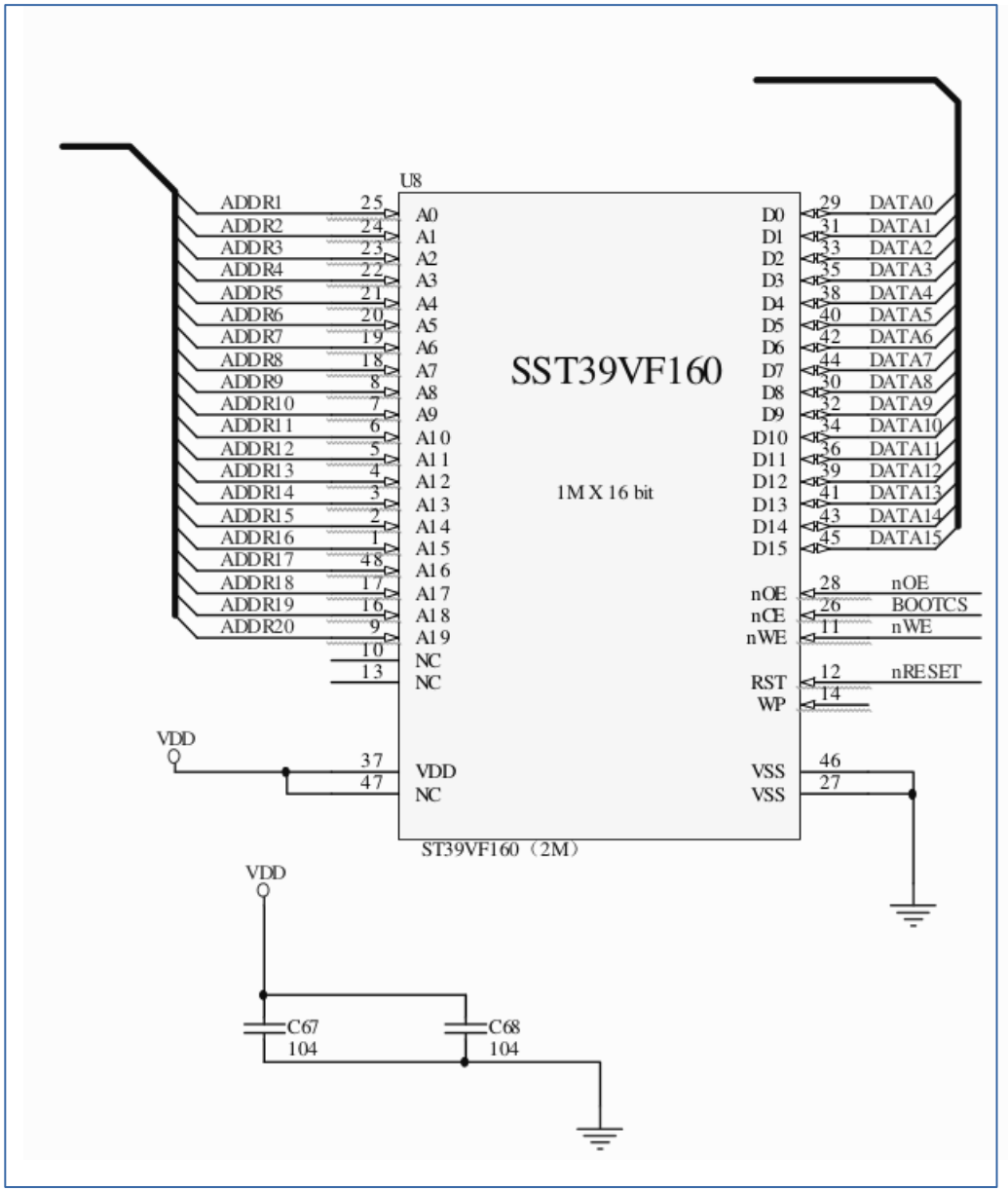
ROM Hardware Interface Design Example

1

Address Bus

Example:
Find address bus A[19:0] linked to the density of the ROM memory



2

Data Bus (16 bits in this design)

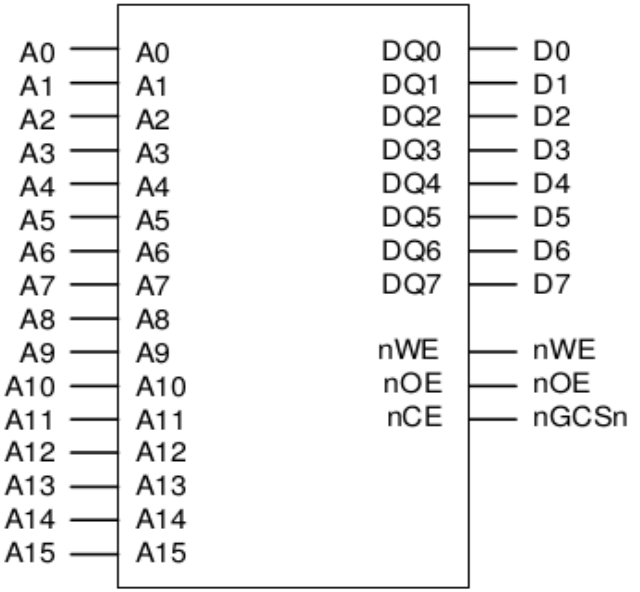
2 Bytes per memory cycle

3

Control signals:
nOE,
nWE,
nCS (Boot select)

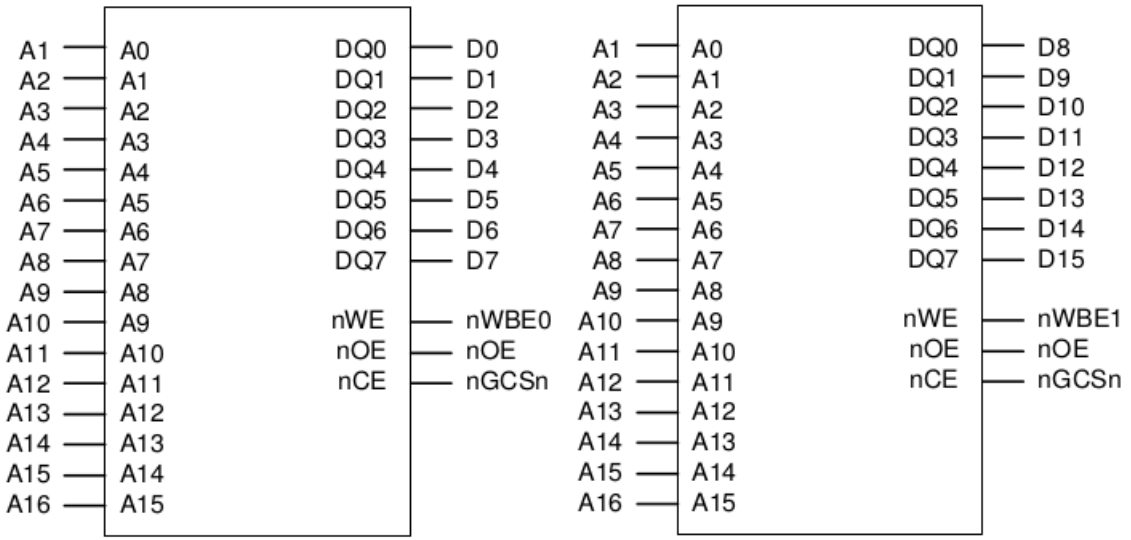
Memory Interface 1 and 2 Banks of 8-bit ROM

Figure 5-4. Memory Interface with 8-bit ROM



Reference: CPU
s3c2440a_um_rev014_040712.pdf

Figure 5-5. Memory Interface with 8-bit ROM x 2



Memory Interface 4 Banks of 8-bit ROM

Reference: CPU s3c2440a_um_rev014_040712.pdf

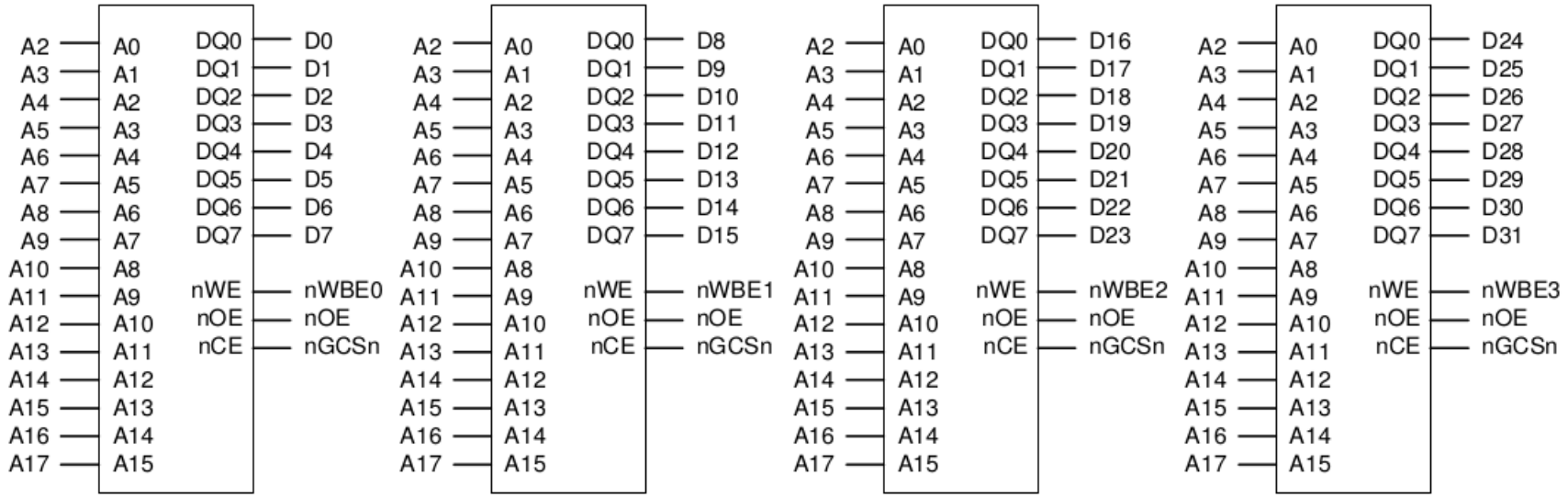


Figure 5-6. Memory Interface with 8-bit ROM x 4