

San José State University
College of Engineering/Computer Engineering
Department
CMPE127 Microprocessor, Section 1, F2017

Professor Hua Harry Li
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Class Meeting: MW 1:30 – 2:20 PM
Office Hours: Tuesday 6:00 – 7:30 PM

Lecture: MW 1:30-2:20 PM, Engr. 337
Lab: ENG 268

Prerequisites

CmpE 125 (with a “C” or better). Students who do not provide documentation of having satisfied the class prerequisite requirements by the second class meeting will be dropped from the class.

Faculty Web Page and MYSJSU Messaging (Optional)

Copies of the course materials such as the syllabus, major assignment handouts, etc. are posted on SJSU CANVAS and also on github.

Course Description

Microprocessor architecture and assembly language. Design of peripheral blocks and their interfaces to the microprocessor. Design projects using standard integrated circuit packages.

Course Goals and Student Learning Objectives

1. Formulate and solve engineering design problems by engaging experiments and implementation of microprocessor systems.
2. Understand and analyze system architecture, CPU organization and its basic operating principles.
3. Design and implement debugging mechanism to trace CPU operation.
4. Design and build bus systems (data vs. address bus, as well as control bus) and their buffers and transceivers.
5. Conduct system performance evaluation, calculate timing requirement for the Microprocessor System.
6. Understand interrupt techniques and implement I/O interface design.

7. Generate formal technical specifications, formal report to document the engineering design and communicate with others effectively.

Course Content Learning Outcomes

Upon successful completion of this course, students will be able to:

1. Understand organization and block diagrams of the Microprocessor System, design and implementation of debugging techniques via serial interface(UART);
2. To be able to analyze sub-systems, e.g., Timing and Reset Circuit, Bus Systems and Buffers/Transceivers, as well as memory interface design. Lab 1 Assignment.
3. Design and implement hardware for CPU memory controller interface to incorporate signals (nCS, nBLS, nOE, nWE etc.), and for data bus as well as address bus in memory interface.
4. Build ROM/FLASH memory interface design.
5. Understand CPU Architecture Theory, Von Neumann Architecture.
6. Understand CPU interface to peripheral controllers.
7. Understand interrupt techniques, utilization of interrupt technique for Wireless IrDA communications.
8. Design inter-processor communications via SPI, IIC interface.

Required Texts/Readings

Textbook

- Reference: ARM7TDMI data sheets and on-line web materials.
- Professor Li's handout materials;
- Datasheets, lab design reference materials will be posted in yahoo group, <http://groups.yahoo.com/group/CMPE127Microprocessor-HarryLi/>

Other Readings

- The reference material for ARM CPU hardware features, application notes, class handouts and lab assignments and reports, please see Professor Li's lecture material at <http://groups.yahoo.com/group/CMPE127Microprocessor-HarryLi/>

Other equipment / material requirements

32Bit RISC Prototype/Development Board.

Library Liaison (Optional)

N/A

Classroom Protocol

Participation and attendance are required, no late arrival times please. No cell phone use in class.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. [Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html](http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html). [Information about late drop is available at http://www.sjsu.edu/sac/advising/latedrops/policy/](http://www.sjsu.edu/sac/advising/latedrops/policy/). Students should be aware of the current deadlines and penalties for adding and dropping classes.

Assignments and Grading Policy

Weekly Quiz	10%
Laboratory	30%
Midterm Examination	25%
Final	35%

0 to 59 F
60 to 69 D
70 to 79 C
80 to 89 B
90 to 100 A

Policies on exams and late assignments

Quizzes, midterm and final are not postponed or retaken under any circumstances. The only exception is medical emergencies accompanied with doctor's report. The lab reports can be delayed under special circumstances. If you know you will delay a report for some unavoidable reason please see me as soon as possible. Extra credit may be available for optional project(s) upon discussion with the course instructor. 10% penalty is given for late project submission. C is the passing grade for the course. Final exam date is published by university schedule. No grade on participation. Attendance is not used as a criterion for grading according to Academic Policy F-69-24.

University Policies

Academic integrity

Students should know that the University's [Academic Integrity Policy is available at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf](http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf). Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for [Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html](http://www.sa.sjsu.edu/judicial_affairs/index.html).

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

Department Policies

All non-proctored report (or similar sized) assignments in courses where some of the final grade depends on prose writing will be submitted to turnitin.com.

Student Technology Resources (Optional)

Computer labs for student use are available in the Academic Success Center located on the 1st floor of Clark Hall and on the 2nd floor of the Student Union. Additional computer labs may be available in your department/college. Computers are also available in the Martin Luther King Library.

A wide variety of audio-visual equipment is available for student checkout from Media Services located in IRC 112. These items include digital and VHS camcorders, VHS and Beta video players, 16 mm, slide, overhead, DVD, CD, and audiotape players, sound systems, wireless microphones, projection screens and monitors.

Learning Assistance Resource Center (Optional)

The Learning Assistance Resource Center (LARC) is located in Room 600 in the Student Services Center. It is designed to assist students in the development of their full academic potential and to motivate them to become self-directed learners. The center provides support services, such as skills assessment, individual or group tutorials, subject advising, learning assistance, summer academic preparation and basic skills development. [The LARC website is located at http://www.sjsu.edu/larc/](http://www.sjsu.edu/larc/).

SJSU Writing Center (Optional)

The SJSU Writing Center is located in Room 126 in Clark Hall. It is staffed by professional instructors and upper-division or graduate-level writing specialists from each of the seven SJSU colleges. Our writing specialists have met a rigorous GPA requirement, and they are well trained to assist all students at all levels within all disciplines to become better writers. [The Writing Center website is located at http://www.sjsu.edu/writingcenter/about/staff/](http://www.sjsu.edu/writingcenter/about/staff/).

Peer Mentor Center (Optional)

The Peer Mentor Center is located on the 1st floor of Clark Hall in the Academic Success Center. The Peer Mentor Center is staffed with Peer Mentors who excel in helping students manage university life, tackling problems that range from academic challenges to interpersonal struggles. On the road to graduation, Peer Mentors are navigators, offering “roadside assistance” to peers who feel a bit lost or simply need help mapping out the locations of campus resources. Peer Mentor services are free and available on a drop –in basis, no reservation required. The Peer Mentor Center website is located at <http://www.sjsu.edu/muse/peermentor/> .

CMPE 127 Microprocessor Systems

The schedule is subject to change with fair notice in class.

Table 1 Course Schedule

Week	Date	Topics, Readings, Assignments, Deadlines
1	First Monday and Wednesday	Organizational Meeting and Introduction, Overview of a RISC Microprocessor System, CPU Architecture
2	Second Monday and Wednesday	System Organization and Design Prototype of a Microprocessor System, System Block Diagrams, GPIO design, CPU software IDE and tools
3	3 rd Monday and Wednesday	Analysis of GPIO functions, Timing diagrams, and design and implement GPIO interface
4	4 th Monday and Wednesday	CPU Peripheral Controllers, UART and RS232 interface design, MAX232 level shifter and design and implementation of debugging techniques based on serial interface
5	5 th Monday and Wednesday	Memory Map, Power-up Address, ROM memory unit and its 8-bit, 16-bit, 32-bit banks design implementation
6	6 th Monday and Wednesday	SPI Interface and SPI FLASH memory interface design
7	7 th Monday and Wednesday	Design and implementation of data logger based on SPI FLASH memory design
8	8 th Monday and Wednesday	Midterm Theory of CPU Architecture, Von Neumann Architecture and Intel 8086 CPU Architecture and Register File
9	9 th Monday and Wednesday	General Purpose Registers, Segment Registers, and Segmented Architecture. Bus Systems, Data Bus, Address Bus, Physical Address vs. Logic Address
10	10 th Monday and Wednesday	Interrupt techniques, case study: Intel CPU interrupt techniques, interrupt vector table, interrupt service routine (ISR) implementations
11	11 th Monday and Wednesday	Intel interrupt controller implementation, Intel 8259 architecture
12	12 th Monday and	ARM Interrupt Controller architecture and implementation

Week	Date	Topics, Readings, Assignments, Deadlines
	Wednesday	
13	13 th Monday and Wednesday	Interrupt and timer function, design and implementation of interrupt controller and timer function with IrDA interface, design and implementation of a sub-system to measure human response time
14	14 th Monday and Wednesday	Timing waveforms of modulated IrDA functions, Theoretical analysis of modulated IrDA interface with Fourier Transforms
15	15 th Monday and Wednesday	Power management, initialization and configuration of external RTC (DS1306).
16	16 th Monday and Wednesday	Power management subsystem design based on SPI interface with external RTC (DS1306) and utilization of external interrupt to CPU for system power management
Final Exam	17 th Monday and Wednesday	Comprehensive final exam