Bandwidth Mismatch and Its Correction in Time-Interleaved Analog-to-Digital Converters

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***Abstract*—The sample-and-hold amplifier in each channel of a time-interleaved analog-to-digital converter system has finite bandwidth, and these bandwidths may be mismatched. This paper analyzes the effect of such mismatches. Correction for bandwidth mismatch in the digital domain is described and demonstrated.**

***Index Terms*—Analog-digital conversion, bandwidth mismatch, finite-impulse response (FIR) digital filters, sample-and-hold circuit.**

I. Introduction

DUE to the rapid evolution of CMOS technologies, digital processing of signals has become an attractive option in mixed-signal systems. In such systems, the analog-to-digital converter (ADC) plays a key role by digitizing the analog input signal. When the input signal has a wide dynamic range, a high resolution is required, and the system throughput is often limited by the conversion rate of the ADC. Time interleaving of ADCs is an attractive way to increase the maximum conversion rate in a given technology [1]. A simplified block diagram of a time-interleaved ADC is shown in Fig. 1. It consists of M ADCs in parallel, with each ADC operating at a sampling rate of f_S/M. With M ADCs in parallel, the sampling rate is increased by a factor of M, giving an overall sampling rate of f_S. However, mismatches among the time-interleaved ADCs generate undesired spectral components and can significantly degrade the signal-to-noise-and-distortion ratio (SNDR) of the system. Thorough analysis of the effects of gain, offset, and sample-time errors among the time-interleaved ADC channels has been done [2]–[4]. Also, a first-order analysis of bandwidth mismatch has been published [4]. Recently, a general model that includes mismatch due to linear channel imperfections, and digital correction of such mismatches based on measured channel data, was presented [5].

To avoid problems that could be caused by sampling the input using an individual sample-and-hold amplifier (SHA) in each channel (i.e., sample-time errors and SHA bandwidth mismatches), some time-interleaved ADCs use a front-rank SHA to sample the input at the overall sampling rate [6]. In practice, the required speed in the front-rank SHA limits the number of channels that can be interleaved. Eliminating the front-rank SHA requires that the sampling is done by the time-interleaved SHAs, as shown in Fig. 1. Each interleaved SHA has finite bandwidth, and these bandwidths could be mismatched due to imperfect fabrication.

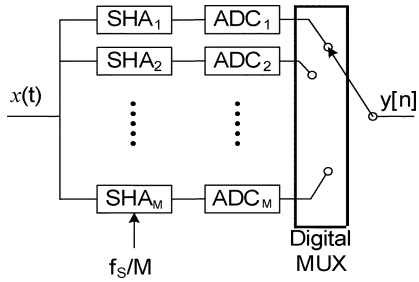

Fig. 1. Block diagram of the time-interleaved SHAs.

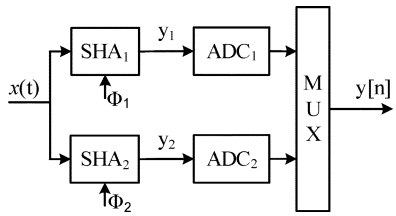

Fig. 2. Two-channel time-interleaved ADCs.

One way to avoid a limitation stemming from bandwidth mismatch among the channels is to increase the SHA bandwidths, so that they are much greater than the maximum input frequency to be digitized. However, this solution potentially reduces the maximum SNDR if the ADC input contains high-frequency noise. This paper extends previously published bandwidth mismatch analysis [4] and demonstrates digital correction for SHA bandwidth mismatch based on a first-order SHA model. This approach allows the SHA bandwidths to be no higher than in a single-channel ADC, avoiding extra noise exposure. The remainder of this paper is organized as follows: Section II analyzes the effects of bandwidth mismatch in a two-channel time-interleaved ADC system. Section III presents the proposed correction technique, and Section IV gives simulation results. Finally, Section V is the conclusion.

II. Bandwidth Mismatch Effects

For simplicity, consider a two-channel time-interleaved ADC system as shown in Fig. 2. Each channel contains an SHA and an ADC, sampling and digitizing the input signal at a rate $f_S/2$, which is half of the overall sampling rate f_S.

Fig. 3(a) shows a simple open-loop CMOS SHA circuit that can be used in Fig. 2. More complex CMOS SHAs are often used in practice [7]. When the clock Φ is high, the switch is on, and the SHA tracks the input signal $x(t)$. A simple model for this SHA in the sample (or track) mode is shown in Fig. 3(b).

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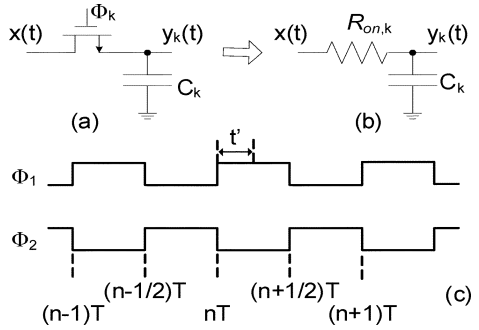

Fig. 3. (a) Simple SHA. (b) Model of the SHA when the MOS switch is on. (c) Clocks Φ_k for $k = 1$ and 2. $T = 2T_S$.

The timing diagram is shown in Fig. 3(c), where n is a discrete time index and $T = 2T_S = 2/f_S$. The on-resistance of the sampling switch and the hold capacitor form a first-order low-pass circuit with time constant $\tau = R_{\text{on}}C$. The continuous-time input $x(t)$ is filtered by this circuit when the sampling switch is on. For SHA_1, the switch turns off at time $t = (n + 1/2)T$, and the voltage on the capacitor is held and later digitized by ADC_1. In practice, the values of R_{on} and C for one SHA may not be the same as for another SHA on an integrated circuit due to imperfect fabrication. If the $R_{\text{on}}C$ values of the SHAs are mismatched, then the bandwidths of the first-order filtering from the SHAs differ in the two parallel channels.

To concentrate on the bandwidth mismatch problem, assume that the ADCs in Fig. 2 are ideal and that the SHA in each channel can be modeled by a first-order system in the sample mode as shown in Fig. 3(b). The time constants associated with the two SHAs will be denoted as τ_1 and τ_2, respectively. Thus, the circuit in Fig. 3(b) can be described by the following equation:

$$x(t) = y_k(t) + \tau_k \cdot \frac{dy_k(t)}{dt}, \qquad k = 1, 2 \tag{1}$$

where $y_k(t)$ is the capacitor voltage on C_k at time t, and k is the channel. Consider channel 1 first. The capacitor voltage $y_1(t)$ during the tracking phase of the nth cycle is obtained by using the convolution integral and the initial held voltage on C_1 from the previous cycle, i.e., $y_1[n-1]$ [8]. Thus

$$y_1(nT + t') = y_1[n-1] + \int_{nT}^{nT+t'} \{x(u) - y_1[n-1]\} P_1(nT + t' - u)du \tag{2}$$

where $P_1(t) = (1/\tau_1) \cdot \exp(-t/\tau_1)$, and t' varies from 0 to $0.5T$. The sampled output $y_1[n]$ is obtained by setting $t' = 0.5T$ in (2). After some simplification

$$\begin{aligned} y_1[n] &= y_1\left((n + 0.5)T\right) \\ &= y_1[n-1] \exp\left(-\frac{T}{2\tau_1}\right) \\ &\quad + \int_0^{T/2} x\left(\left(n + \frac{1}{2}\right)T - v\right) P_1(v)dv. \end{aligned} \tag{3}$$

The first term on the right of (3) stems from the residue charge on C_1 from the previous sample. If the hold capacitor C_1 is reset before each sampling phase, this term becomes zero. By iteration from (3), the sampled output at the nth cycle can be described as

$$\begin{aligned} y_1[n] &= \sum_{\ell=-\infty}^{n} \exp\left\{-\frac{T}{2\tau_1}(n-\ell)\right\} \\ &\quad \times \int_0^{T/2} x\left(\ell T + \frac{1}{2}T - v\right) P_1(v)dv \\ &= \sum_{\ell=-\infty}^{n} \exp\left\{-\frac{T}{2\tau_1}(n-\ell)\right\} \cdot W_\ell\left(\frac{T}{2}\right) \end{aligned} \tag{4}$$

where $W_\ell(T/2)$ is the ℓth convolution integral from 0 to $T/2$. Define $h_1(t) = P_1(t)$, $0 \le t \le T/2$, and 0 for elsewhere. $W_\ell(T/2)$ can be calculated as

$$\begin{aligned} W_\ell\left(\frac{T}{2}\right) &= \int_{-\infty}^{\infty} x\left(\ell T + \frac{T}{2} - v\right) h_1(v)dv \\ &= \int_{-\infty}^{\infty} e^{j\omega(\ell T + T/2)} X(\omega) H_1(\omega)d\omega \end{aligned} \tag{5}$$

where $X(\omega)$ and $H_1(\omega)$ are the Fourier transform of $x(t)$ and $h_1(t)$, respectively. $H_1(\omega)$ can be expressed as

$$H_1(\omega) = \frac{1 - e^{-(T/2\tau_1 + j\omega T/2)}}{(1 + j\omega\tau_1)}. \tag{6}$$

Substituting $W_\ell(T/2)$ from (5) into (4) and carrying out the analysis in the frequency domain yields

$$\begin{aligned} y_1[n] &= \int_{-\infty}^{\infty} \frac{X(\omega)\left(1 - e^{-(T/2\tau_1 + j\omega T/2)}\right) e^{j\omega(n+0.5)T}}{(1 + j\omega\tau_1)\left(1 - e^{-(T/2\tau_1 + j\omega T)}\right)} d\omega \\ &= \int_{-\infty}^{\infty} X(\omega) G_1(\omega) e^{j\omega(n+0.5)T} d\omega \end{aligned} \tag{7}$$

where

$$G_1(\omega) = \frac{1 - e^{-(T/2\tau_1 + j\omega T/2)}}{(1 + j\omega\tau_1)\left(1 - e^{-(T/2\tau_1 + j\omega T)}\right)}. \tag{8}$$

Equation (7) shows that the sampled output from channel 1, i.e., $y_1[n]$, is the result of the input signal $x(t)$ passing through a linear filter with magnitude response $|G_1(\omega)|$. Similarly, following the analysis above, $H_2(\omega)$ can be found by replacing τ_1 with τ_2, computing the convolution integral when Φ_2 is high, and sampling the output from channel 2 at $t = (n + 1)T$. The sampled output from channel 2 is given by

$$\begin{aligned} y_2[n] &= \int_{-\infty}^{\infty} \frac{X(\omega)\left(1 - e^{-(T/2\tau_2 + j\omega T/2)}\right) e^{j\omega(n+1)T}}{(1 + j\omega\tau_2)\left(1 - e^{-(T/2\tau_2 + j\omega T)}\right)} d\omega \\ &= \int_{-\infty}^{\infty} X(\omega) G_2(\omega) e^{j\omega(n+1)T} d\omega \end{aligned} \tag{9}$$

where

$$G_2(\omega) = \frac{1 - e^{-(T/2\tau_2 + j\omega T/2)}}{(1 + j\omega\tau_2)\left(1 - e^{-(T/2\tau_2 + j\omega T)}\right)}. \tag{10}$$

For a sinusoidal input of $x(t) = A\cos(\omega t)$, the output samples of the ADC array, i.e., $y[n]$, are given by

$$y[n] = |G_k(\omega)|\, A\cos\left[\omega(nT_S + T/2) + \theta_k(\omega)\right] \tag{11}$$

where $k = 1$ for n odd, $k = 2$ for n even, and

$$|G_k(\omega)| = \frac{|1-e^{-T/2\tau_k - j\omega T/2}|}{|1-e^{-T/2\tau_k - j\omega T}|\sqrt{1+(\omega\tau_k)^2}}, \quad k = 1,2 \tag{12}$$

$$\theta_k(\omega) = \angle G_k(\omega), \qquad k = 1,2. \tag{13}$$

$|G_1(\omega)|$ and $|G_2(\omega)|$ are the gains, and $\theta_1(\omega)$ and $\theta_2(\omega)$ are the phase shifts introduced by the SHAs. If τ_1 and τ_2 are not equal, a bandwidth mismatch exists between the two time-interleaved channels. With bandwidth mismatch, $|G_1(\omega)|$ and $|G_2(\omega)|$ are not equal as shown in (12). Thus, gain mismatches are introduced by bandwidth mismatches. Similarly, $\theta_1(\omega)$ will not equal $\theta_2(\omega)$ if τ_1 is not equal to τ_2. Phase mismatches are also introduced by bandwidth mismatches. Therefore, the undesired effects of bandwidth mismatch include both gain and phase mismatches that are input frequency dependent as shown in (12) and (13).

With finite SHA bandwidths, using (11) for $k = 1$ and $k = 2$, the ADC output can be written as [4]

$$y[n] = B_s\cos\left(\omega\cdot nT_s + \frac{T}{2} + \theta_s\right) + B_n\cos\left[(\omega_s/2-\omega)nT_s + \frac{T}{2} + \theta_n\right]. \tag{14}$$

The first term on the right of (14) is the input signal sampled, scaled by gain B_s and phase shifted by θ_s. The second term on the right is an undesired tone due to the bandwidth mismatch, which appears at an image frequency $\omega_i = \omega_S/2 - \omega$, where $\omega_S = 2\pi f_S$. For the case $\tau_1 = \tau_2$ (no bandwidth mismatch), B_n becomes 0 and B_s equals $A|G_1(\omega)|$. Minimizing or eliminating the image amplitude B_n will improve the SNDR of the interleaved ADC system. The effect of bandwidth mismatch is worse at high frequencies than at low frequencies. Therefore, such mismatch may be only noticeable for high-frequency input signals.

If the sampling capacitor is reset before each sampling phase, the charge from the previous sampling cycle is discarded before a new sample is taken. Then the sampled output, i.e., $y_k[n]$, is simply the convolution of the input $x(t)$ and the impulse response of a one-pole filter with time constant $R_{\mathrm{on},k}C_k$ for a period $T/2$. For example, with reset, $y_1[n]$ is given by the integral term in (3), which is expressed in (5) as

$$\begin{aligned} y_1[n] &= \int_{-\infty}^{\infty} x(nT + 0.5T - v)h_1(v)dv \\ &= \int_{-\infty}^{\infty} e^{j\omega(nT+0.5T)}X(\omega)H_1(\omega)d\omega \end{aligned} \tag{15}$$

where $H_1(\omega)$ is given in (6). Thus, with reset, the sampled output from channel 1 is the result of the input $x(t)$ passing through a filter with magnitude response $|H_1(\omega)|$. Similarly, the sampled output of channel 2 is the result of passing the input through a filter with magnitude response $|H_2(\omega)|$.

The on-resistance of a MOS sampling switch is assumed to be a constant R_{on} in the analysis above. However, R_{on} is a function of the input signal [9] in practice. If square-law equations can be applied, and if the voltage difference between the drain and source is small (i.e., $V_{\mathrm{ds}} \ll V_{\mathrm{gs}} - V_T$) when the switch is on, the on-resistance can be approximated by [10]

$$R_{\mathrm{on}}fs = \frac{1}{\mu_n C_{\mathrm{ox}}\frac{W}{L}(V_{\mathrm{gs}} - V_T)}. \tag{16}$$

Distortion is introduced into the sampled signal when R_{on} varies with the input signal [11]. During the sampling phase, $V_{\mathrm{gs}} = V_{\mathrm{dd}} - V_{\mathrm{in}}$ because the gate voltage of the MOS switch is held at the supply voltage V_{dd}. The R_{on} variation is severe when the amplitude of the input signal is large. Hence, limiting the input signal to a small range helps to reduce distortion.

To avoid reducing the input range, the transistor is typically sized large enough, so that the value of R_{on} remains small for the entire input signal range. Keeping R_{on} constant without using large switches is desirable to avoid nonlinearity limitations from large voltage-dependent parasitic capacitances. Ideally, R_{on} should be independent of the input signal. Bootstrapping can be used to make R_{on} approximately constant [12].

III. Bandwidth Mismatch Correction

Fig. 4 shows the block diagram of the digital calibration for bandwidth mismatch correction. Digital finite impulse response (FIR) filters $F_1(z)$ and $F_2(z)$ are inserted in the paths of the channels for the bandwidth mismatch correction. The goals of filters F_1 and F_2 are to compensate for the filtering effects introduced by the SHAs and eliminate the image components at the image frequency ω_i.

To determine the filters that can compensate for bandwidth mismatches between the interleaved SHAs, consider an input signal $x(t) = A\cos(\omega_0 t)$. First, consider $e^{j\omega_0 t}$, the positive frequency component of the input $x(t)$. Ideally, the input/output processing in Fig. 4 should give unity gain and zero phase shift at ω_0 while eliminating the image at $-\omega_s/2 + \omega_0$, i.e.,

$$F_1(\omega_0)G_1(\omega_0) + F_2'(\omega_0)G_2(\omega_0)e^{j\omega_0 T_s} = 2 \tag{17}$$

$$F_1(-\omega_s/2+\omega_0)G_1(\omega_0) + F_2'(-\omega_s/2+\omega_0)G_2(\omega_0)e^{j\omega_0 T_s} = 0. \tag{18}$$

Here, $F_2'(z) = F_2(z)z^{-1}$ has been used to simplify the equations. Similarly, the equations for the negative frequency component of the input, i.e., $e^{-j\omega_0 t}$, are given by

$$F_1(-\omega_0)G_1(-\omega_0) + F_2'(-\omega_0)G_2(-\omega_0)e^{-j\omega_0 T_s} = 2 \tag{19}$$

$$F_1(\omega_s/2-\omega_0)G_1(-\omega_0) + F_2'(\omega_s/2-\omega_0)G_2(-\omega_0)e^{-j\omega_0 T_s} = 0. \tag{20}$$

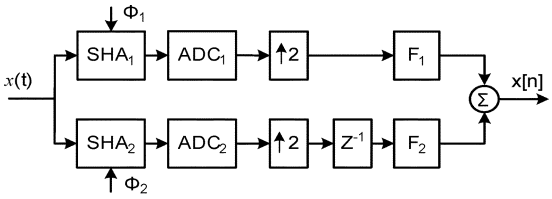

Fig. 4. Block diagram of bandwidth mismatch correction.

From the last four equations, F_1 and F_2 are given as

$$F_1(\omega)=\frac{2G_2(-\omega_s/2+\omega)}{G_2(\omega)G_1(-\omega_s/2+\omega)+G_1(\omega)G_2(-\omega_s/2+\omega)} \tag{21}$$

$$F_2(\omega)=\frac{2G_1(-\omega_s/2+\omega)}{G_2(\omega)G_1(-\omega_s/2+\omega)+G_1(\omega)G_2(-\omega_s/2+\omega)}. \tag{22}$$

Because $F_1(\omega)$ and $F_2(\omega)$ are discrete-time filters, (21) and (22) are valid for $-\omega_s/2 \le \omega \le \omega_s/2$ and periodic with period ω_s.

Extension to M channels requires finding $G_k(\omega)$ for $k = 1,\ldots,M$ following the steps in Section II and then solving for the correction filters $F_k(\omega)$ for $k = 1,\ldots,M$ using an M-channel extension of (17)–(20). The extension of (17) and (18) to M channels is

$$\sum_{i=1}^{M} F_i'(\omega)G_i(\omega)e^{j\omega(i-1)T_s}=M \tag{23}$$

$$\sum_{i=1}^{M} F_i'(\omega_k)G_i(\omega)e^{j\omega(i-1)T_s}=0, \qquad k=1,2,\ldots,M-1 \tag{24}$$

where $\omega_k = \omega - k(\omega_s/M)$ and $F_i'(\omega) = e^{-j\omega(i-1)}F_i(\omega)$.

IV. Simulation Results

Simulations were carried out on the system in Fig. 4, which has two time-interleaved channels. The input is $x(t) = A\cos(\omega_1 t+\theta_1)+A\cos(\omega_2 t+\theta_2)+A\cos(\omega_3 t+\theta_3)$. The bandwidth of the top SHA is $\omega_{c1} = \omega_S/2$, and $\omega_{c2} = 0.95(\omega_{c1})$ for the bottom SHA, giving a 5% bandwidth mismatch between the two channels. The input frequencies are $\omega_1 = 0.0376(\omega_s)$, $\omega_2 = 0.1154(\omega_s)$, and $\omega_3 = 0.3962(\omega_s)$, respectively. For simplicity, each ADC samples its input but does not quantize the signal. Fig. 5 shows the output spectrum of the ADC system with bandwidth mismatches before correction. The highest undesired tone appears at −42.8 dB. Fig. 6 shows the same output spectrum after bandwidth mismatch correction with 61-tap FIR filters for F_1 and F_2. The largest undesired tone is decreased to −87.1 dB. The coefficients of the FIR filters were found by calculating the inverse discrete Fourier transform (IDFT) of F_1 and F_2 in (21) and (22) and then applying a Hann window. The magnitude responses of F_1 and F_2 are shown in Fig. 7. Table I gives the largest undesired tone magnitude and its attenuation for different correction filter lengths.

Extension to four channels has been carried out and verified by simulation. The SHA bandwidths in this simulation are $\omega_{C1} = \omega_S/2$, $\omega_{C2} = 0.95(\omega_{C1})$, $\omega_{C3} = 0.97(\omega_{C1})$, and $\omega_{C4} = 0.90(\omega_{C1})$, giving a 10% peak bandwidth mismatch among the four parallel channels. The input is the same as was

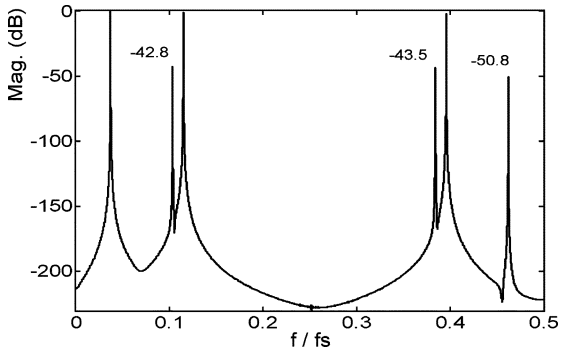

Fig. 5. Spectrum of the two-channel ADC output with a three-tone input before correction.

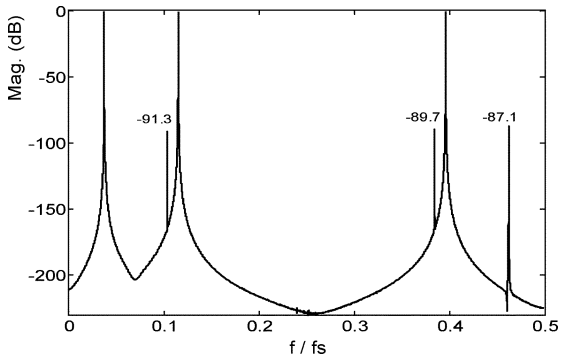

Fig. 6. Spectrum of the two-channel ADC output with a three-tone input after correction.

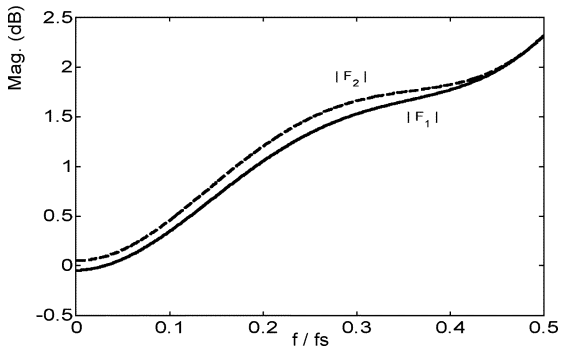

Fig. 7. Magnitude responses of the correction filters F_1 and F_2.

TABLE I
Undesired Tone Magnitude and Its Attenuation for Different Numbers of Filter Taps (Two-channel ADC System)

Number of taps (f_1, f_2)	Largest undesired tone	Attenuation of largest undesired tone
11	–48.4 dB	5.6 dB
21	–57.4 dB	14.6 dB
31	–67.0 dB	24.2 dB
41	–78.7 dB	35.9 dB
61	–87.1 dB	44.3 dB
81	–91.2 dB	48.4 dB
101	–96.5 dB	53.7 dB
201	–108.4 dB	65.6 dB

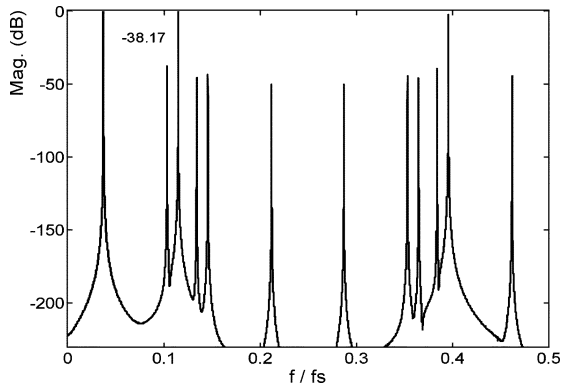

Fig. 8. Spectrum of the four-channel ADC output with a three-tone input before correction.

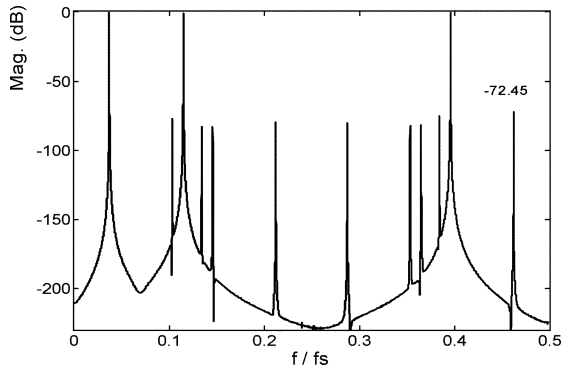

Fig. 9. Spectrum of the four-channel ADC output with a three-tone input after correction (61-tap correction filters).

TABLE II
UNDESIRED TONE MAGNITUDE AND ITS ATTENUATION FOR DIFFERENT NUMBERS OF FILTER TAPS (FOUR-CHANNEL ADC SYSTEM)

Number of taps (f_1, f_2, f_3, f_4)	Largest undesired tone	Attenuation of largest undesired tone
11	–43.5 dB	5.3 dB
21	–50.0 dB	11.8 dB
31	–58.0 dB	19.8 dB
41	–65.0 dB	26.8 dB
61	–72.4 dB	34.2 dB
81	–77.1 dB	38.9 dB
101	–81.2 dB	42.0 dB
201	–93.2 dB	54.0 dB

used for the two-channel case. The spectra before and after correction are shown in Figs. 8 and 9. Simulation results for the undesired tones for different numbers of correction filter taps are in Table II.

V. CONCLUSION

Analysis of the effect of SHA bandwidth mismatch, based on a first-order SHA model, and its correction by digital filters in a two-channel ADC have been presented. Digital correction becomes increasingly attractive as CMOS technology advances, which decreases the area and power dissipation required by digital circuits. Digital correction has also been shown to work in a four-channel interleaved system and can be extended to any number of channels.

The effect of SHA bandwidth mismatch can be estimated through simulation using the G_k filters and the estimated SHA time-constant τ_k mismatch, based on transistor and capacitor mismatch data. Then the complexity of correction filters can be determined, based on the desired ADC performance.

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