Audio Audio	Xbar I2C CAN SPI Serial	PWM		Digital DiwM	Analog Serial	CAN 12C Xbar	OIX	oibu OIA	/ative	Prop Audio
G GND	Xba Xba SPI SPI Seri	≧ iji GND		.jg } Vin	Ana Seri	CAN Xba	A A	Au	Z Z	
AD_B0_03 1.3	17 RX2 CS1 RX1	1X1 0		GND						G G
AD_B0_03 1.3 AD B0 02 1.2	16 TX2 MISO1 TX1	1X0 1	THE PARTY OF THE P	3.3V 250mA m	nax					3V 3.3
S EMC_04 4.4 O2 1:4	6	4A2 2	ADV B China C	23 4A1		RX1	3:9 N	MCL1 1.25 A	AD B1 09 (CSD D8 A
M EMC_05 4.5 LR2 1:5	7	4B2 3		22 4A0		TX1	3:08			CSI_D9
A EMC_06 4.6 BCL2 1:6	8	2A0 4		21	A7 RX5			BCL1 1.27 A		CSI_D6 A
A A-EN EMC_08 4.8 IN2 1:8	17	2A1 5	God III	20	A6 TX5			RC1 1.26 A		CSI_D7 A
M-CS B0_10 2.10 O1D 2:10		2A2, Q41 6	6 nd : 11 ["""] *	19 Q30	A5 CTS3	SCL0	3:00	1.16 A	AD_B1_00	S C
L-EN B1_01 2.17 O1A 2:17, 3:1	17 15 RX2	1B3 7		18 Q31	A4	SDA0	3:01	1.17 A	AD_B1_01	S C
B1_00 2.16 IN1 2:16, 3:1	16 14 sda0 TX2	1A3 8	A CONTRACTOR OF THE PARTY OF TH	17	A3 TX4	SDA1	3:06	1.22 A	AD_B1_06 CS	SI_VSYNC
B0_11 2.11 O1C 2:11		2B2,Q42 9	· >	16	A2 RX4	SCL1	3:07	1.23 A	AD_B1_07 CS	I_HSYNC
S B0_00 2.0 MQR 2:0	CS0	Q10 10	MIMXRT1062	15 Q33	A1 RX3		3:03	SPDI 1.19 <i>F</i>	AD_B1_03	V
SM M/L B0_02 2.2 2:2	TX1 MOSI0	Q12 11	6N06X	14 Q32	A0 TX3		3:02 S	SPDO 1.18 A	AD_B1_02	
SM M B0_01 2.1 MQL 2:1	MISO0	Q11 12	CTAB1912J	13 Q20	LED SCK0	rx1	2:03	2.3	B0_03	M SM
		3.3V		GND						
AD_B0_12 1.12	SCL2 TX6 A10-1	1X2 24	O partition and the control of the c	41 G21	A17		3:5	1.21 A	AD_B1_05 C	SI_MCLK
AD_B0_13 1.13	SDA2 RX6 A11-1	1X3 25		40	A16		3:4	1.20 A	AD_B1_04	
CSI_D3 AD_B1_14 1.30 3:14	MOSI1 A12-2	26		39	A15-2 MISO1		3:13	1.29 A	AD_B1_13 (CSI_D4
CSI_D2 AD_B1_15 1.31 3:15	SCK1 A13-2	27		38	A14-2 CS1-0		3:12	1.28 A	AD_B1_12 (CSI_D5
EMC_32 3.18	RX7	3B1 28		37 2B3	CS0-1	17	2:19,3:19	2.19	B1_03	
EMC_31 4.31	TX7	3A1 29	Prog Prog SND	36 2A3	CS0-2	16	2:18,3:18	2.18	B1_02	
EMC_37 3.23	23 RX3	G13 30		35	TX8		2:28,3:28	2.28	B1_12 CS	SI_PIXCLK
EMC_36 3.22	22 TX3	G12 31		34		RX1	2:29,3:29	2.29		SI_VSYNC
B0_12 2.12 O1B 2:12	10	32	OM CHILLIANO	33 2B0		TX1 9	1:7 N	MCL2 4.7	EMC_07	
-										
SD_B0_03 2.15 DATA1	7 MISO2		SDIO Pins	47 1A2	TVE	0	DATA2	3.16 S	D_B0_04	
SD_B0_03 2.15 DATA1 SD B0 02 3.14 DATA0	6 MOSI2 CTS5	1B1 42 1A1 43		47 1A2 46 1B2	TX5 RX5		DATA2 DATA3		D_B0_04 D_B0_05	
		GND		45 1A0	SCK2		CMD		D_B0_00	
SD_B0_01 3.13 CLK	5 SDA1 CS2	1B0 44			3.3V					
			D. I.M Ol.							
EMC 26 4.26 1:1	12 RX1	1B1 52	Back Memory Chips	GND						
					CTCO MOCIO		4.4.4	4.28 E	MC_28	
	TX1 MISO2				CTS8 MOSI2		1:14			
EMC_29 4.29 1:1	MISO2	3A0 54		49 1A2 51 3B3,Q23	SCK2	0014	1:13		MC_27	
		3.31	este	51 303,423	,	SCL1		4.22 E	IVIC_ZZ	
EMC_26 4.26 1:1	12 RX1	1B1 52	100000	GND						
EMC 25 4.25	TX1	1A1 53	Comment of the latest of the l	50 1B2	CTS8 MOSI2		1:14	4.28 E	MC 28	
EMC_29 4.29 1:1		3A0 54	Name and Address of the Owner, where the Personal Property lies are not to the Personal Property lies are no	49 1A2	SCK2		1:13		MC_27	
LIVIO_23 4.23 1.1	WIGOZ	3.3V	The second secon	49 1A2 48 1B0	RX8		1.10		MC_24	
				40 .50	IVAU			7.47	1110_41	