**Angeles University Foundation**

*College of Engineering and Architecture*

Computer Engineering Department

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| **NAME OF STUDENT:** |
| **GROUP NUMBER: DATE PERFORMED:** |
| **COURSE CODE:** *AEC 41* **DATE SUBMITTED:** |
| **COURSE TITLE:** *Logic Circuits and Switching Theory***YEAR AND SECTION:** |
| **LAB. INSTRUCTOR: GRADE:** |

EXPERIMENT NO. 9

**RS and D Flip-Flop**

1. ***OBJECTIVES:***
2. To determine how to construct an RS Flip-Flop using resistors and transistors, using NOR gates and D Flip-Flop using NAND gates.
3. To verify the operation and characteristics of a RS and D Flip-Flops.
4. To introduce to clocked triggered logic gates
5. ***MATERIALS AND EQUIPMENT:***

1 - Digital Trainer

1 - Logic Probe

1 - TTL 74LS00

1 - TTL 74LS75

1 - 4001 CMOS IC

2 - 5Kohm Resistors

4 - 100Kohm Resistors

2 - MPSA20 Transistors

1 - IC Remover

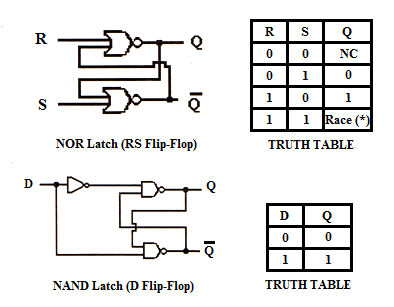
1 - Set Connecting Copper Wires

1. ***INTRODUCTION:***

The memory unit of a computer is composed of small storage circuits called Flip-Flops. All flip-flops are bistable devices, which mean that they are capable of storing two stable states depending on their input signals. Flip-flops have the ability to retain their stored data unless otherwise triggered to change. In this experiment involves the operation of the RS and D Flip-Flops.

The simplest form of flip-flop is the R-S flip-flop. There are two input signals R and S, and two output signals Q and Q’. RS flip-flops can be constructed using NOR or NAND latch, although in this experiment it will investigate the use of a NOR latch.

The RS Flip-flop was modified to avoid the race condition, thus producing what is called the D-Flip-flop. The main characteristic of a D Flip-flop is that its input D is equal to its output Q once it is triggered. A D Flip-flop is commonly used as a storage device in the memory unit of a computer. Figure 1 shows the logic diagram of the RS and D Flip-flop with their corresponding truth table. Take note that in all two outputs of all flip-flops, one is the complement of the other.

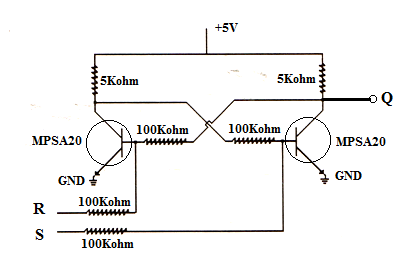


**Figure 1**

This experiment, particularly of the D Flip-flop will be implemented using the NAND latch and will also make use of the TTL 74LS75 IC. It is an enabled 2-2 bit D latch. Take note that this is a 16 pin IC and unlike the other 14 pin IC which has been used from the previous experiments. The power supply of this IC is at pin 12 for th negative and pin 5 for the positive.

1. ***PROCEDURE:***
2. ***RS Flip-Flop***

**Discrete Circuit testing using Logic Probe**

* 1. Connect the circuit as shown in Figure 2.

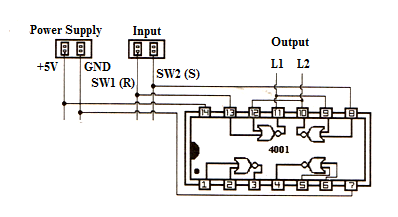
**Figure 2**

* 1. Using the logic probe, determine the output of the circuits at point Q, using the input combinations at Table 1. Record the readings in Table 1.

**Table 1**

|  |  |  |
| --- | --- | --- |
| **R** | **S** | **Q** |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

* 1. Connect the circuit as shown in Figure 3.



**Figure 3**

* 1. Using the input combinations in Table 2, observe the output of the Flip-Flop at L1 and L2. Record your readings in Table 2

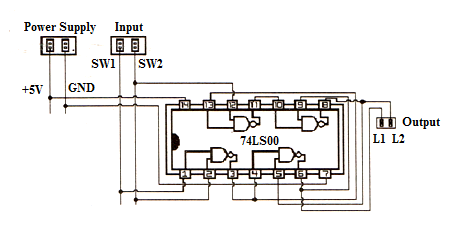
**Table 2**

|  |  |  |  |
| --- | --- | --- | --- |
| **R** | **S** | **L1** | **L2** |
| 1 | 0 |  |  |
| 0 | 0 |  |  |
| 0 | 1 |  |  |
| 0 | 0 |  |  |
| 1 | 0 |  |  |
| 0 | 0 |  |  |
| 1 | 1 |  |  |

1. ***D Flip-Flop***

**Integrated Circuit testing using Logic Probe**

* 1. Connect the circuit shown in Figure 4. Be careful in connecting the wires. This circuit will make use of the 74LS00 TTL IC in constructing the D- Flip-Flop. SW1 will serve as the input to the Flip-Flop and SW2 will serve as the clocking device. The LED indicators L1 and L2 will determine the output.



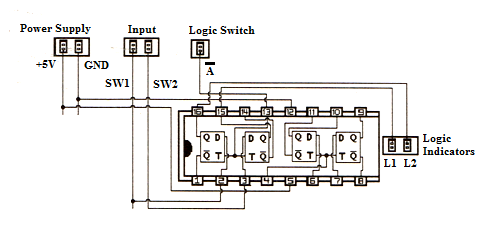
**Figure 4**

* 1. Using the input values of SW1 and SW2 in Table 3, determine the output of the circuit using your logic probe. Record the readings in Table 3.

**Table 3**

|  |  |  |  |
| --- | --- | --- | --- |
| **SW1** | **SW2** | **L1** | **L2** |
| 0 | 0 |  |  |
| 0 | 1 |  |  |
| 0 | 1 |  |  |
| 0 | 0 |  |  |
| 1 | 0 |  |  |
| 1 | 1 |  |  |
| 1 | 1 |  |  |
| 1 | 0 |  |  |

* 1. Wire the circuit shown in Figure 5.



**Figure 5**

* 1. Using the input conditions in Table 4, determine the output of the circuit using the logic indicators L1 and L2. Record your readings in Table 4.

**Table 4**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Logic Switch** | **SW1** | **SW2** | **L1** | **L2** |
| A complement.png | 0 | 0 |  |  |
| A complement.png | 0 | 1 |  |  |
| A complement.png | 1 | 1 |  |  |
| A complement.png | 1 | 0 |  |  |
| A complement.png | 1 | 1 |  |  |
| A complement.pngA complement.png | 0 | 0 |  |  |
|  | 1 | 1 |  |  |
| A complement.png | 0 | 1 |  |  |

1. ***QUESTIONS:***
2. Analyze carefully the circuit in Figure 2. Explain how it works.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. Observe carefully the values of L1 and L2 of Figure 3. How is L1 related to L2? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
2. Observe the data on Table 4. What is the function of the logic switch? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
3. Enumerate the possible applications of RS and D Flip-Flops. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
4. ***PROBLEM:***
5. Draw the IC layout of the NAND latch equivalent circuit to RS Flip-Flop using TTL 74LS00 IC.

1. Draw the logic circuit equivalent of D Flip-Flop using NOR gates.
2. ***CONCLUSION:***

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_