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Control signals for various states:
// This is our default state. It assigns instruction address to memory
State 8'h0:
                ld_mar=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                pc_alu=1;
                ld_mar=1;
                mem_size=1;
                mem_r_w=1;

// Read state. Reads instruction from memory to mdr
State 8'h1:
                ld_mdr=1;
                mdr_sext=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=1;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;
                reset=0;

// Fetch state. IR fetches instruction
State 8'h2:
                ld_mar=1;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;
                mar_8=0;
                sel_mem=01;
                mem_r_w=1;
                ld_ir=1;

// Load state. Loads in ir
State 8'h3:
                ld_mar=0;
                ld_ir=1;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;

// Decode state. This decodes the instruction
State 8'h4:
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;

// Once we have decoded the instruction, we can start with the signals

// BR instruction state i.e Opcode [15:12] = 0000
State 8'h10:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;
                if((n==opcode[11]) or (z==opcode[10]) or (p==opcode[9]))
                {     nine=01;
                      sel_pc=01;
                }

State 8'h11:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;
                ld_pc=0;

// ADD instruction state i.e Opcode [15:12] = 0001
State 8'h20:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1 ;
                sr1 = opcode[8:6];
                sr2 = opcode[2:0];
                dr = opcode[11:9];
                reg_r=1;
                reg_w=0;
                alusel={opcode[5],1'b0};

State 8'h21:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;
                opsel=001;
                reg_w=1;
                reg_r=0;
                rfsel=11;
                sel_pc=2'b10;

// LDB instruction state i.e Opcode [15:12] = 0010
State 8'h30:
                pc_alu=0;
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_r=1;
                reg_w=0;
                alusel=01;

                dr=opcode[11:9];
                sr1=opcode[8:6];
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State 8'h31:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;
                opsel=001;
                ld_mar=1;
                mem_size=0;

State 8'h32:
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                ld_mdr=1;
                mdr_sext=1;
                sel_mem=01;
                rfsel=00;
                reg_w=1;
                reg_r=0;
                sel_pc=2'b10;

// STB instruction state i.e Opcode [15:12] = 0011
State 8'h40:
                pc_alu=0;
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_r=1;
                reg_w=0;
                alusel=01;
                opsel=001;

                sr2=opcode[11:9];
                sr1=opcode[8:6];

State 8'h41:
                ld_mdr=0;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;
                pc_alu=0;
                ld_mar=1;
                mem_size=0;

State 8'h42:
                ld_mdr=1;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=0;
                pc_alu=0;
                mdr_sext=0;
                ld_mar=0;
                sel_pc=2'b10;
                sel_mem=10;

// JSR/JSRR instruction state i.e Opcode [15:12] = 0100
State 8'h50:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                dr=3'd7;
                reg_w=1;
                reg_r=0;
                rfsel=10;

                sr1=opcode[8:6];

State 8'h51:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                reg_w=0;
                mem_r_w=1;
                if(opcode[11]==1)
                {   reg_r=0;
                    nine=00;
                    sel_pc=01;
                }
                else
                {   reg_r=1;
                    alusel=01;
                    opsel=001;
                    sel_pc=00;
                }

State 8'h52:
                alusel=10;
                sel_pc=00;
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=1;
                reg_r=0;
                reg_w=1;
                mem_r_w=1;

State 8'h53:
                sel_pc=10;
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=1;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;

// AND instruction state i.e Opcode [15:12] = 0101
State 8'h60:
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                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_r=1;
                reg_w=0;
                alusel={opcode[5],1'b0};

                sr1 = opcode[8:6];
                sr2 = opcode[2:0];
                dr = opcode[11:9];

State 8'h61:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                opsel=000;
                reg_w=1;
                reg_r=0;
                rfsel=11;
                sel_pc=2'b10;

// LDW instruction state i.e Opcode [15:12] = 0110
State 8'h70:
                pc_alu=0;
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_r=1;
                reg_w=0;
                alusel=01;

                dr=opcode[11:9];
                sr1=opcode[8:6];

State 8'h71:
                ld_mdr=0;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                opsel=001;
                pc_alu=0;
                ld_mar=1;
                mem_size=1;
                mem_r_w=1;

State 8'h72:
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                ld_mdr=1;
                mdr_sext=0;
                sel_mem=01;
                rfsel=00;
                reg_w=1;
                reg_r=0;
                sel_pc=2'b10;

// STW instruction state i.e Opcode [15:12] = 0111
State 8'h80:
                pc_alu=0;
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_r=1;
                reg_w=0;
                alusel=01;

                sr2=opcode[11:9];
                sr1=opcode[8:6];

State 8'h81:
                ld_mdr=0;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                pc_alu=0;
                ld_mar=1;
                mem_size=1;
                sel_mem=10;
                mem_r_w=1;

State 8'h82:
                ld_mdr=1;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=0;
                pc_alu=0;
                mdr_sext=0;
                ld_mar=0;
                sel_mem=10;
                sel_pc=2'b10;

//XOR instruction state i.e Opcode [15:12] = 1001
State 8'h90:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_r=1;
                reg_w=0;
                alusel={opcode[5],1'b0};

State 8'h91:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;
                opsel=010;

State 8'h92:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_w=1;
                reg_r=0;
                rfsel=11;
                sel_pc=2'b10;

//JMP/RET instruction state i.e Opcode [15:12] = 1100
State 8'ha0:

                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_r=1;
                reg_w=0;
                alusel=10;
                opsel=001;
                sel_pc=00;

                sr1=opcode[8:6];

State 8'ha1:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=1;
                mem_r_w=1;
                reg_r=1;
                reg_w=0;

// LEA instruction state i.e Opcode [15:12] = 1110
State 8'hc0:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                reg_r=0;
                reg_w=0;
                mem_r_w=1;
                nine=01;

                dr=opcode[11:9];

State 8'hc1:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_w=1;
                reg_r=0;
                rfsel=01;
                sel_pc=2'b10;

//SHF instruction state i.e Opcode [15:12] = 1101
State 8'hb0:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_r=1;
                reg_w=0;
                alusel=11;

                sr1 = opcode[8:6];
                dr = opcode[11:9];

State 8'hb1:
                ld_mdr=0;
                ld_mar=0;
                ld_ir=0;
                ld_pc=0;
                mem_r_w=1;
                reg_w=1;
                reg_r=0;
                rfsel=11;

                if (opcode[5:4] == 2'b00) opsel=011;
                else if (opcode[5:4] == 2'b01) opsel=100;
                else if (opcode[5:4] == 2'b10) opsel=101;
```