MAULANA ABUL KALAM AZAD
UNIVERSITY OF TECHNOLOGY,
WEST BENGAL

THE DEPARTMENT OF
MICROELECTRONICS AND VLSI TECHNOLOGY

SYLLABUS

FOR POST GRADUATE DEGREE COURSE (M.Tech)

IN

Embedded Systems and VLSI Design

VISION OF THE UNIVERSITY

To achieve the status of a globally ranked premier University in the field of Science, Technology, Pharmacy, Architecture, Management and interdisciplinary areas for the creation of high-caliber professionals with environmental consciousness, social, moral and ethical values along with the competency to face the new challenges of rapid technological advancements.

MISSION OF THE UNIVERSITY

To impart quality and value-based teaching & learning of international standard for solving the real life problems

- To create and disseminate knowledge both nationally & internationally towards the transformations of the civilization into a knowledge-based society
- To institutionalize the extension and field outreach activities with a view to transform the university system into an active instrument for social change
- To develop liaison and collaboration with the globally recognized academic institutions in order to inject new and fresh thinking in teaching, learning and research
- To generate intellectually capable and imaginatively gifted professionals and successful entrepreneurs having environmental consciousness and ethics who can work as individual or in group in multi-cultural global environments for continuing significantly towards the betterment of quality of human life.

Vision of Department of Microelectronics and VLSI Technology

The Department of Microelectronics and VLSI Technology envisions being a leader in pursuit of knowledge and wisdom for the holistic development of the rapid technological advancements of society in multi-disciplinary areas through excellence in teaching, training, and research and aspires to meet the global and socio-economic challenges of the state as well as country.

Mission statements of the Department of Microelectronics and VLSI Technology (MS)

The Department of Microelectronics and VLSI Technology motivates

MS-1: To participate in the Special Man Power Development Program to meet the ever-challenging issues in the field of Microelectronics and VLSI Technology

MS-2: To enable the students to formulate, design, and solve problems in applied science and engineering.

MS-3: To provide excellent teaching and research environment using state-of-the-art facilities.

MS-4: To provide adequate support in developing knowledge-based skills to meet the requirements of the Microelectronics, Embedded Systems, & VLSI industry.

MS-5: To develop a positive attitude among students to participate in collaborative research work

Program Outcomes (POs)

PO 1: An ability to independently carry out research /investigation and development work to solve practical problems
PO 2: An ability to write and present a substantial technical report/document
PO 3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PO 4. Acquire competency in the areas of VLSI and Embedded Systems, Design, Testing, Verification and prototype development focusing on applications.
PO 5. Integrate multiple sub-systems to develop System-On-Chip, optimize its performance.
PO 6. Acquire technical skill to excel in industry sectors related to VLSI / Embedded domain.

Program Specific Outcomes (PSOs)

M. Tech. in **Embedded Systems and VLSI Design Program**, students will be able to:
PSO 1. Acquire competency in the areas of VLSI and Embedded Systems, Design, Testing, Verification and prototype development focusing on applications.
PSO 2. Integrate multiple sub-systems to develop System-On-Chip, optimize its performance.
PSO 3. Acquire technical skill to excel in industry sectors related to VLSI / Embedded domain.

Semester-wise Course Schedule:

Semester I

Sr. No.	Course Type/ Code	Course Name	Teaching			Credits
			L	T	p	
1	PGVES - 101	Digital VLSI Design	3	0	0	3
2	PGVES - 102	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3

3	PGVES-103: PE I	Elective I 1) Digital Signal and Image Processing 2) Programming Languages for Embedded Systems 3) VLSI signal processing	3	0	0	3
4	PGVES-104: PE II	Elective II 1) Parallel Architecture & Processing 2) System Design with Embedded Linux 3) CAD of Digital System	3	0	0	3
5	PGVES-105	Research Methodology and IPR	2	0	0	2
6.	PGVES-106 PA I	Audit course	2	0	0	0
7.	PGVES-191	Digital VLSI Design Lab	0	0	4	2
8.	PGVES-192	Micro-controller and Programmable Digital Signal Processor Lab.	0	0	4	2
		Total	**14**	**0**	**8**	**18**

Semester II

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	p	
1	PGVES - 201	Analog VLSI Design	3	0	0	3
2	PGVES - 202	VLSI Design Verification and Testing	3	0	0	3
3	PGVES-203: PE III	Elective III (1) Memory Technologies (2) SOC Design (3) Low power VLSI Design	3	0	0	3
4	PGVES-204: PE IV	Elective IV (1) Communication Buses and Interfaces (2 Introduction to AI , Machine Learning and Applications (3) Physical Design Automation	3	0	0	3
5	PGVES - 291	Analog VLSI Design Lab	0	0	4	2
6	PGVES - 292	VLSI Design Verification and Testing Lab	0	0	4	2
7	PGVES - 293	Mini Project	0	0	4	2
8	PGVES-205	Audit course 2	2	0	0	0
		Total	**14**	**0**	**12**	**18**

Semester-III

Sr. No.	Course Code	Course Name	Teaching Scheme	Credits

1.	PGVES-301: PE V	Elective -V 1) Communication Network 2) Selected Topics in Mathematics 3) Nano Materials and Nanotechnology	3	0	0	3
2.	PGVES - 302: OE VI	1. Business Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of Engineering Projects 5. Composite Materials 6. Waste to Energy	3	0	0	3
3	PGVES - 391	M.Tech. Project Phase-I (Dissertation Phase-I)	0	0	20	10
		Total	**6**	**0**	**20**	**16**

Semester-IV

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	p	
I.	PGVES - 491	M.Tech. Project Phase-II (Dissertation Phase-II)	-	-	32	16
		Total	**-**	**-**	**-**	**16**

Detailed Syllabus

PGVES101: Digital VLSI Design	**Lecture/Week:4 (3L,1T), Total lectures: 36 Hours**	**Credit:3**
Faculty: Dr. Mihir Mahata		

Course Outcomes:

After completion of this course, students will be able to

CO1: Learn the basics of Integrated Circuit (IC); different Domains of VLSI design, design automation tools and the state-of-the-art VLSI circuits.

CO 2: Learn CMOS logic behaviour, advantages and drawbacks using static, dynamic, Domino logic and Bi-CMOS logic

CO3.Learn the basics of CMOS fabrication and Layout.

CO4: Learn EDA tools and their advantages, concept of test bench, simulation, design verification, synthesis and hardware description language (Verilog/VHDL/System 'C'), the design of a 32-bit RISC CPU, Static RAM and Simulation, Synthesis & validation of the architectures on FPGA and analysis their performances.

CO5: learn the concept of Programmable Hardware and their requirements, FPGA -- architecture, configuration and design flow, concept of System on Chip (SOC), logical effort, path effort, path effort delay, path parasitic delay, designing fast circuits and multistage logic networks and the concept of delay **vs** fan out

MODULE1: Introduction to VLSI Design

Basics of Integrated Circuit (IC), SSI, MSI, LSI, VLSI, ULSI, Integration levels. History of IC development, Moore's Law, Different types of IC chips; Digital, Analog & Mixed signal ICs; Different Domains of VLSI design; EDA- the VLSI design CAD tools, VLSI design state-of-the-art, some emerging applications of VLSI, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay VLSI design of complex processor, VLSI Design Flow, Synthesis, layout generation, Verification and simulation, VLSI chip manufacturing process flow, Radiation-hardened VLSI technology.

MODULE2: CMOS logic Basics

Basics of MOS transistors and MOS as switches, Complementary CMOS logic, CMOS logic behaviour, advantages and drawbacks of CMOS logic, Pull-up and pull down network, conduction complement, complex logic function using CMOS, pass transistors, transmission gates, tri-state buffers, Flip- flops (D- F/F, JK F/F etc.), transistor count, Delay, drawbacks of CMOS, Dynamic logic, Domino logic, Bi-CMOS to overcome the drawbacks of CMOS, standard cell design, full custom design. example of standard cell., combinatorial and Sequential Logic circuits –asynchronous and

synchronous sequential circuits, Moore machine, Mealy machine, examples, Finite state machine design

MODULE3: Basics of CMOS Layout:

Introduction to VLSI fabrication and fabrication steps, Concept of MASK, Lithography, etching, polysilicon patterning, ion implementation , metallization etc., fabrication error, concept of layout , feature size, Lamda rule, concept of process technology , stick diagram, general design rules for layout, width spacing rule, poly diffusion interaction, contacts, VIA and contact spacing, examples of CMOS layout of an inverter, NAND /NOR gates, simplified design rule, full custom and standard cell layout, placement , routing .floor planning ,

MODULE4: Hardware description language & EDA tools

EDA tools and their advantages, concept of test bench, simulation, , design verification , synthesis, hardware description language (HDL) -VHDL/VERILOG/SYSTEM C etc.

MODULE 5: Programmable Hardware and FPGA (6)
Concept of Programmable Hardware (PLA, PLD, CPLD, FPGA) and their requirements, FPGA --Architecture, configuration and design flow , system design using FPGA, concept of System on Chip(SOC). FPGA as reconfigurable computing and programmable System on Chip (pSOC).

MODULE 6: Logical Effort

Logical effort, Path Logical Effort, Path Electrical Effort, Path Effort, branching effort, delay in a logic gate, path effort delay, path parasitic delay , designing fast circuits and gate sizes, multistage logic networks, choosing the best number of stages, delay **vs** fan out,

MODULE 7: Example of VLSI chip Design (Design of a 32-bit RISC CPU and 1K8 bit RAM

Designing a RISC CPU with fixed instruction length (32 bit) CPU, few instructions, Static RAM design with 1024 locations with each word size of 8 bits., Simulation, Synthesis & validation of the architecture on FPGA and analysis of the performance of the CPU with a small program written in machine language.

Text Books:

1. Carver Mead, Lynn Conway, Introduction to VLSI Systems", B.S. Publication
2. John P Uyemura ," Chip Design for Submicron VLSI", Thompson Publication.
3. Etienne Scardx, Sonia Delmas Bendhia ," Advanced CMOS cell Design :",McGraw Hill Professional .
4. K.V. K. K. Prasad, Kattula Shyamala, "VLSI Design Black Book", dreamtech Publication
5. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.

References:

1. JP Rabaey, AP Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation",Wiley,2nd Edition.
3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis and Design, McGraw-Hill, 1998.
4. Amitabha Sinha," Lecture Notes on VLSI Design", MAKAUT

CO -PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Digital VLSI Design	Learn the basics of Integrated Circuit (IC),; different Domains of VLSI design, design automation tools and the state-of-the-art VLSI circuits.	2	2	1	1	1	1
	2. To learn CMOS logic behaviour , advantages and drawbacks using static , dynamic, Domino logic and Bi-CMOS logic.	3	3	3	3	2	1
	3. To learn the basics of CMOS fabrication and Layout.	3	3	3	2	3	1
	4. Learn EDA tools and their advantages, concept of test bench, simulation, design verification, synthesis and hardware description language (Verilog/VHDL/System 'C'), the design of a 32-bit RISC CPU, Static RAM and Simulation, Synthesis & validation of the architectures on FPGA and analysis their performances.	2	2	2	2	3	1
	5. Learn the concept of Programmable Hardware and their requirements, FPGA -- architecture, configuration and design flow, concept of System on Chip (SOC), logical effort, path effort, path effort delay, path parasitic delay, designing fast circuits and multistage logic networks and the concept of delay **vs** fan out	2	3	3	3	3	1

PGVES-102: Microcontrollers and Programmable Digital Signal Processors [Sem – I] 3(L)
(36 Lectures) CREDIT-3

Faculty Name: Prof. Amitabha Sinha
Lectures: 3 hrs/week

Course Outcomes: After the completion of this course, students will learn:

CO1. The Concept of Processor Architecture, Data path Design and Control Unit (hardwired control unit, microprogrammed and nano programmed Control unit).
CO2: the Architecture and Programming model of ARM Cortex-M3 Processor/LPC l7xx Microcontroller, the concept of Interrupt with emphasize to interrupt vector, nested interrupt, Interrupt chaining, interrupt latency, interrupt controller and efficient handling of interrupts.
CO3: the concept of RISC & CISC Processors, Harvard Architecture and VLIW Architecture.
CO4: to identify and characterize architectural and programming requirements of DSP Processors and to learn the architectural details of Texas Instrument TMS320C67xx series DSP Processors.
CO5: to acquire skills on handling DSP software development platform for application development with a case study on code composer studio.

Syllabus Contents:

MODULE 1:

1**. Processor Architecture:**

i) Concept of a Computer Systems, Basic building blocks, Store and forward concept, Von-Neumann Architecture, Introduction to Processor and Processor Organization.
ii) Processor Architecture: Instruction Set Architecture: Instructions & Addressing, Procedures and Data, Instruction Set Variations. (2L)

2. Datapath Design:

i) The Arithmetic/ Logic Unit: Number Representation, Adders and Simple ALUs, Multipliers and Dividers, Floating-Point Architecture. Carry Look Ahead adders, Carry Save adder, Pipelined array multiplier, Pipelined adder.

3.Control unit Design:

i) Design of a Processor ii) Control unit Design: Hardwired Control Unit, Microprogram Controlled Unit, Nano Program Control Unit.

MODULE2:

1. **ARM Cortex-M3 Processor**:

i)Applications, Programming model - Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

ii) Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault

Exceptions, Supervisor and Pending Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

iii) LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

iv) to develop small applications by utilizing the ARM processor/LPC 17xx microcontroller.

MODULE 3:

the concept of RISC & CISC processors, limitations of Von-Neumann Architecture, Harvard Architecture and VLIW Architecture,

MODULE4:

i) **Programmable DSP (P-DSP) Processors:**

Introduction to the computational requirements of DSP algorithms, architectural structure of DSP Processors: Pipelining, need of Harvard architecture in building DSP Processors, Multiple memory units, MAC unit, circular addressing scheme, zero overhead looping, bit reversal technique, butterfly computing unit, Barrel shifters,

ii) **Introduction to TI DSP processor family:**

Architectural details of TMS320C67xx series DSP Processors, data paths, cross paths, Introduction to Instruction level architecture of C54xx family, Assembly Instructions, memory addressing, for arithmetic, logical operations.

MODULE5:

DSP software development platform: Code Composer Studio for application development On chip peripherals, Processor benchmarking

Text Books:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2ndEdition
2. John Hayes, “Computer Architecture and Organization”, McGraw Hill Publications.
3. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH ,2ndEdition.
4. Rulph Chassaing, Donald Reay,” Digital Signal Processing and Applications with the TMS320C6713 and TMS 320C6416 DSK”, Willey Student Edition.

References:

5. SlossAndrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing", Morgan KaufmanPublication.
6. Steve furber, "ARM System-on-Chip Architecture", PearsonEducation
7. Frank Vahid and Tony Givargis, 'Embedded System Design",Wiley
8. Technical references and user manuals on www.arm.com,NXP Semiconductor www.nxp.comand Texas Instrumentswww.ti.com
9. Amitabha Sinha , “ DSP – Algorithms, Architecture & Applications”, MAKAUT

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Microcontrollers and Programmable Digital Signal Processors	1. To learn The Concept of Processor Architecture, Data path Design and Control Unit (hardwired control unit, microprogrammed and nano programmed Control unit).	2	2	3	3	3	1
	2. To learn the Architecture and Programming model of ARM Cortex-M3 Processor/LPC l7xx Microcontroller, the concept of Interrupt with emphasize to interrupt vector, nested interrupt, interrupt chaining, interrupt latency, interrupt controller and efficient handling of interrupts.	2	3	3	3	3	1
	3. To learn the concept of RISC & CISC Processors, Harvard Architecture and VLIW Architecture.	2	3	3	3	3	1
	4. To identify and characterize architectural and programming requirements of DSP Processors and to learn the architectural details of Texas Instrument TMS320C67xx series DSP Processors.	3	3	3	3	3	1
	5. To acquire skills on handling DSP software development platform for application development with a case study on code composer studio.	3	3	3	3	3	1

PGVES-103: Elective I: Programming Languages for Embedded Software
[Sem – I] 3(L) (36 Lectures) CREDIT-3

Faculty Name: Mr. Sowvik Dey
Lectures: 3hrs/week

Course Outcomes:

At the end of this course, students will be able to

1. To learn about the concept of high-level programming language
2. To Write an embedded C application of moderate complexity.
3. To develop the concept about Object oriented Programming
4. To Develop and analyze algorithms in C++
5. Differentiate interpreted languages from compiled languages.

Syllabus Contents:

MODULE 1: Embedded 'C' Programming
Bitwise operations, Dynamic memory allocation, OS services Linked stack and queue, Sparse matrices, Binary tree Interrupt handling in C, Code optimization issues Writing LCD drives, LED drivers, Drivers for serial port communication Embedded Software Development Cycle Methods (Waterfall, Agile)

MODULE 2: Object Oriented Programming
Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

MODULE 3: CPP Programming: 'cin', 'cout', formatting and 110 manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

MODULE 4: Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

MODULE 5: Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch-throw, Multiple Exceptions.

MODULE 6: Scripting Languages
Overview of Scripting Languages -PERL, CGI, VB Script, Java Script, PERL: Operators, Case study: Python for Embedded system development, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation &Line Interfacing.

References:

- Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition,2008
- Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition[h]2011
- A. Michael Berman, "Data structures via C++", Oxford University Press,2002
- Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company,1999
- Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Programming Languages for Embedded Software	1. To learn about the concept of high-level programming language	1	2	2	3	3	2
	2. To Write an embedded C application of moderate complexity	1	1	2	3	3	3
	3. To develop the concept about Object oriented	1	2	2	3	3	2

	Programming						
	4. To Develop and analyze algorithms in C++	1	1	2	3	3	3
	5. Differentiate interpreted languages from compiled languages	1	1	2	3	3	2

PGVES-103: Elective I: VLSI Signal Processing
[Sem – I] 3(L) (36 Lectures) CREDIT-3

Faculty Name: Prof. Amitabha Sinha and Ms. Tania Das
Teaching Scheme
Lectures: 3hrs/week

Course Outcomes:

At the end of this course, students will be able to

CO1: acquire knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches.

CO2: acquire knowledge about retiming techniques, folding and register minimization path problems.

CO3: Ability to have knowledge about algorithmic strength reduction techniques and parallel processing of FIR and IIR digital filters.

CO4: Acquire knowledge about the architecture of the state-of-the-art DSP processor

CO5: To learn about FPGA based design and implementation of DSP algorithms.

Syllabus Contents:

Module1: Introduction to DSP systems,

Module2: Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.

Module3: Pipelined and Parallel Processing, Systolic architecture design, fast convolution, pipelined and parallel recursive filters.

Module4: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic, Scaling and round off noise

Module5: Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design.

Module6: Programmable digital signal processors: Computational requirements of DSP processor and Architecture, case studies: TI TMS320c6000 series DSP processor, FPGA architecture and implementation of DSP algorithms.

Text Books:

1.Keshab K. Parthi [A1], VLSI Digital signal processing systems, design and

implementation [A2], Wiley, Inter Science, 1999.

2.Mohammad Isamail and Terri Fiez," Analog VLSI signal and information processing", McGraw Hill,1994

3.S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

References:

1.www.cs.berkeley.edu/~pattrsn/152F97/slides/CS152_dsp.pdf

2. Bob Brodersen, "Introduction to Architectures for Digital Signal Processing" (http://infopad.eecs.berkeley.edu)

3. Mike Schulte," Application-Specific Processor Design", http://www.eecs.lehigh.edu/~mschulte/ece450-00

4. Uwe Meyer-Baese ," Digital Signal Processing with Field Programmable Gate Arrays", Springer, third edition.

5. www.ti.com , www.analog.com, www.xilinx.com

CO -PO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3	3	2	1
CO2	2	2	3	2	2	1
CO3	2	2	3	3	2	1
CO4	2	2	3	2	2	1
CO5	2	1	3	3	2	1

PGVES-104D: Elective II: CAD of Digital System
[Sem – I] 3(L) (36 Lectures) CREDIT-3

Faculty Name: Dr. Mihir Mahata
Teaching Scheme
Lectures:3 hrs/week

Course Outcomes:

At the end of this course, students will be able to

CO1: Study of design and fabrication process of VLSI Devices.

CO2: Demonstrate knowledge of computational algorithms and tools for CAD.

CO3: Study of various steps of physical design automation.

CO4: Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.

CO5: Learn circuit design using HDL.

Syllabus Contents:

Unit 1: Introduction to VLSI Methodologies - Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design.

Unit 2: VLSI design automation tools - Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

Unit 3: General purpose methods for combinational optimization - partitioning, floorplanning and pin assignment, placement, routing.

Unit 4: Simulation - logic synthesis, verification, high level Synthesis.

Unit 5 and 6: MCMS-VHDL-Verilog-implementation of simple circuits using VHDL

References:

N. A. Sherwani, "Algorithms for VLSI Physical Design Automation".

S.H. Gerez, "Algorithms for VLSI Design Automation.

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3	3	2	1
CO2	2	2	3	2	2	1
CO3	2	2	3	3	2	1
CO4	2	2	3	2	2	1
CO5	2	1	3	3	2	1

PGVES-105: Research Methodology and IPR **[Sem – I] 2(L) (25 Lectures) CREDIT-2**
Faculty Name: Prof. Shibamay Dasgupta **Teaching Scheme Lectures: l** **hrs/week**
Course Outcomes: At the end of this course, students will be able to • Understand research problem formulation. • Analyze research related information • Follow research ethics • Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity. • Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular. • Understand that IPR protection provides an incentive to inventors for further research work and investment in R &D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Syllabus Contents:

Unit 1: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.

Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Unit 2: Effective literature studies approaches, analysis Plagiarism, Research ethics,

Unit 3: Effective technical writing, how to write report, Paper; Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit 4: Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit 5: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Unit 6: New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References:

- Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
- Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
- Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
- Halbert, "Resisting Intellectual Property", Taylor &Francis Ltd,2007.
- Mayall, "Industrial Design", McGraw Hill,1992.
- Niebel, "Product Design", McGraw Hill,1974.
- Asimov, "Introduction to Design", Prentice Hall,1962.
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
- T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand,2008

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	3	2	3	2	2
CO2	1	2	3	2	2	1
CO3	2	1	3	1	2	3
CO4	2	2	2	2	2	2

CO5	**1**	**1**	**3**	**3**	**2**	**1**

PGVES-191: Digital VLSI Lab [Sem – I] 4(P) (48 Practical Hours)
CREDIT-2

Faculty Name: Mr. Sowvik Dey
Lectures: 4 hrs/week

Course Outcomes:

After the completion of this lab course students will be able to:
CO1. Be familiarized with the steps by step process involved in VLSI design and with different EDA tools (open as well as commercial)
CO2. Write program in hardware description language (HDL) like Verilog, VHDL for digital circuits and learn d verification using test bench.
CO3. Develop skill to design, simulate, synthesize and validate digital circuits on FPGA Platform using design T like Xilinx ISE / Icarus Verilog.
CO4. Develop skill to design digital circuits using VLSI design Tools like DSCH & Microwind.
CO5. Develop the skill for Layout of digital circuit using EDA tools like Cadence and Electric.

Pre-requisite: Knowledge of high-level structured programming Language (preferably 'C' and /or digital HDL), electronics.

Software & Hardware Tools –

Sl. No	Software Name / Hardware	Open Source / Purchase
1.	Xilinx ISE with iSim Simulator	Open Source Software
2.	Icarus Verilog with GTK Wave	Open Source Software
3.	DSCH and Microwind	Open Source Software
4.	Electric with LT Spice	Open Source Software
5.	FPGA Kit (Hardware)	Commercial
6.	Cadence EDA Software	Commercial

Part-A: FPGA Based Digital Design, synthesis and Validation

LAB – 1A: Introduction to FPGA Based Digital Design:
- Register-transfer-level abstraction
- Introduction to HDL Coding by Basic Digital Gates, Concept of Test Benches.
- Using Xilinx ISE Pack for HDL Coding, Simulation & Synthesis

LAB – 1B: Understanding the FPGA Board
- Identifying the Board Parts
- Procedure of Bit-Stream Downloading by Basic Digital Gates
- JTAG

LAB – 2: Writing HDL (Verilog, VHDL) Code, Test Bench for Simulation & Synthesis
- Combinational Circuit – Multiplexer, Demultiplexer, Decoder, Encoder,Half Adder, Full Adde Subtractor, Full Subtractor, Adder- Subtractor.

- Combinational Circuit – Ripple Carry, Carry look ahead adder
- Construction of Higher Level Multiplexer using Lower Level Multiplexer
- Circuit Designing using universal logic: Multiplexer

LAB – 3: Writing HDL (Verilog, VHDL) Code, Test Bench for Simulation & Synthesis

- Sequential Circuit –
- Flip-Flop – SR, D, JK, T
- Counter – Up, Down, Bidirectional, Ring, Ripple, Johnson, Mod-N.
- Register – Left/Right Shift Register, Construction of Memory.
- FSM – Mealy & Moore

LAB – 4: Writing Verilog Code, Test Bench for Simulation & Synthesis

1. ALU Design 2. A 12-bit CPU Design 3.FFT Processor Design

Part-B: Lab assignments with VLSI Design Automation tool (Cadence, DSCH and Microwind) for Layout Design.

LAB – 5: Lab assignments with Cadence, DSCH, Microwind:

- Familiar with VLSI Design Tools like:**Cadence, DSCH , Microwind**.
- Study and Validation of the behavior of the basic logic Gates on DSCH schematic window and Extra layouts using Microwind.
- Study and Validation of the behavior of Combinational logics a) Full adder using half adder, b)full sub using half subtractor c) Binary adder sub tractor circuit and d) Ripple carry adder circuit on DSCH sch window and Extract the layout using Microwind.

LAB – 6: Lab assignments with Cadence and Micro wind:

- Study and Validation of the behavior of a) Parity checker circuit, b) 2:4 decoder circuit, c) the 4:1 mux using 2:1 mux circuit and d) 1 bit comparator circuit on DSCH schematic window and extract the layout Microwind.
- Study and Validation of the behavior of 2:1 mux as a universal logic on DSCH schematic window and extract their layouts using Microwind.

LAB – 7: Lab assignments with DSCH and Microwind:

- Study and Validation of the behavior of Sequential logics a) Flip-flops: S-R, D, J-K, T b)Register c) C Ripple, Ring, Up, Down, Mod-N Counter circuit on DSCH schematic window and Extract the layou Microwind.

LAB – 8: Lab assignments with DSCH and Microwind:

- Study and Validation of the behavior of a) CMOS inverter circuit and b) CMOS- NOR circuit c) CMO circuit and d) CMOS Combinational circuit on DSCH schematic window and extract the layout using Microwind.

Part-C: Lab assignments with Cadence, Electric

LAB – 9: Lab Assignments with Cadence, Electric:

- Familiar with Schematic design and test using Electric.
- Study and Validation of the behavior of the basic Gates on Electric schematic window and Extract their using Electric.
- Study and Validation of combinational logic such as a) full adder using half adder, b) Full subtractor circuit, c) Ripple carry adder circuit, d) Binary adder subtractor circuit and e) Parity checker circuit and extract the layout using Cadence, Electric.

LAB – 10: Lab Assignments with Cadence, Electric:

- Study and Validation of a) 2:4 decoder circuit and b) 4:1 mux using 2:1 mux circuit, c) 1 bit comparator circuit and extract the layout using electric.
- Study and Validation of the behavior of 2:1 mux as a universal logic and extract the layout using

Cadence, Electric.

LAB – 11: Lab Assignments with Cadence, Electric:

- Study and Validation of Sequential logics a) Flip-flops: S-R, D, J-K, T b) Register c) Counter and Extr layout using electric
- Learn to design and test of a) CMOS inverter b) CMOS-NAND, c) CMOS-XOR and CMOS Combinational circuit and extract the layout using Cadence, Electric.

Text Books:

1. Advanced Digital Design using Verilog-HDL, Michael. D. Ciletti, PHI publications.
2.Carver Mead, Lynn Conway, Introduction to VLSI Systems", B.S. Publication
3.John P Uyemura," Chip Design for Submicron VLSI", Thompson Publication.
4. Etienne Scard., Sonia Delmas Bendhia," Advanced CMOS cell Design:", McGraw Hill Professional

References:

1.K.V.K.K. Prasad, Kattula Shyamala, "VLSI Design Black Book", dreamtech Publication
2.Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition1.
3.Amitabha Sinha, "Lecture Notes on VLSI Design", MAKAUT

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Digital VLSI Lab	CO1. be familiarized with the steps by step process involved in VLSI design and with different EDA tools (open source as well as commercial)	1	2	3	2	3	2
	CO2. Write program in hardware description language (HDL) like Verilog, VHDL for digital circuits and learn design verification using test bench.	1	3	2	2	3	2
	CO3. develop skill to design, simulate, synthesize and validate digital circuits on FPGA Platform using design Tools like Xilinx ISE / Icarus Verilog.	1	2	2	2	3	2
	CO4. Develop skill to design digital circuits using VLSI design Tools DSCH & Microwind.	1	2	2	2	3	2
	CO5. Develop the skill for Layout of digital circuit using EDA tools like Cadence and Electric.	1	2	2	3	3	2

PGVES-192: Microcontrollers and Programmable Digital Signal Processors Lab [Sem – I]
4(P) (48 Practical Hours) CREDIT-2

Faculty Name: Mr. Sowvik Dey
Teaching Scheme
Lectures: 4 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
2. Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

List of Assignments:

A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool-chain

1. Blink an LED with software delay, delay generated using the SysTicktimer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGBLED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

B) Experiment s to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2	3	3	2	2
CO2	1	2	3	2	2	2

CO3	**3**	**2**	**2**	**3**	**2**	**3**
CO4	**2**	**2**	**3**	**2**	**2**	**3**
CO5	**2**	**1**	**3**	**2**	**2**	**1**

Semester II

PGVES-201: Analog VLSI Design **[Sem – II] 3(L) (36 Lectures) CREDIT-3**
Faculty Name: Dr. Mihir Mahata **Teaching Scheme** **Lectures: 3 hrs/week**

Sl. No	Module Name and Topics
1	**Introduction:** Motivation for analog VLSI and mixed signal circuits in CMOS technologies and issues thereof.
2	**CMOS device fundamentals:** Basic MOS models, device capacitances, parasitic resistances, substrate models, transconductance, output resistance, f_T, frequency dependence of device parameters.
3	**Single stage amplifiers, Differential Amplifiers:** Common source amplifier, source degeneration, source follower, common gate amplifier, cascade stage. Basic differential pair, common mode response, differential pair with MOS loads, Gilbert Cell, device mismatch effects, input offset voltage.
4	**Current Mirrors, Current and Voltage Reference:** Basic current mirrors, cascode current mirrors, active current mirrors, low current biasing, supply insensitive biasing, temperature insensitive biasing, impact of device mismatch.
5	**Frequency Response of Amplifiers, Feedback:** Miller effect, CS amplifier, source follower, CG amplifier, cascade stage, differential amplifier, Multistage amplifier. Feedback topologies, effect of load, modeling input and output ports in feedback circuits.
6	**Operational Amplifiers:** Performance parameters, One-stage and two-stage Op Amps, gain boosting, comparison, common mode feedback, input range, slew rate, power supply rejection, noise in Op Amps.

7	**Other Sub-circuits**, **Field Programmable Analog array (FPAA):** Comparators; AD & DA conversion; Switched-mode circuits – principle of operation. Concept of switch capacitor, Configurable analog block (CAB), Basic concept of FPAA, Architecture of FPAA, EDA tools, Application of FPAA.

References:

- J P Rabaey, A P Chandrakasan. B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2ndEdition.
- Baker, L Boyce, "CMOS Circuit Design. Layout, and Simulation", Wiley, 2ndEdition.
- Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH,2007.
- Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rdEdition.
- R J Baker, "CMOS circuit Design. Layout and Simulation", IEEE Inc.,2008.
- Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH,3rdEdition.
- Pucknell, D.A. and Eshraghian. K.,'Basic VLSI Design", PHI, 3rdEdition.

COURSE OUTCOME(CO)

After completion of this course students are able

1. Learn circuit design technique and design issues in CMOS technologies.
2. Gain knowledge of basic MOS models, device capacitances, parasitic resistances, transconductance, up to frequency dependence of device parameters.
3. Understand the significance of different biasing styles and apply them aptly for different circuits.
4. Design basic building blocks like sources, sinks, mirrors, up to layout level, become capable with computer skills (e.g., LT spice) for the design and analysis of circuits.
5. Comprehend the design and analysis of MOS Op-Amp circuits and systems, identify suitable topologies of the constituent sub systems and corresponding circuits as per the specifications of the system.

CO -PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3	3	2	1
CO2	2	2	3	2	2	1
CO3	2	2	3	3	2	1
CO4	2	2	3	2	2	1
CO5	2	1	3	3	2	1

Department: Embedded Systems and VLSI Design	**Session:**2021-2023
Year:1st	**Semester:** II
Course Name: VLSI Design Verification and Testing	**Course Code:** PGVES202
Contact: 3L+1T / Week	**Target Student:** PG
	Name of the faculty: Mr. Sabyasachi Sen
	Credit: 3

PGVES-202: VLSI Design Verification and Testing [Sem – II]
3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes:

At the end of this course, students will be able to:

- Familiarity with the Front-end design, verification techniques and reusable test environments.
- Test and verify increasingly complex designs more efficiently and effectively using EDA tools
- Develop test bench environment for Design under Test
- Summarize the System Verilog assertions
- Describe the applications of randomization techniques

Syllabus Contents:

Module 1: Basic concept of Testing &Verification and their differences, Automatic Testing equipment., testing in different stages of manufacturing, Design verification, chip yield, system level operation and testing, different testing algorithms,

Module 2: EDA tools for testing, Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse,Testbench performance.

Module3:

Procedural statements and routines: tasks, functions and void functions, Routine arguments, returning from a routine, Local data storage, Time values Connecting the test bench and design: Separating the test bench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

Module4: Randomization, what to randomize, Randomization in System Verilog, Constraint details solution probabilities, controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre-randomize and post-randomize functions,

Module 5: Concept of Automatic Test pattern Generation (ATPG), Fault coverage, Fault models, Stuck-
at -1, stuck-at-0 faults, transistor faults, collapsed faults, bridging faults, Delay Faults and Crosstalk, pattern sensitivity and coupling faults. Automatic Test Pattern Generation (ATPG):

Algorithms for generating sequence of test vectors for a given circuit based on specific fault models,

Fault analysis and Simulation to emulate fault models in CUT and application of test vectors to determine fault coverage: Parallel, deductive, and concurrent fault simulation, Design for testability, Scan, Built-in self-test, Pseudo random number generator, Automatic Test Generation, Built in Logic Block observer (BILBO).

Module 6: Boundary Scan, JTAG (IEEE standard 1149.1) concept, Architecture and Instruction set and
Boundary Scan TAP control operation ,testing process using JTAG(IEEE1149.4) for testing of Analog and Mixed signal VLSI circuits, Differences from digital testing, Test procedures, DSP based mixed signal test, Test plan, Boundary Scan Architecture & instruction Set of Mixed Signal Testing (IEEE1149.4) and test Process, Standard Analog Test Bus (ATB), Basic Mixed Signal Chip structure IEEE 1149, Digital/Analog Interfaces, Analog test access Port, Test Bus Interface circuit (TBIC), TBIC Switching Patterns, Chaining of 1149.4 compliance ICs.

Text Books:

1. N. K. Jha et.al., "Testing of Digital Systems"
2. M L Bushnell and V D Agrawal. "Essentials of Electronic Testing"
3. M Abramovici and A D Friedman. " Digital Systems Testing and Testable Design"
4. M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005.
5. M. Abramovici, M. Breuer, and A. Friedman, *Digital System Testing and Testable Design*, IEEE Press, 1994

References:

1.Chris Spears, "System Verilog for Verification", Springer,2nd Edition
2.M. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers
3.IEEE 1800-2009 standard (IEEE Standard for System Verilog— Unified Hardware Design Specification, and Verification Language).
4. Amitabha Sinha, "Lecture notes on Testing & Verification of VLSI circuits", MAKAUT.
5. H. Fujiwara, *Logic Testing and Design for Testability*, MIT Press, 1985

CO-PO Mapping

Subject	Course Outcomes	POs					
		1	2	3	4	5	6
VLSI Design Verification and Testing	1. Familiarity with the Front-end design, verification techniques and reusable test environments.	2	1	2	2	2	3

	2.Test and verify increasingly complex designs more efficiently and effectively using EDA tools	2	1	2	2	2	3
	3.Develop test bench environment for Design under Test	2	1	2	3	2	3
	4. Summarize the System Verilog assertions	1	1	2	2	2	2
	5. Describe the applications of randomization techniques	2	1	2	3	2	2

PGVES-203: Elective III: Low Power VLSI Design
[Sem – II] 3(L) (36 Lectures) CREDIT-3

Faculty Name: Dr. Ria Bose and Ms. Tania Das
Teaching Scheme Lectures: 3hrs/week

Course Outcomes:

At the end of the course, students will be able to:

- CO 1: Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- C02: Characterize and model power consumption & understand the basic analysis methods.
- C03: Understand leakage sources and reduction techniques
- CO4: Analyze and design various types of low power adders
- CO5: Understand about the low power memory design

Syllabus Contents:

Unit 1: Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of V_{dd} & Vt on speed, constraints on V_t reduction, transistor sizing & optimal gate-oxide thickness, impact of technology scaling, technology innovations.

Unit 2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit 3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver vs. distributed buffers, buffers & device sizing under process variations, zero skew vs. tolerable skew, chip & package co-design of clock network.

Unit 4: Low power SoC design *I* Digital system,

- Design synergy, Low power system perspective-power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit 5: Low Power Memory Design: Sources &reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Unit 6: Low Power Microprocessor Design System: power management support, architectural trade-offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power &performance.

References:

- P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
- Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wileysonslnc., 2000.
- J. B. Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
- A. P. Chandrasekaran and R. W. Broadersen, "Low power digital CMOS design", Kluwer, 1995

CO/PO Mapping

Cos	Program Outcome (PO)					
	PO1	PO 2	PO 3	PO4	PO 5	PO6
CO1: Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.	3	2	2	3	2	2
CO2: Characterize and model power consumption & understand the basic analysis methods.	3	2	2	1	1	3
CO3: Understand leakage sources and reduction techniques	2	2	3	2	1	1
CO4: Analyze and design various types of low power adders	3	2	2	3	2	1
CO5: Understand about the low power memory design	1	2	2	3	3	3

PGVES-204 : Elective IV : Introduction to AI , Machine Learning and Applications
[Sem – II] 3(L) (36 Lectures) CREDIT-3

Teaching Scheme
Lectures: 3 hrs/week

Course Outcomes:

CourseOutcomes:

At the end of the course, students will be able to:

CO1: Learn the basic concept of Artificial Intelligence, Machine Learning , Neural network and their inter-relations different AI techniques

CO2: Learn the concept of Knowledge Representation and knowledge representation issues and the concept of Logic programming.

CO3: Learn the basic concept of Biological Network and modelling of Artificial Neural Network.

CO4: Learn the concept of Machine Learning and different types of Machine Learning Network

CO5: Learn the Architecture of Convolutional Neural Network (CNN) & it's application to Image classification and VLSI implementation of Machine Learning Engine.

SyllabusContents:

MODULE 1: Introduction to AI, Machine Learning, Deep Learning and Neural Network and their inter relation, Machine Learning vs Neural Network and key differences,

The AI Problems, The Underlying Assumption, AI Techniques, Level of The Model, Criteria For Success, Some General References, One Final Word Problems, State Space Search & Heuristic Search Techniques: Defining The Problems as aStateSpaceSearch,ProductionSystems,ProductionCharacteristics,ProductionSystemCharacteristics, Issues In The Design Of Search Programs, Additional Problems. Generate-And-Test, Hill Climbing, Best-First search and Breadth-first Search, \ Problem Reduction, Constraint Satisfaction, Means-Ends Analysis.

MODULE 2:

Knowledge Representation Issues: Representations And Mappings, Approaches To Knowledge Representation. Using Predicate Logic: Representation Simple Facts In Logic, Representing Instance

And Isa Relationships, Computable Functions And Predicates, Resolution. Representing Knowledge Using Rules: Procedural Versus Declarative Knowledge ,Logic Programming, Forward Versus Backward Reasoning.

MODULE 3:

Symbolic Reasoning under uncertainty: Introduction To Nomonotonic Reasoning, Logics For Non-monotonic Reasoning. Statistical Reasoning: Probability And Bays 'Theorem, Certainty Factors And Rule-Base Systems, Bayesian Networks, Dempster Shafer Theory

MODULE4:

Concept and structure and functions of Biological Neuron, introduction to function of Human Brain, Characteristics of Biological Neural Network, Introduction to Artificial Neural Network (ANN), Non-Linear Characteristics, model of an Artificial Neural Network, Properties of ANN, Layers and structures of ANN, Forward and Back Propagation NN, Different Activation Functions,

MODULE 5:
Concept of Learning, Machine Learning and key elements, Different types of machine Learning: Supervised learning Unsupervised learning, Semi-supervised learning, Reinforcement learning, Adaptive Learning, Difference between traditional programming and machine Learning. Deep Learning Network, Concept of Convolution and Convolutional Neural Network (CNN), Layers of CNN: Pooling Layer, Max Pooling Layer, Global average Pooling Layer, Normalization Layer, Fully-Connected Layer , Converting Fully Connected Layers to Convolutional Layers, different Activation Layers.

MODULE 6:

Architecture of CNN: Layer Patterns ,Layer Sizing Patterns , Image Classification using CNN: CNN Architecture of Image Classification ,concept of activation Layer RELU ,Details about CNN, Stages of CNN, concepts of Filters, Stride, Padding, Filter hyperparameters, Parameter Sharing
Filter Activations: Feature maps, Soft Max Function, Computational considerations.
Efficient Hardware Realization for Neural Networkof CNN, Reconfigurable VLSI Architecture of CNN, Concept and need of Reconfigurability, VLSI AI Engines to Provide Compute Density for
Machine Learning, Case studies (Xilinx AI engine), Concept of" Near Memory Computing" and Analog VLSI for implementing Machine Learning Systems, Neural Network training using Analog Memory, State-of-the-art Analog Deep Machine Learning Systems.

Text Books:

1.Elaine Rich and Kevin Knight "Artificial Intelligence", 2nd Edition, Tata McGraw-Hill, 2005.

2.StuartRusselandPeterNorvig,"ArtificialIntelligence:AModernApproach",3rdEdition,PrenticeHall,2009

References:

1. Amitabha Sinha , " AI. Machine Learning & Applications in Image Classifications", MAKAUT

2. Jianxin Wu ,"Introduction to Convolutional Neural Networks", LAMDA Group National Key Lab for Novel Software Technology Nanjing University, China wujx2001@gmail.com May 1, 2017 (https://cs.nju.edu.cn/wujx/paper/CNN.pdf)
3.https://towardsdatascience.com/an-introduction-to-convolutional-neural-networks-eb0b60b58fd7
4.Himadri Sankar Chatterjee,"A Basic Introduction to Convolutional Neural Network",https://medium.com/@himadrisankarchatterjee/a-basic-introduction-to-convolutional-neural-network-8e39019b27c4

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Introduction to AI , Machine Learning and Applications	CO1. Learn the basic concept of Artificial Intelligence, Machine Learning , Neural network and their inter-relations different AI techniques	2	2	3	2	3	2
	CO2. Learn the concept of Knowledge Representation and knowledge representation issues and the concept of Logic programming.	1	2	3	2	3	2
	CO3: Learn the basic concept of Biological Network and modelling of Artificial Neural Network.	1	2	2	2	3	2
	CO4: Learn the concept of Machine Learning and different types of Machine Learning Network	1	2	2	3	3	2
	CO5: Learn the Architecture of Convolutional Neural Network (CNN) & it's application to Image classification and VLSI implementation of Machine Learning Engine.	1	2	3	3	3	2

PGVES-291 Teaching: Analog VLSI Design lab [Sem – II] 0(L) 2(T) 2(P) (36 Practical Hours) (CREDIT-2)

Faculty Name: Dr. Mihir Mahata
Contact hours: 3 hrs/week

Course Objective:

1. Student will be familiar about VLSI Tools like LTSpice and cadence virtuoso for Schematic and Layout design.
2. Student will be able to design circuit on cadence virtuoso using the schematic editor window. They will be able to simulate circuit by launching ADE-L in the schematic editor window.
3. Student will be able to do transient, dc and ac analysis.
4. Student will be able to do circuit verification. The layout for the schematic has to be prepared using Layout-XL, and the same has to be physically verified.

Course Outcomes:

After completion of this course students are able to
CO1. Familiar about VLSI Tool like cadence virtuoso.
CO2. Design analog circuit using schematic editor window and also able to test the design.
CO3. Extract the Layout of analog circuits and CMOS circuits using Layout-XL, familiar about
CO4. Do transient, dc and ac analysis of the designed circuit using cadence virtuoso.
CO5. Understand the DRC check, LVS and RC Extraction, familiar about LT-Spice Tool
Pre-requisite: Knowledge of Analog electronics and high-level structured programming Language (preferably 'C').

Software & Hardware Tools –

Sl. No	Software Name / Hardware	Open Source / Purchase
1.	LT-Spice	Open Source Software
2.	Scilab	Open Source Software
3.	Cadence EDA Software	Commercial
4.	FPGA Kit (Hardware)	Commercial

List of Lab Assignments:

List of Lab assignments with LT-Spice and cadence virtuoso:

2. i) Familiar with VLSI Design Tools like: LT-Spice and cadence virtuoso.
   ii) Design the schematic of an Inverter using **cadence virtuoso** and verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

3. Design and simulate the schematic of the common source amplifier. And verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

4. Design and simulate the schematic of the common drain amplifier, and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

5. Design and simulate the schematic of a stage differential amplifier and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

6. Design and simulate the schematic of the operational amplifier and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

7. Design and simulate the schematic of the of cascode current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

8. Design and simulate the schematic of Wilson current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

9. Using LT Spice design and simulate a switched capacitor Amplifier. Perform the DC Analysis and Transient Analysis.

10. Design a mixed signal circuit. Implement the circuit in FPAA.

Text:

1 CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford)

Reference:

1. Weste N and Eshraghian K; Addision Wesley 1985, *Principles of CMOS VLSI Design*
2. Mukherjee A, 1986, *Introduction to NMOS and CMOS VLSI Systems Design*, Prentice-Hall
3. Mead and Conway, *Introduction to VLSI Systems*, Notes: Addison Wesley D C & Co

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Analog VLSI Design lab	CO1. Familiar about VLSI Tool like cadence virtuoso.	2	2	3	2	3	2
	CO2. Design analog circuit using schematic editor window and also able to test the design.	1	2	3	2	3	2
	CO3. Extract the Layout of analog circuits and CMOS circuits using Layout-XL.	1	2	2	2	3	2
	CO4. Do transient, dc and ac analysis of the designed circuit using cadence virtuoso.	1	2	2	3	3	2
	CO5. Understand the DRC check, LVS and RC Extraction, familiar about LT-Spice tool	1	2	3	3	3	2

Department: Embedded Systems and VLSI Design **Year:1st** **Course Name: VLSI Design Verification and Testing Lab** **Contact:** 3L+1T / Week	**Session:**2021-2023 **Semester:** II **Course Code:** PGVES292 **Target Student:** PG **Name of the faculty: Mr. Sabyasachi Sen, Mr. Sowvik Dey, Dr. Ria Bose** **Credit:** 2

Teaching Scheme
Lectures: 4 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Verify increasingly complex designs more efficiently and effectively.
- Analyze the use of procedural statements and routines in testbench design with system verilog.
- Apply randomization concepts in designing testbench.
- Understand the use of multi-threading and inter-process communication in testbench design.
- Interface a system verilog testbench with system C.

List of Assignments:

I. Sparse memory
2. Semaphore
3. Mailbox
4. Classes
5. Polymorphism
6. Coverage Assertions

CO-PO Mapping

Subject	Course Outcomes	POs					
		1	2	3	4	5	6
VLSI Design Verification and Testing Lab	1. Verify increasingly complex designs more efficiently and effectively.	**2**	**1**	2	3	3	3
	2. Analyze the use of procedural statements and routines in testbench design with system verilog.	**2**	**1**	**2**	2	2	3
	3. Apply randomization concepts in designing testbench.	**2**	**1**	**2**	3	2	3
	4. Understand the use of multi-threading and inter-process communication in testbench design.	**1**	1	**2**	2	2	2
	5. Interface a system verilog testbench with system C.	2	1	2	2	3	**2**

Semester III

Department: Embedded Systems and VLSI Design **Year:2nd** **Course Name:** Selected topics in Mathematics **Contact:** 3L+1T / Week	**Session:**2021-2023 **Semester:** III **Course Code:** PGVES301 **Target Student:** PG **Name of the faculty: Dr. Ria Bose and Ms. Tania Das** **Credit:** 3

Syllabus Contents:

Module-1:

Laplace Transform and solving differential equations and applications to electric circuit analysis.

Fourier series and Transform: Revision of Fourier series, integrals and transforms and their properties. The Two-dimensional Fourier transform, convolution theorem, Parseval's formula, discrete fourier transform, fast fourier transform.

Z-transforms: sequence, representation of sequence, basic operations on Sequences, z transforms, properties of z transforms, change on scale, shifting Property, inverse z transform, solution of difference equations, region of Convergence, bilinear (s to z) transform, difference among Laplace and Z transforms.

Walsh function and Hadamard transform: generating walsh functions of Order n, characteristics and applications of walsh function, Hadamard Matrix, properties, fast Hadamard transform, applications

Module-2: Probability and Statistics:

- Definitions, conditional probability, Bayes Theorem and independence.
- Random Variables: Discrete, continuous and mixed random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality.

Module-3: Special Distributions: Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions.

- Pseudo random sequence generation with given distribution, Functions of a Random Variable

Module-4: Joint Distributions: Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution.

- Stochastic Processes: Definition and classification of stochastic processes, Poisson process
- Norms, Statistical methods for ranking data

Module-5: Multivariate Data Analysis

- Linear and non-linear models, Regression, Prediction and Estimation
- Design of Experiments – factorial method
- Response surface method

Module-6: Graphs and Trees:

- Graphs: Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graph colouring.

Module-7: Trees: Rooted trees, path length in rooted trees, binary search trees, spanning trees and cut set, theorems on spanning trees, cut sets, circuits, minimal spanning trees, Kruskal 's and Prim's algorithm

References:

- Henry Stark, John W. Woods, "Probability and Random Process with Applications to Signal Processing", Pearson Education, 3rdEdition
- C. L. Liu, "Elements of Discrete Mathematics", Tata McGraw-Hill, 2"dEdition
- Douglas C. Montgomery, E.A. Peck and G. G. Vining, "Introduction to Linear Regression Analysis", John Wiley and Sons,2001.
- Douglas C. Montgomery, "Design and Analysis of Experiment s", John Wiley and Sons, 2001.
- B. A. Ogunnaike, "Random Phenomena: Fundamentals of Probability and Statistics for Engineer s", CRC Press,2010.

Course Outcomes:

At the end of the course, students will be able to:

- Characterize and represent data collected from experiments using statistical methods.
- Model physical process/systems with multiple variables towards parameter estimation and prediction.
- Represent systems/architectures using graphs and trees towards optimizing desired objective.
- Provide knowledge of a wide range of mathematical techniques and application of mathematical methods/tools in other scientific and engineering domains.
- Provide advanced knowledge on topics in pure mathematics, empowering the students to pursue higher degrees at reputed academic institutions.

CO-PO Mapping

Subject	Course Outcomes	POs					
		1	2	3	4	5	6
Selected Topics in Mathematics	1. Characterize and represent data collected from experiments using statistical methods.	1	1	1	1	1	1
	2. Model physical process/systems with multiple variables towards parameter estimation and prediction.	2	1	2	2	3	2
	3. Represent systems/architectures using graphs and trees towards optimizing desired objective.	1	1	1	1	1	1
	4.Provide knowledge of a wide range of mathematical techniques and application of mathematical methods/tools in other scientific and engineering domains.	2	2	2	1	2	1
	5.Provide advanced knowledge on topics in pure mathematics, empowering the students to pursue higher degrees at reputed academic institutions.	2	2	2	2	1	3

Department: Embedded Systems and VLSI Design **Year:**2nd **Course Name: Cost** Management of Engineering Project **Contact:** 3L+1T / Week	**Session:**2021-2023 **Semester:** III **Course Code:** PGVES302 **Target Student:** PG **Name of the faculty: Dr. Ria Bose and Ms. Tania Das** **Credit:** 3

Pre-requisites: Basic concept of Management

UNIT-I INTRODUCTION Classes: 09 Introduction and Overview of the Strategic Cost Management Process.

UNIT-II COST CONCEPTS Classes: 09 Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision Making.

UNIT-III PROJECT MANAGEMENT Classes: 09 Project: meaning, Different types, why to manage, cost overruns centers, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents. Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process.

UNIT-IV COST BEHAVIOR AND PROFIT PLANNING Classes: 09 Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement, Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT-V QUANTITATIVE TECHNIQUES Classes: 09 Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation Problems, Assignment problems, Simulation, Learning Curve Theory.

Text Books:
1. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting.
2. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

Reference Books:
1. Cost Accounting: A Managerial Emphasis, Prentice Hall of India, New Delhi.
2. Charles T. Horngren and George Foster Advanced Management Accounting.
3.Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher.

COURSE OUTCOME(CO)

After completion of this course students are able

1. Understand the concept of strategic cost management, strategic cost analysis – target costing, life cycle costing and Kaizen costing and the cost drive concept.
2. Describe the decision-making; relevant cost, differential cost, incremental cost and opportunity cost, objectives of a costing system.
3. Understand the meaning and different types of project management and project execution, detailed engineering activities.
4. Understand the project contracts, cost behaviour and profit planning types and contents, Bar charts and Network diagram.
5. Analyze by using quantitative techniques for cost management like PERT/CPM.

CO-PO Mapping

Subject	Course Outcomes	POs					
		1	2	3	4	5	6
Cost Management Of Engineering Project	1. Understand the concept of strategic cost management, strategic cost analysis – target costing, life cycle costing and Kaizen costing and the cost drive concept.	1	1	1	1	1	1
	2. Describe the decision-making; relevant cost, differential cost, incremental cost and opportunity cost, objectives of a costing system.	1	1	1	1	1	1
	3. Understand the meaning and different types of project management and project execution, detailed engineering activities.	3	1	2	1	1	2
	4.Understand the project contracts, cost behaviour and profit planning types and contents, Bar charts and Network diagram.	2	3	2	1	1	1
	5. Analyze by using quantitative techniques for cost management like PERT/CPM.	2	3	2	1	1	2