MAULANA ABUL KALAM AZAD
UNIVERSITY OF TECHNOLOGY,
WEST BENGAL

THE DEPARTMENT OF
MICROELECTRONICS AND VLSI TECHNOLOGY

SYLLABUS

FOR POST GRADUATE DEGREE COURSE (M.Tech)

IN

Microelectronics and VLSI Technology

VISION OF THE UNIVERSITY

To achieve the status of a globally ranked premier University in the field of Science, Technology, Pharmacy, Architecture, Management, and interdisciplinary areas for the creation of high-caliber professionals with environmental consciousness, social, moral, and ethical values along with the competency to face the new challenges of rapid technological advancements.

MISSION OF THE UNIVERSITY

To impart quality and value-based teaching & learning of international standards for solving the real-life problems

- To create and disseminate knowledge both nationally & internationally towards the transformations of the civilization into a knowledge-based society
- To institutionalize the extension and field outreach activities with a view to transforming the university system into an active instrument for social change
- To develop liaison and collaboration with globally recognized academic institutions in order to inject new and fresh thinking into teaching, learning, and research
- To generate intellectually capable and imaginatively gifted professionals and successful entrepreneurs having environmental consciousness and ethics who can work as an individual or in a group in multi-cultural global environments for continuing significantly towards the betterment of the quality of human life.

The vision of the Department of Microelectronics and VLSI Technology

The Department of Microelectronics and VLSI Technology envisions being a leader in pursuit of knowledge and wisdom for the holistic development of the rapid technological advancements of society in multi-disciplinary areas through excellence in teaching, training, and research and aspires to meet the global and socio-economic challenges of the state as well as a country.

Mission statements of the Department of Microelectronics and VLSI Technology (MS)

MS-1: To participate in the Special Man Power Development Program to meet the ever-challenging issues in the field of Microelectronics and VLSI Technology

MS-2: To enable the students to formulate, design, and solve problems in applied science and engineering.

MS-3: To provide excellent teaching and research environment using state-of-the-art facilities.

MS-4: To provide adequate support in developing knowledge-based skills to meet the requirements of the Microelectronics, Embedded Systems, & VLSI industry.

MS-5: To develop a positive attitude among students to participate in collaborative research work.

Program Educational Objectives (PEOs)

PEO-1: Gain the ability to analyze, design, and implement VLSI Systems. Learn to apply modern skills, techniques, and engineering tools to create VLSI Devices, Circuits and Systems.
PEO-2: Understand the state of the art in the recent areas of research and to formulate problems from them and perform original work to contribute in the advancement of Microelectronics and VLSI Technology.
PEO-3: To learn different process steps involved in the fabrication of ICs.
PEO-4: To offer training on full cycle development of Device design and itd fabrication using Electronic Design Automation (EDA) tool.
PEO-5: To train students in analytical reasoning, experimental skills and attitude to collaborate between inter-disciplinary research groups.

Mapping Program Educational Objectives (PEOs) with Mission Statements (MS)

	MS-1	MS-2	MS-3	MS-4	MS-5
PEO-1	3	3	3	3	1
PEO-2	3	3	3	3	1
PEO-3	2	3	3	3	2
PEO-4	2	2	3	3	1
PEO-5	2	3	2	2	2

Note: '3' in the box for high-level mapping, 2 for Medium-level mapping, and 1 for 'Low-level' mapping.

Program Outcomes (POs)

After completion of this M.Tech program, the students will be able to
PO-1. Independently carry out research /investigation and development work to solve practical problems

PO-2. Write and present a substantial technical report/document.

PO-3. Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program

PO-4. Achieve conceptual knowledge-based skill to meet the man-power demand of upcoming semiconductor IC Design & Fabrication Industry.
PO-5. Apply the knowledge in analysing the cutting-edge problems of Microelectronics, VLSI Device and Technology for their implementation in future integrated circuits.
PO-6. Acquire professional and intellectual integrity and ethics of research for the requirement of sustaining in the advance Academics or Industry.

Program Specific Outcomes (PSOs)

PSO-1: Achieve conceptual knowledge-based skill to meet the man-power demand of upcoming semiconductor IC Design & Fabrication Industry.
PSO-2: Apply the knowledge in analysing the cutting-edge problems of Microelectronics, VLSI Device and Technology for their implementation in future integrated circuits.
PSO-3: Acquire professional and intellectual integrity and ethics of research for the requirement of sustaining in the advance Academics or Industry.

Mapping of Program Outcomes (POs) and Program Specific Outcomes (PSOs)

with Program Educational Objectives (PEOs)

	PEO-1	PEO-2	PEO-3	PEO-4	PEO-5
PO-1	3	3	3	2	3
PO-2	1	3	2	2	3
PO-3	2	2	2	1	2
PO-4	3	3	2	3	3
PO-5	2	3	3	3	2
PO-6	2	2	2	2	3
PSO-1	3	3	2	3	3
PSO-2	2	3	3	3	2
PSO-3	2	2	2	2	3

Note: '3' in the box for 'high-level'mapping, 2 for 'Medium-level'mapping, 1 for 'Low-level' mapping.

Semester-wise Course Schedule

Semester – I

SL. NO.	CODE	PAPER NAME	L	T	P	MARKS	CREDIT POINTS
1.	**PGMVD-101**	Advanced Engineering Mathematics	3	1	0	100	4
2.	**PGMVD-102**	Physics Of VLSI Devices	3	1	0	100	4
3.	**PGMVD-103**	Processor Architecture & SOC Design	3	1	0	100	4
4.	**PGMVD-104**	Microelectronics Technology	3	1	0	100	4
5.	PGMVD-105	Digital VLSI Circuits & Systems	3	1	0	100	4
		Total Theory				**500**	**20**
6.	PGMVD-191	Microelectronics Lab-I	0	0	3	100	2
7.	PGMVD-192	VLSI Design - Lab-I	0	0	3	100	2
8.	PGMVD-193	Seminar – Review of current research Papers				100	2
		Total Practical and Sessional				**300**	**6**
		Total				800	26

Semester – II

SL. NO.	CODE	PAPER NAME	L	T	P	MARKS	CREDIT POINTS
1.	**PGMVD-201**	Analog VLSI Circuits & Systems	3	1	0	100	4
2.	**PGMVD-202**	**Testing & Verification of Digital Systems**	3	1	0	100	4
3.	**PGMVD-203**	A: Digital Signal Processing and Application B. Advanced communications System	3	1	0	100	4
4.	**PGMVD-204**	Advanced Micro & Nano Devices	3	1	0	100	4
5.	PGMVD-205	Project Management	3	1	0	100	4
		Total Theory				**500**	**20**
6.	PGMVD-291	Micro Electronics Lab-II	0	0	3	100	2
7.	PGMVD-292	VLSI Design Lab-II	0	0	3	100	2
8.	PGMVD-293	Term paper leading to Thesis			2	100	2
		Total Practical and Sessional				300	6
		Total				**800**	**26**

Semester – III

SL. NO.	CODE	PAPER NAME	L	T	P	MARKS	CREDIT POINTS
1.	**PGMVD-301**	A. Operating System B. Computer Organization C. Algorithms	3	1	0	100	4
		Total Theory				**100**	**4**
2.	PGMVD-391	Project Part-I	0	0	4	100	4
3.	PGMVD-392	Project Defense				100	4
4.	PGMVD-393	Group Project	0	0	4	100	4

		Total Sessional				300	12
		Total				**800**	**16**

Semester – IV

SL. NO.	CODE	PAPER NAME	L	T	P	MARKS	CREDIT POINTS
1.	**PGMVD-491**	Project Part –II	0	0	6	100	10
3.	**PGMVD-492**	Comprehensive Viva-voce				100	4
		Total				**200**	**14**

Detailed Syllabus

SEMESTER – I

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Advanced Engineering Mathematics **Contact:** 3L+1T / Week	**Session:** 2022-2024 **Semester:** I **Course Code:** PGMVD101 **Target Student:** PG **Name of the faculty:** Dr. Ria Bose **Credit:** 4

Module-I:
Fourier series and Transform: Revision of Fourier series, integrals and transforms and their properties. The 2-dimensional fourier transform, convolution theorem, Parseval's formula, discrete fourier transform, fast fourier transform .

Module-II:
Z-transforms: sequence, representation of sequence, basic operations on Sequences, z-transforms, properties of z transforms, change on scale, shifting Property, inverse z-transform, solution of difference equations, region of Convergence, bilinear (s to z) transform.

Module-III:
Walsh function and hadamard transform: generating walsh functions of Order n, characteristics and applications of walsh function, hadamard Matrix, properties, fast hadamard transform, applications

Module-IV:
Advanced Graph Theory: Connectivity, Matching, Hamiltonian Cycles, Coloring Problems, Algorithms for searching an element in a data structure (DFS, BFS).

Module-V:
A review of concepts of probability and random variables: Classical, relative frequency and axiomatic definitions of probability, addition rule, conditional probability, multiplication rule, Bayes' Theorem. Random Variables: Discrete and continuous random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function. Standard Distributions: Uniform, Binomial, Geometric, Negative Binomial, Poisson, Exponential, Gamma, Normal. Sampling Distributions: Chi-Square, t and F distributions. Estimation: The method of moments and the method of maximum likelihood estimation, confidence intervals for the mean(s) and variance(s) of normal populations. Testing of Hypotheses: Null and alternative hypotheses, the critical and acceptance regions, two types of error, power of the test, the most powerful test, tests of hypotheses on a single sample, two samples.

Reference Books:

1) N. Deo, Graph Theory with Applications to Engineering and Computer Science.
2) Dimitris G. Manolakis and John G Proakis, Digital Signal Processing: Principles, Algorithms, and Applications.
3) Alexander M. Mood, Franklin A. Graybill and Duane C. Boes, Introduction to the Theory of Statistics, 3rd Ed., Tata McGraw- Hill, Reprint 2007.
4) Sheldon Ross, Introduction to Probability Models, 9th Ed., Academic Press, Indian Reprint, 2007.
5) A. D. Poularikas, The Transforms and Applications Handbook, CRC Press, 1996.

Course Outcomes: At the end of the course, students will be able to:

CO 1: Characterize and represent data collected from experiments using statistical methods.
CO 2: Solve Boundary value and Initial value problems.
CO 3: To formulate problems in graph theoretic terms such as using graph coloring and matching theory.
CO 4: Apply statistical theories to solve engineering problems.
CO 5: Provide advanced knowledge on topics in pure mathematics, empowering the students to pursue higher degrees at reputed academic institutions.

CO-PO Mapping

Subject	Course Outcomes	POs					
		1	**2**	**3**	**4**	**5**	**6**
Advanced Engineering Mathematics	1. Characterize and represent data collected from experiments using statistical methods.	1	1	1	1	1	1
	2. Model physical process/systems with multiple variables towards parameter estimation and prediction.	2	1	2	2	3	2
	3. Represent systems/architectures using graphs and trees towards optimizing desired objective.	1	1	1	1	1	1
	4.Provide knowledge of a wide range of mathematical techniques and application of mathematical methods/tools in other scientific and engineering domains.	2	2	2	1	2	1
	5.Provide advanced knowledge on topics in pure mathematics, empowering the students to pursue higher degrees at reputed academic institutions.	2	2	2	2	1	3

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Physics of VLSI Devices **Contact:** 3L+1T / Week **Credit:** 4	**Session:**2021-2023 **Semester:** I **Course Code:** PGMVD102 **Target Student:** PG **Name of the faculty:** Dr. Madhumita Das Sarkar

Pre-requisite: Knowledge of basic physics of Semiconductors, Junctions and Devices - diodes, BJTs, FETs, MOS structures.

Module – 1: Introduction to VLSI Design:
What is Integrated Circuit (IC)? History of IC development, Moore's Law, Different types of IC chips; Digital, Analog & Mixed signal ICs; Different Domains of VLSI design; Discussion on VLSI design fundamentals.

Module – 2: (Recapitulation and Orientation):

Discussion on properties of semiconductors in connection with the study of Physics of Junctions; Metal-metal junction, metal-semiconductor junction (Ohmic & Schottky); Bipolar Junction Transistor.

Module -3: Field Effect Transistors & MOS:
What is Transverse field effect & how it leads to channel modulation? Different modes of channel isolation (in brief); Two Terminal MOS Structure: Flat-band voltage, Potential balance & charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance; Poisson's equation for Depletion approximation model.

Module – 4: Three Terminal MOS Structure:
Body effect, Regions of inversion, Pinch-off voltage; Concept of strong & weak inversion.

Module – 5: Four Terminal MOS Transistor:
Current-voltage characteristic of MOSFET; Regions of operation; Solution of Poisson's equation for general channel charge model; regions of inversion - strong inversion, weak inversion, moderate inversion; Enhancement and depletion type MOSFETs. DC and AC equivalent circuit of MOSFET]

Module – 6: Small Channel Effects:
Channel length modulation, Drain induced barrier lowering, Hot electron effect & Voltage
saturation effects; Effect on SCEs on MOSFET performance; Different strategies of scaling, and their relative merits & demerits; Effects of thin oxides and high doping; Subthreshold regions; Advanced MOS devices; SOC, Gate-Engineering, Multi-Gate MOSFETs; Doping Engineering, Material Engineering etc.

Module – 7: CMOS as Mainstay of VLSI chips:
CMOS Performance Factors: Basic CMOS circuit elements; parasitic elements; sensitivity of CMOS delay to device parameters

Text:
1. The MOS Transistor (second edition) Yannis Tsividis (Oxford)
2. Fundamentals of Modern VLSI Devices by Yuan Taur & Tak H. Ning (Cambridge)

Reference:
1. CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford)

Additional Learning Materials:
1. Presentations prepared by self.
2. NPTEL lectures & certification modules.

Course Outcomes:

- Apply the knowledge of basic semiconductor material physics and analyze the characteristics of various electronic devices
- To make the student conversant with the VLSI chip; In this context the importance of the Physics of the devices that make up the chip are to be highlighted.
- The fundamental Physics of the Devices, with special emphasis on the MOSFET should be explained.
- The effects of scaling of device dimensions for inclusion in the VLSI chip are to be enumerated and analyzed.
- Finally, the methods used to overcome the limitations in the context of the devices as they appear in the VLSI chip are to be included.

CO-PO Mapping

Subject	Course Outcomes	POs					
		1	**2**	**3**	**4**	**5**	**6**
Physics of VLSI Devices	1. Apply the knowledge of basic semiconductor material physics and analyze the characteristics of various electronic devices	2	1	2	3	2	3
	2. To make the student conversant with the VLSI chip; In this context the importance of the Physics of the devices that make up the chip are to be highlighted.	3	1	2	2	2	3
	3. The fundamental Physics of the Devices, with special emphasis on the MOSFET should be explained.	1	1	1	3	2	2
	4. The effects of scaling of device dimensions for inclusion in the VLSI chip are to be enumerated and analyzed.	2	1	2	2	2	3
	5. Finally, the methods used to overcome the limitations in the context of the devices as they appear in the VLSI chip are to be included.	2	1	2	2	3	2

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Processor Architecture & SOC Design **Contact:** 3L+1T / Week	**Session:** 2021-2022 **Semester:** I **Course Code:** PGMVD103 **Target Student:** PG **Name of the faculty:** Prof. Amitabha Sinha **Credit:** 4

Prerequisite:
Digital Electronics and logic design with a thorough knowledge about state machine design**.** Familiarization with algorithm and programming concept, FPGA boards may be used for the laboratory, along with design/simulation tools as and when necessary.

Course Objectives:
i) Student should learn the basic and advanced concepts of processor & memory architecture and designing processor and memories. They should also know the performance matrix and how to enhance performance of the processor
ii) Student should learn High Performance Computing
iii) Student should learn SoC Design
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1**. Processor Architecture: (4L)**
a) Concept of a Computer Systems, Basic building blocks, Store and forward concept, Von-Neumann Architecture , Introduction to Processor and Processor Organization. (2L)
b) Processor Architecture: Instruction Set Architecture: Instructions & Addressing, Procedures and Data, Instruction Set Variations. (2L)

2. Datapath Design: (4L)
a) The Arithmetic/ Logic Unit: Number Representation, Adders and Simple ALUs, Multipliers and Dividers, Floating-Point Architecture. Carry Look Ahead adders, Carry Save adder, Pipelined array multiplier, Pipelined adder (4L)

3. Control unit design: **(6L)**
a) Hardwired control unit, Micro-program-controlled unit, Nano Program Control Unit (4L)
b) RISC and CISC Architectures. Harvard architecture, VLIW architecture. (2L)

4. Memory Design: (3L)
a) Concept of Volatile and non-volatile memory, ROM, EPROM, EEPROM, Static RAM, Dynamic RAM, Cache memory, Primary and secondary cache, cache cohesion (3L)

5. Performance Enhancement of Processor by Pipelining: (6L)
a) Basic idea to enhance the performance of a processor, Concept of Pipelining, Pipeline performance, various hazard in pipeline, methods to solve the hazards. (2L)
b) Pipeline performance measurement parameters- speedup, efficiency, throughput, classification of pipeline processor, pipeline structure of CPU, examples from design of arithmetic pipeline- floating point adder, Multifunction pipeline, reservation table, Dynamic pipeline. (2L)
c)Vector Processing: a) Characteristics of vector processing, vector instructions, differences between scalar and vector processing with example, Pipeline chaining. (2L)

6. High Performance Computing:(6L)
a) Performance measurement parameters – MIPS, MFLOPS, SPEC rating, CPI etc., introduction to high performance computing – Overview, Flynn's classification – SISD, SIMD, MISD, MIMD (2L)
b) SIMD Array processors: SIMD computer organization, Masking and Data-Routing Mechanisms, Inter PE Communication, SIMD Inter Connection Networks, Loosely Coupled and Tightly Coupled Multiprocessors (4L)

7. Introduction to SOC and FPGA Architecture and Design: (6L)
a) Concept of SOC, pSOC, SOC vs processor on chip, FPGA concept, architecture and design flow.

b) SOC design issues: SOC architecture, SOC Design Flow,
c) Reconfigurable architecture.

Books:

1. Computer Architecture & Organization J.P Hayes (McGraw Hill)
2. Hwang & Briggs, *Computer Architecture & Parallel Processing* (TMH)
3. Tien-Fu Chen, *Overview of SOC architecture design*, (National Chung Cheng University)

Reference Books:

1. Hwang, *Advanced Computer Architecture*, (TMH)
2. Patterson & Hennessy, *Computer Organization & design,* (Morgan Kaufmann)
3. Stalling, *Computer organization and architecture, designing for performence*, (PHI)
4. Antonakos, *An Introduction to intel family of Microprocessors*, (Pearson)
5.. Flynn , *Computer Architecture*, (Narosa)
6. Tammy Noergaard*, Embedded Systems Architecture – a comprehensive guide for engineers and programmer*s, (Elsevier)
7. David A. Patterson and John L. Hennessy, Computer Organization and Design
8.Carl Hamachar, Zvonco Vranesic and Safwat Zaky, *The Hardware/Software Interface*, Elsevier.
9. William Stallings, *Computer Architecture and Organization*, McGraw Hill.
10. Vincent P. Heuring and Harry F. Jordan, *Computer Organization and Architecture: Designing*
11. A.Sinha , Processor Architecture (Lecture notes), MAKAUT

COURSE OUTCOME (CO)

1. To learn the Concept of a Computer System and Design methodology of Processor Design
2.. To learn Datapath Design (Adder, Subtractor, multiplier etc.)
3. To learn the design of hardwired control unit, microprogrammed and nano programmed Control unit.
4. To learn Memory Technology & design various types of memory units and memory Organization.
5. To learn the concept of Performance Enhancement of Processor by Pipelining, SOC architecture, FPGA architecture, design, and Reconfigurable Architecture

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Processor Architecture and System On Chip	**1. To learn the Concept of a Computer System and Design methodology of Processor Design**	1	2	3	1	1	1

design	**2. To learn Datapath Design (Adder, Subtractor, multiplier etc.)**	2	3	3	3	3	1
	3. To learn the design of hardwired control unit, microprogrammed and nano programmed Control unit.	2	3	3	3	3	1
	4. To learn Memory Technology & design various types of memory units and memory organization.	3	3	3	3	3	1
	5. To learn the concept of Performance Enhancement of Processor by Pipelining, SOC architecture, FPGA architecture, design and Reconfigurable Architecture	3	3	3	3	3	1

Department: Microelectronics and VLSI Technology **Year:**1st **Course Name:** Microelectronics Technology **Contact:** 3L+1T / Week **Credit:** 4	**Session:**2021-2023 **Semester:** I **Course Code:** PGMVD104 **Target Student:** PG **Name of the faculty:** Dr. Madhumita Das Sarkar

Module-1: Introduction to Microelectronics Technology

Domain Overview:
Concepts to development of IC, Level of Integrations; Different types of Integrated circuits; Silicon as a material of choice for VLSI chip, Discussion on fabrication process fundamentals. 4L

Module – 2: Recapitulation and Orientation
Brief discussion on crystalline Properties of semiconductor in connection with the growth of Si as a substrate material, Si Ingots and wafer, Studies on properties PN Junctions; Metal-metal junction, metal-semiconductor junction (Ohmic & Schottky); 6L

Module- 3: Cleaning and Etching
Wafer Cleaning as a unit Process, Surface Contaminations, Cleaning methods : Solvent method, Pirhanah Cleaning & RCA cleaning, Concept of Clean room
(Laboratory Practices under PGMVD-191: Cleaning of p-type & n-type Si-wafer by solvent method, Piranha Cleaning & RCA cleaning) 4L
Etching – Introduction to Etch Process, Types of Etching, Issues in Etching, Basic Mechanisms of Etching process, Etch Parameters; Isotropic and Anisotropic etching. Bias and Degree of Anisotropy, Reactive Ion Etching, selective etchant for different subject. 4L

Module 4 : Oxidation
Introduction to Oxidation Process, Properties and Function of Oxide layer, Growth mechanism and kinetics of Oxidation, Oxidation Techniques and systems, growth and properties of dry and and wet oxide, Oxide properties, Oxide induced defects, characteristics of oxide films, Application of thermal oxide and CVD oxide; Dopant distribution, quality of oxide layer, Local Oxidation (LOCOS);
(Laboratory Practices under PGMVD-191: Fabrication of MOS capacitor) 8L

Future plan: Fabrication of capacitor

Module 5 : Ion implantation
Solid State Diffusion and Diffusion Vs modern method of Dopant incorporation –
Ion implantation – Range theory, Equipments, Annealing, high energy implantation

Module 6: Lithography
Introduction to Lithography, Optical Lithography: Concept of lithography room, Exposure tools, Masks, Photo resists and Pattern Transfer 6L

Module 7: Metallization
Introduction, Different types of metallisation : physical vapour deposition uses, sputtering deposition, Aluminium Metallization, Junction spiking,, Electromigration, Damascene and Dual damascene technology, Salicide technology 4L
Laboratory Practices under PGMVD-191 Learning Metallisation process (PVD) by using Thermal evaporation and Electron beam gun)

Module 8:
VLSI Process integration for making a particular Device (MOSFET) 2L

Text Book:

- Sze, S.M , Wiley, 1985*, Semiconductor Devices: Physics and Technology*,
- Campbell ,*The Science and Engineering of Microelectronic Fabrication*,Oxford University Press
-

Reference Book:

- Morgan, D.V., and Board, K , *An Introduction to Semiconductor Microtechnology*
- The National Technology Roadmap for Semiconductors , Notes: Semiconductors Industry Association, SIA, 1994
- Sze, S.M. , *Electrical and Electronic Engineering Series VLSI Technology*, Mcgraw-Hill International Editions

Course Outcomes: Students must be able to

- appreciate the role of material Silicon in VLSI chips.
- have a clear concept of the Unit Processes and their specific application area.
- understand the fabrication of a complete device.

- assess the different performance parameters of the unit process of a VLSI chip and comment on how to optimize the performance.
- Understand the steps involved in nano device processing applied in Semiconductor manufacturing industry.

CO-PO Mapping

Subject	Course Outcomes	POs					
		1	**2**	**3**	**4**	**5**	**6**
Microelectronics Technology	1. Appreciate the role of material Silicon in VLSI chips.	2	1	2	3	2	3
	2. Have a clear concept of the Unit Processes and their specific application area.	2	1	2	2	2	2
	3. Understand the fabrication of a complete device.	1	1	1	3	2	3
	4. Assess the different performance parameters of the unit process of a VLSI chip and comment on how to optimize the performance.	2	2	2	2	2	3
	5. Understand the steps involved in nano device processing applied in Semiconductor manufacturing industry.	2	1	2	2	1	3

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name: Digital VLSI Circuits & Systems** **Contact:** 3L+1T / Week	**Session:**2021-2022 **Semester:** I **Course Code:** PGMVD105 **Target Student:** PG **Name of the faculty:** Prof. Amitabha Sinha **Credit:** 4

Prerequisite: Basic concept of Digital Logic - combinatorial & sequential logic design, Digital Laboratory, Basic concept of BJT and MOS transistors.

Principal Objective:

- To make the student conversant with the VLSI chip design
- Special emphasis on the MOSFET should be explained.

- The effects of scaling of device dimensions for inclusion in the VLSI chip are to be enumerated and analyzed.
- Finally the methods used to overcome the limitations in the context of the devices as they appear in the VLSI chip are to be included.

1: Introduction to VLSI Design (4 Lectures)

Basics of Integrated Circuit (IC), SSI, MSI, LSI, VLSI, ULSI, Integration levels. History of IC development, Moore's Law, Different types of IC chips; Digital, Analog & Mixed signal ICs; Different Domains of VLSI design; EDA- the VLSI design CAD tools, VLSI design state-of-the-art, some emerging applications of VLSI, VLSI design complex processor, VLSI Design Flow, Synthesis, layout generation, Verification and simulation, VLSI chip manufacturing process flow.

2: **CMOS logic Basics (6 Lectures)**

Basics of MOS transistors and MOS as switches, Complementary CMOS logic, CMOS logic behaviour, advantages and drawbacks of CMOS logic, Pull-up and pull-down network, conduction complement, complex logic function using CMOS, pass transistors, transmission gates, tri-state buffers, Flip- flops (D- F/F, JK F/F etc.), transistor count, Delay, drawbacks of CMOS, Dynamic logic, Domino logic, Bi-CMOS to overcome the drawbacks of CMOS, standard cell design, full custom design. example of standard cell., Sequential Logic circuits –asynchronous and synchronous sequential circuits, Moore machine, Mealy machine, examples, Finite state machine design

3. Basics of CMOS fabrication and Layout: (6)

Introduction to VLSI fabrication and fabrication steps, Concept of MASK, Lithography, etching, polysilicon patterning, ion implementation , metallization etc., fabrication error, concept of layout, feature size, Lambda rule, concept of process technology, stick diagram, general design rules for layout, width spacing rule, poly diffusion interaction, contacts, VIA and contact spacing, examples of CMOS layout of an inverter, NAND/NOR gates, simplified design rule, full custom and standard cell layout, placement, routing, floor planning

4. Hardware description language & EDA tools (6)

EDA tools and their advantages, concept of test bench, simulation, design verification, synthesis, hardware description language (HDL)-VHDL/VERILOG/SYSTEM C etc.

5. Programmable Hardware and FPGA (6)

Concept of Programmable Hardware (PLA, PLD, CPLD, FPGA) and their requirements, FPGA --Architecture, configuration and design flow, system design using FPGA, concept of System on Chip (SOC). FPGA as reconfigurable computing and programmable System on Chip (pSOC). FPGA as validation of custom design or ASIC.

6. Logical Effort (4)

Logical effort-Path Logical Effort, Path Electrical Effort, Path Effort, branching effort, delay in a logic gate, path effort delay, path parasitic delay, designing fast circuits and gate sizes, multistage logic networks, choosing the best number of stages, delay **vs.** fan out

7. Design of a 32-bit RISC CPU and 1K8 bit RAM (6)

Designing a RISC CPU with fixed instruction length (32 bit) CPU , few instructions , Static RAM design with 1024 locations with each word size of 8 bits, Simulation, Synthesis & validation of the architecture on FPGA and analysis of the performance of the CPU with a

small program written in machine language.

Text:

1. Introduction to VLSI Systems—Carver Mead, Lynn Conway, B.S. Publication
2. Chip Design for Submicron VLSI-- John P Uyemura, Thompson Publication.
1. Advanced CMOS cell Design: Etienne Scard., Sonia Delmas Bendhia, McGraw Hill Professional.
2. VLSI Design Black Book—K.V.K.K. Prasad, Kattula Shyamala, dreamtech Publication
3. A Verilog HDL Premier , 2nd edition, J. Bhaskar , BS Publication

References:

1. Fundamentals of Modern VLSI Devices by Yuan Taur & Tak H. Ning (Cambridge)
2. Logic and Computer Design Fundamentals—M. Morris Mano and Charles R.Kime, Pearson Education.
3. Digital Design | With an Introduction to the Verilog HDL, VHDL, and ,System Verilog| by M. Morris Mano and Michael D. Ciletti Sixth Edition, Pearson
4. CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford).
5. The MOS Transistor (second edition) Yannis Tsividis (Oxford)
6. NPTEL lectures & certification modules.
7. Russell, G, Kinniment, D.J., Chester, E.G., and McLauchlan, M.R., *CAD for VLSI* Notes: Van Norstrand Rheinhold, 1985.
8. Neil Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* (3rd Edition).

COURSE OUTCOME(CO)

1.To learn the basics of Integrated Circuit (IC): different Domains of VLSI design, design automation tools and the state-of-the-art VLSI circuits.
2. To learn CMOS logic behaviour, advantages and drawbacks using static, dynamic, Domino-logic and Bi-CMOS logic, logical effort, path effort, path effort delay, path parasitic delay, designing fast circuits and multistage logic networks and the concept of delay **vs.** fan out
3. To learn the basics of CMOS fabrication and Layout.
4. To learn EDA tools and their advantages, concept of test bench, simulation, design verification, synthesis and hardware description language (Verilog)
5. To learn the concept of Programmable Hardware and their requirements, FPGA --architecture, configuration and design flow, concept of System on Chip (SOC) and FPGA as validation of custom design or ASIC, the design of a 32-bit RISC CPU, Static RAM and Simulation, Synthesis & validation of the architectures on FPGA and analysis their performances.

CO -PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Digital VLSI Circuits & Systems	1. To learn the basics of Integrated Circuit (IC); different Domains of VLSI design, design automation tools and the state-of-the-art VLSI circuits.	2	2	1	1	1	1
	2. To learn CMOS logic behaviour, advantages and drawbacks using static, dynamic, Domino-logic and Bi-CMOS logic, logical effort, path effort, path effort delay, path parasitic delay, designing fast circuits and multistage logic networks and the concept of delay **vs.** fan out	3	3	3	3	2	1
	3. To learn the basics of CMOS fabrication and Layout.	3	3	3	2	3	1
	4. To learn EDA tools and their advantages, concept of test bench, simulation , design verification , synthesis and hardware description language(Verilog)	2	2	2	2	3	1
	5. To learn the concept of Programmable Hardware and their requirements, FPGA --architecture, configuration and design flow, concept of System on Chip (SOC) and FPGA as validation of custom design or ASIC, the design of a 32-bit RISC CPU, Static RAM and Simulation, Synthesis & validation of the architectures on FPGA and analysis their performances.	2	3	3	3	3	1

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name: Microelectronics Lab-I** **Contact:** 3P / Week **Credit:** 2	**Session:**2021-2022 **Semester:** I **Course Code:** PGMVD191 **Target Student:** PG **Name of the faculty:** Dr. Madhumita Das Sarkar

1. Cleaning the substrate by using Solvent Method.
   - Glass Substrate
   - Silicon substrate (P-type and n-type)

2. Cleaning the n-type and p-type water for further processing / Thin film deposition using following methods:-
   - Solvent method.
   - Piranha Method.
   - RCA Cleaning method.

3. Etching of a cleaned P-type Si-wafer by using HF:HNO3 in required Stoichiometric volume.
   - Study the sample under compound microscope and Study illumination of the sample under UV light.

4. Study the etching rate under environmental condition:-
   - Isotropic etching.
   - Anisotropic etching.

5. Contact metallization on Si wafer by using Physical Vapour Deposition (PVD Technique)
   - Ohmic contact.
   - Schottky contact.

6. Contact metallization on Si wafer by using Electron Beam Evaporation ()
   - Ohmic contact.
   - Schottky contact.

7. Contact Metallization by depositing Thin Film Coating
   - By using Spin Coating method.

COURSE OUTCOME(CO)

After completion of this course students are able

1. To get familiar about Cleaning the substrate by using Solvent Method
2. To get familiar about Etching of a cleaned P-type Si-wafer
3. To Study the etching rate under environmental condition
4. To Understand about the Contact metallization on Si wafer

CO -PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Microelectronics Lab-I	1. To get familiar about Cleaning the substrate by using Solvent Method	3	3	2	1	2	2

	2. To get familiar about Etching of a cleaned P-type Si-wafer	3	3	3	2	2	2
	3. To Study the etching rate under environmental condition	2	2	3	2	3	2
	4. To Understand about the Contact metallization on Si wafer	3	2	3	3	1	2

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name: VLSI Design - Lab-I** **Contact:** 3P / Week **Credit:** 2	**Session:**2021-2022 **Semester:** I **Course Code:** PGMVD192 **Target Student:** PG **Name of the faculty:** Dr. Mihir Kumar Mahata + Mr. Sowvik Dey

Course Objective:
1- student will be familiar about the steps involved in VLSI design.
2- students will be able to write program in hardware definition language (HDL) like Verilog.
3- student will be able to design the digital circuit on VLSI design Tools like Xilinx ISE / Icarus Verilog.
4- students will be able to write the Test Bench program for simulation.
5- student will be able to Validate the design of circuit by Test Bench in iSim/GTK Wave Simulator.
6- student will be able to make Bit-stream file and download into FPGA.

Pre-requisite: Knowledge of programming, Basic gates, Digital Circuits – Combinational & Sequential

Part-A: FPGA Based Digital Design

Software & Hardware Tools – Xilinx ISE, VIVADO, FPGA Boards

LAB – 1A: Introduction to FPGA Based Digital Design:
- Register-transfer-level abstraction
- Introduction to HDL Coding by Basic Digital Gates
- Using Xilinx ISE Pack for HDL Coding, Simulation & Synthesis

LAB – 1B: Understanding the FPGA Board
- Identifying the Board Parts
- Procedure of Bit-Stream Downloading by Basic Digital Gates
- JTAG

LAB – 2: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Combinational Circuit – Multiplexer, Demultiplexer, Decoder, Encoder, Half Adder, Full Adder, Half Subtractor, Full Subtractor, Adder- Subtractor.

LAB – 3: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Combinational Circuit – Ripple Carry, Carry look ahead adder
- Construction of Higher Level Multiplexer using Lower Level Multiplexer
- Circuit Designing using universal logic: Multiplexer

LAB – 4: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Sequential Circuit –
- Flip-Flop – SR, D, JK, T

LAB – 5: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Sequential Circuit –
- Counter – Up, Down, Bidirectional, Ring, Ripple, Johnson, Mod-N.

LAB – 6: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. Sequential Circuit –
2. Register – Left/Right Shift Register, Construction of Memory.

LAB – 7: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. Sequential Circuit –
2. FSM – Mealy & Moore

LAB – 8: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. ALU Design

Part-B: Front End Using Synopsys

Software – Synopsys, CentOS

LAB – 9: Synopsys Front End - Introduction
- Using Verilog Compiler Simulator (VCS)
- Using DVE for analyze, compile and simulate
- Using Design Vision for Synthesis & Gate Level Netlist preparation

LAB – 10: Synopsys Front End-Experiment
- Experiment with Up-Down Counter with above 3 modules
- Functionality Check
- Timing Analysis
- Power Analysis

Books:
1. Advanced Digital Design using Verilog-HDL, Michael. D. Ciletti, PHI publications.

COURSE OUTCOME(CO)

After completion of this course students are able

1. To get familiar about VLSI Design Tools like Xilinx, Icarus Verilog, GTK Wave
2. To Understand the difference between sequential language and concurrent language.
3. To Know about the Hardware Description Language (Verilog/VHDL) to describe the Combinatorial and Sequential logic as well as Test Bench for simulation.
4. To Understand about the FPGA Board and JTAG Cable and generate bit stream file and download to the programmable hardware device: FPGA.
5. To get familiar about front-end design tool: Synopsys and understand the hardware realization of the design by Synthesis Steps: High level Synthesis, logic Synthesis, physical Synthesis.

CO -PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
VLSI Design Lab-I	CO1. Familiar about VLSI Design Tools like Xilinx, Icarus Verilog, GTK Wave.	1	2	3	2	3	1
	CO2. Understand the difference between sequential language and concurrent language.	1	3	2	2	3	1
	CO3. Know about the Hardware Description Language (Verilog/VHDL) to describe the Combinatorial and Sequential logic as well as Test Bench for simulation.	1	2	2	2	3	1
	CO4. Understand about the FPGA Board and JTAG Cable and generate bit stream file and download to the programmable hardware device: FPGA.	1	2	2	2	3	1
	CO5. To get familiar about front-end design tool: Synopsys and understand the hardware realization of the design by Synthesis Steps: High level Synthesis, logic Synthesis, physical Synthesis.	1	2	2	3	3	1

SEMESTER – II

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Analog VLSI Circuits & Systems **Contact:** 3L+1T / Week	**Session:** 2021-2022 **Semester:** II **Course Code:** PGMVD201 **Target Student:** PG **Name of the faculty:** Dr. Mihir Kumar Mahata **Credit:** 4

Objectives:

1. To Design the single stage amplifiers using PMOS and NMOS driver circuits with different loads.
2. To Analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
3. To Study the different types of current mirrors and to know the concepts of voltage and current reference circuits.

4. To Understand about MOS switched capacitor filters.
5. Apply the methods learned in the class to design and implement practical projects.

Sl. No	Module Name and Topics	Class hours
1	**Introduction:** Motivation for analog VLSI and mixed signal circuits in CMOS technologies and issues thereof.	2
2	**CMOS device fundamentals:** Basic MOS models, device capacitances, parasitic resistances, substrate models, transconductance, output resistance, f_T, frequency dependence of device parameters.	6
3	**Single stage amplifiers, Differential Amplifiers:** Common source amplifier, source degeneration, source follower, common gate amplifier, cascade stage. Basic differential pair, common mode response, differential pair with MOS loads, Gilbert Cell, device mismatch effects, input offset voltage.	10
4	**Current Mirrors, Current and Voltage Reference:** Basic current mirrors, cascode current mirrors, active current mirrors, low current biasing, supply insensitive biasing, temperature insensitive biasing, impact of device mismatch.	4
5	**Frequency Response of Amplifiers, Feedback:** Miller effect, CS amplifier, source follower, CG amplifier, cascade stage, differential amplifier, Multistage amplifier. Feedback topologies, effect of load, modeling input and output ports in feedback circuits.	4
6	**Operational Amplifiers:** Performance parameters, One-stage and two-stage Op Amps, gain boosting, comparison, common mode feedback, input range, slew rate, power supply rejection, noise in Op Amps.	8
7	**Other Sub-circuits**, **Field Programmable Analog array (FPAA):** Comparators; AD & DA conversion; Swiched-mode circuits – principle of operation.Concept of switch capacitor, Configurable analog block (CAB), Basic concept of FPAA, Architecture of FPAA, EDA tools, Application of FPAA.	6
	Total	40

Text:

1 CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford)

Reference:

1. Weste N and Eshraghian K; Addision Wesley 1985 ,*Principles of CMOS VLSI Design*
2. Mukherjee A , 1986, *Introduction to NMOS and CMOS VlSI Systems Design* , Prentice-Hall
3. Mead and Conway, *Introduction to VLSI Systems* , Notes: Addison Wesley D C & Co

COURSE OUTCOME(CO)

After completion of this course students are able

1. Learn circuit design technique and design issues in CMOS technologies.
2. Gain knowledge of basic MOS models, device capacitances, parasitic resistances, transconductance, up to frequency dependence of device parameters.
3. Understand the significance of different biasing styles and apply them for different circuits.
4. Design basic building blocks like sources, sinks, mirrors, up to layout level and acquire computer skills (e.g. LT-spice) for the design and analysis of circuits.
5. Comprehend the design and analysis of MOS Op-Amp circuits and systems, identifying suitable topologies of the constituent sub systems and corresponding circuits as per the specifications of the system.

CO -PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3	3	2	1
CO2	2	2	3	2	2	1
CO3	2	2	3	3	2	1
CO4	2	2	3	2	2	1
CO5	2	1	3	3	2	1
CO6	1	2	3	3	3	2
CO7	1	1	3	2	2	2
Average	2	2	3	3	2	1

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name: Testing & Verification of Digital Systems** **Contact:** 3L+1T / Week	**Session:**2021-2022 **Semester:** II **Course Code:** PGMVD202 **Target Student:** PG **Name of the faculty:** Prof. Amitabha Sinha **Credit:** 4

Module 1 (2 Hrs.) **(Introduction to VLSI Design Flow, concept of Testing & Verification)**	Introduction to VLSI Design (Flow, Synthesis, layout generation, Verification and simulation), background of testing of electronic circuits, basic concept of Testing & Verification and their differences, Automatic Testing equipment.
Module 2 (6 Hrs.) **(Testing in different stages of manufacturing, Design verification, and system level operation and testing)**	Testing in different stages of manufacturing, Design verification, chip yield, system level operation and testing, different testing algorithms, EDA tools for testing

Module 3 (6 Hrs.) **(Test Pattern Generation and Fault Modelling)**	Concept of Automatic Test pattern Generation (ATPG), Fault coverage, Fault models, Stuck-at-1, stuck-at-0 faults, transistor faults, collapsed faults, bridging faults, Delay Faults and Crosstalk, pattern sensitivity and coupling faults.
Module 4 (6 Hrs.) **(Automatic Test Pattern Generation, different types of faults and Design for Testability)**	Automatic Test Pattern Generation (ATPG): Algorithms for generating sequence of test vectors for a given circuit based on specific fault models. Fault analysis and Simulation to emulate fault models in CUT and application of test vectors to determine fault coverage: Parallel, deductive, and concurrent fault simulation, Design for testability, Scan, Built-in-self-test, Pseudo random number generator, Automatic Test Generation, Built in Logic Block observer (BILBO)
Module 5 (6 Hrs.) **(Boundary Scan and JTAG)**	Boundary Scan , JTAG (IEEE standard 1149.1) concept , Architecture and Instruction set and Boundary Scan TAP control operation .testing process using JTAG Testing of Analog and Mixed signal circuits, Differences from digital testing , Test procedures, DSP based mixed signal test, Test plan , Boundary Scan Architecture & instruction Set of Mixed Signal Testing (IEEE1149.4) and test Process
Module 6 (6 Hrs.) **(Testing of Analog & mixed signal circuits)**	Different packages, Concept of Analog circuit testing, traditional concept of analog circuit testing and their limitations, specification-based test, different methods of functional testing, testing of Analog VLSI circuits, testing of mixed signal circuits, DSP based mixed signal circuit testing, waveform synthesizer/digitizer.
Module 7 (4 Hrs.) **(Boundary scan method for Testing of Analog & mixed signal circuits)**	boundary scan technique (IEEE 1149.4) method of using them for testing analog and mixed signal circuits IEEE 1149.4 Standard Analog Test Bus (ATB), Basic Mixed Signal Chip structure IEEE 1149. Digital /Analog Interfaces, Analog test access Port, Test Bus Interface circuit (TBIC), TBIC

	Switching Patterns, Chaining of 1149.4 compliance ICs.

Text Books:

1. Testing of Digital Systems" by N. K. Jha et.al.

2. Essentials of Electronic **Testing**" by M L Bushnell and V D Agrawal.

3. Digital Systems **Testing** and Testable **Design**" by M Abramovici and A D Friedman.

Reference Books:

1. Testing & Verification of VLSI circuits – Lecture notes by A.Sinha
2. Built-in **Test** for **VLSI**: Pseudorandom Techniques" by P H Bardell and J Savir

COURSE OUTCOME(CO)

After completion of this course students are able

1.To learn the step by step design flow of VLSI circuits and systems in details , the need of design verification & testing and the difference between testing and verification
2. To learn testing in different stages of manufacturing, Design verification, chip yield, system level operation and testing
3. To learn the concept of test vectors, test generation, different types of faults, fault modelling and to analyse the behaviour of the circuit under test (CUT)
4.To learn different algorithms of Automatic Test generation (ATPG) on specific fault models and fault simulation, Design for Testability (DFT) and different approaches and also various techniques and methodologies used for testing different analog and mixed signal circuits.
5. To learn the concept of boundary scan technique and standardized test interface (IEEE standard 1149.1) to build capability of observing and controlling pins into each chip to make board test easier

CO -PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Testing & Verification of VLSI circuits	1.To learn the step by step design flow of VLSI circuits and systems in details , the need of design verification & testing and the difference between testing and verification	2	2	3	3	2	1
	2.. To learn testing in different stages of manufacturing , Design verification ,chip yield, system level operation and testing	3	3	3	3	2	1

	3. To learn the concept of test vectors , test generation , different types of faults ,fault modelling and to analyse the behaviour of the circuit under test (CUT)	2	3	3	3	2	1
	4. To learn different algorithms of Automatic Test generation (ATPG) on specific fault models and fault simulation, Design for Testability (DFT) and different approaches and also various techniques and methodologies used for testing different analog and mixed signal circuits.	2	3	2	3	3	1
	5. To learn the concept of boundary scan technique and standardized test interface (IEEE standard 1149.1) to build capability of observing and controlling pins into each chip to make board test easier	2	3	3	3	3	1

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name: Digital Signal Processing and Applications** **Contact:** 3L+1T / Week	**Session:**2021-2022 **Semester:** II **Course Code:** PGMVD203 **Target Student:** PG **Name of the faculty:** Prof. Amitabha Sinha **Credit:** 4

Pre-requisites: 1] Signals and Systems ii] Advanced Engg. Maths iii]Digital Electronics iv] Computer Architecture & Organization / Processor Architecture

Course Objective:

This course is to make students familiar with the most important methods in DSP, including digital filter design, transform-domain processing , multi resolution signal Processing and importance of signal processors by providing a thorough knowledge of design , implementation and analysis of DSP systems .

Module 1: Introduction to Discrete-Time Signal & Systems (3L)

Concept of continuous time signal and discrete time signals, Discrete Analog and Digital signals & Systems. Advantages of Digital signal Processing Systems Analog Signal Processing Systems. Converting continuous signal to digital signal (Sampling, Quantization and coding): Study of sampling theorem, effect of under sampling.

i] Aliasing Problem: To analyze the effect of under-sampling a signal using MATLAB

ii] Study of Quantization of continuous-amplitude, discrete-time analog signals Quantization error

iii] Coding of quantized signal, different types of coding

Concept of ADC, DAC and Different types of ADC (Successive approximation, dual slope, pipelined, Flash, Sigma delta etc.) and DAC

2. Concept of continuous-time Fourier transform , discrete- time Fourier transform (DTFT), Discrete-Fourier Transform (DFT)and Fast Fourier Transform (FFT).

Continuous time Fourier Transform (3L)

Concept of continuous time Fourier transform and to derive equation for discrete time Fourier transform (DTFT) and analyze them using MATLAB, Computer discrete time Fourier transform of various signals, Properties of Discrete Time Fourier Transform, Discrete Fourier transform, decimation in time and decimation in frequency, Various properties of discrete time Fourier transform and verify these properties on various signals on MATLAB. Algorithm of Discrete Fourier Transform on MATLAB and to find discrete Fourier transform of various signals on MATLAB. Properties of discrete Fourier transform.

Module 2: Fast Fourier Transform (FFT) (3L)

Fast Fourier transform (FFT) algorithm and complexity analysis. To analyze fast Fourier algorithms and analyze using MATLAB. Architecture of DFT and FFT Processor.

Module 3: Z Transform (6)

Z – Transform: Basic concept, Transformation from S to Z Transformation, DTFT to Z Transformation, two sided and one-sided Z Transform, Concept of unit circle and ROC, Stability, casualty, Properties of ROC, properties of Z Transform, Z Transformations of basic functions like unit impulse, step, exponential, Sine etc., Examples, inverse z transform, partial fraction method etc. Bi-linear transformation (relation between S and Z transformation), System Transfer Function, to understand basic building blocks like adder, multiplier and delay units of discrete time systems, Transfer functions of Recursive and Non-Recursive filters and their different realization (Direct, Transpose, Cascade, Parallel etc.) of FIR and IIR Filters.

Module 4: Digital Filter Design (4L)

a) **FIR filter design** (Low pass, High Pass, Band Pass, Band stop) Linear phase FIR filter, Filter design using Fourier Transform, Gibbs Phenomenon, Goertzel Algorithm.

b) **IIR Filter design**, analog filter approximation and to design of Butterworth, Chebychev and Elliptic filters.

c) **simulation** of Infinite Impulse Response (IIR) Filters and Finite Impulse Response (FIR) filters and analyzes their responses on MATLAB.

d) **Multi-Rate Signal Processing (2)**
Introduction, Why multi-rate Signal processing? Up Sampling , Down Sampling, rational sampling, CIC (Cascaded Integrated comb filtering)

e) **Adaptive Signal Processing (2)**
Introduction, LMS algorithm, Adaptive filtering with DCT/ LMS,Applications: Adaptive echo cancellation, Adaptive echo cancellation, fatal electrocardiography etc.

Module 5: Time frequency analysis and introduction to wavelet transform. (4L)

Introduction**,** Time frequency analysis**,** Limitation of Fourier transform**,** Short term Fourier transform**,** Mathematical expression of Wavelet transform and analysis**,** Wavelength transform algorithm and architecture. Application of wavelet transform

Module 6: DSP Architecture: (4)

Key features of DSP processors (MAC unit, circular addressing scheme, zero overhead looping , bit reversal technique , Pipelining , Harvard Architecture), Different DSP Processors and their Architectures, Implementation of DSP algorithms on 16 bit , 32 bit DSP Processors like TMS320 C30 , TMS 320 C65XX series DSP Processors , FPGA architecture, (, Xilinx Spartan 6E, Virtex 6, Artix 7 etc.) , Programming using HD and system design. Mapping DSP algorithms onto DSP

Processors/ FPGA .

Module 7: DSP Applications (4L)

i] DTMF detection ii] LMS algorithm iii] Adaptive echo cancellation iv] Software Defined Radio/Cognitive Radio

Text Books:

1. Digital Signal Processing -j.g.Proakis 7 D.G. Manolakis (Pearson Education)
2. Digital Signal Processing – S.K. Mitra (Tata Mcgraw- Hill Publishing Co.)
3. Digital Signal Processing -Andreas Antonio (Tata Mcgraw Hill Publishing Co.)

Reference Books:

1.Theory and Problems of Digital Signal Processing- M.H. Hayes (Tata Mcgraw- Hill Publishing Co.)
2. Digital Signal Processing- Steve White (Cengage Learning,India edition)
3. Digital Signal Processing & Applications with the TMS320C6713 and TMS320C6416 DSK – R. Chassing, Donald Reay (Willey student edition)
4. Digital Signal Processing – Lecture notes by A.Sinha
5. Network analysis -Van Valkenburg (Prentice-hall of India Pvt. Ltd.)

COURSE OUTCOME(CO)

After completion of this course students are able

1.To learn the concept of Discrete Signals/Digital signals & Systems and their advantages over Analog Signal Processing systems
2. To learn Continuous Time Fourier Transform (CTFT), Discrete Time Fourier Transform (DTFT), Discrete Fourier Transform (DFT) , Fast Fourier Transform (FFT),
3.To learn the requisite mathematics (Z Transform) to model system behavior and their response to a given stimuli.
4.To learn and acquire design skills on frequency domain analysis of different filters such as FIR & IIR, multi-resolution filter and adaptive Filter using MATLAB, realization of Digital Filters on different hardware platforms (DSP Processors, FPGAs, advanced Signal Processors, FPGAs and ASICs.)
5. To learn in details about time frequency analysis and Wavelet transform, different applications of Digital Signal Processing like DTMF, Echo cancellation, SDR etc.

CO -PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Digital Signal Processing & Applications	1. To learn the concept of Discrete Signals/Digital signals & Systems and their advantages over Analog Signal Processing systems	2	2	2	1	2	1

	2.. To learn Continuous Time Fourier Transform (CTFT), Discrete Time Fourier Transform (DTFT), Discrete Fourier Transform (DFT) , Fast Fourier Transform (FFT),	3	3	3	3	3	1
	3. To learn the requisite mathematics (Z Transform) to model system behaviour and their response to a given stimuli	3	3	3	3	3	1
	4.To learn and acquire design skills on frequency domain analysis of different filters such as FIR & IIR, multi-resolution filter and adaptive Filter using MATLAB, realization of Digital Filters on different hardware platforms (DSP Processors, FPGAs, advanced Signal Processors, FPGAs and ASICs.)	3	3	3	3	3	1
	5. To learn in details about time frequency analysis and Wavelet transform, different applications of Digital Signal Processing like DTMF, Echo cancellation, SDR etc.	3	3	3	3	3	1

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Advanced Micro and Nano Devices **Contact:** 3L+1T / Week	**Session:**2021-2023 **Semester:** I **Course Code:** PGMVD204 **Target Student:** PG **Name of the faculty:** Dr. Madhumita Das Sarkar **Credit:** 4

Prerequisite:

Fundamentals of semiconductor physics and basics of p-n junctions, bipolar transistors, JFETs, MOS capacitors, MOSFETs, CMOS, low and high frequency equivalent circuits of BJTs and MOSFETs, IC technology.

Course content:

Module-1 (14 lectures) – [Recapitulation of MOS scaling laws, Short channel effects, MOSFET models], Nano CMOS, Effects of gate oxide tunneling, Concept of EOT, high-k dielectrics, Effects of nanoscaling on MOSFET characteristics and performance, Technology trend, Advanced CMOS structures, SOI.

Module-2 (8 lectures) – Semiconductor heterojunctions; compound semiconductor and silicon-germanium heterostuctures, superlattice, HBTs, PETs, MESFETs, advanced solar cell structures.

Module-3 (14 lectures) – Fundamental concepts of quantum structures and tunneling junctions, Nanotubes, Devices based on quantum wells, quantum wires/nanotubes and quantum dots – HEMTs, RTDs, CNT MOSFETs, SETs, Terahertz devices, advanced optoelectronic devices

Module-4 (6 lectures) – Outline of nanofabrication – nanolithography, MBE, MOVPE; Introduction to molecular electronics.

Module-5 (6 lectures) - Optical Properties, Photoconductivity, Optical absorption &amp transmission, Photoluminescence, Fluorescence, Phosphorescence, Electroluminescence., LEDs, laser diodes, photodetectors, solar cells.

Text Books:

1. Ning & Taur
B.R.Nag
S.M. Sze`
2. Quantum Physics – A. Ghatak
3. Quantum Mechanics - Bransden and Joachen

Course outcomes: At the end of the course, students will be able to:

- CO1-Develop and evaluate the fabrication and design of nanometric CMOS devices.
- CO2- Explain the physical principles of spintronic devices, carbon nanotubes and graphene
- CO3- Compare the properties of materials for deep-submicron and nanometre CMOS IC, HEMT, single electron transistors and resonant tunnelling devices
- CO4- Plan the fabrication procedure for deep-submicron and nanometre CMOS IC with the proper technological process for the materials of the substrate, implanted areas, isolation, metallisation.
- CO5-Design simple CMOS integrated silicon MEMS sensor devices.

CO-PO Mapping

Subject	Course Outcomes	POs

		1	2	3	4	5	6
Advanced Micro and Nano Devices	1. Develop and evaluate the fabrication and design of nanometric CMOS devices.	**2**	1	**2**	3	2	3
	2. Explain the physical principles of spintronic devices, carbon nanotubes and graphene	**2**	1	2	2	3	2
	3. Compare the properties of materials for deep-submicron and nanometre CMOS IC, HEMT, single electron transistors and resonant tunnelling devices	**1**	1	**1**	**3**	2	**1**
	4. Plan the fabrication procedure for deep-submicron and nanometre CMOS IC with the proper technological process for the materials of the substrate, implanted areas, isolation, metallisation.	**2**	**2**	**2**	1	2	1
	5. Design simple CMOS integrated silicon MEMS sensor devices.	2	2	2	2	1	**3**

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Project Management **Contact:** 3L+1T / Week	**Session:**2021-2022 **Semester:** II **Course Code:** PGMVD205 **Target Student:** PG **Name of the faculty:** Prof. Amitabha Sinha **Credit:** 4

Pre-requisites: Basic concept of Management

1. Introduction to Project : (2 Hrs)
Definition of project, Characteristics of project, Stages of a project, project performance, Performance dimensions, Project development life cycle, Example of a real project, Where is project management applied. Factors for successful completion of a Project.

2. Project Management (5 Hrs)
What is Project Management, Project management objective, Different stages of Project management (conceptualization phase, Planning Phase, Execution Phase, Termination phase), Life cycle path,

Project classification, benefits of project management, Concerns about Project management, What is scope creep, How to Manage Project scope, Some examples about scope creep.

3.Project Identification & Formulation: (5 Hrs)

Project identification, Project Formulation (Opportunity Studies/Support Studies: Identification of Product / Service, Prefeasibility Study, Feasibility Study (Techno Economic Feasibility), Financial Analysis, Project Appraisal, Writing a feasibility study report, Detailed Project Report, Risk and uncertainty, Some examples of risk, The importance of a business case, Risk identification, Types of risk, Risk assessment, Identify the risks, Risk analysis, Negating risks and responding to threats, Identifying and using positive risk.

4. Project Management Techniques: (6 Hrs)

Bar Charts, Gantt chart, Milestone Chart, Networks, Programme Evaluation and Review Technique (PERT), Steps For Network Analysis (Prepare the list of activities 2. Define the inter relationship among the activities. 3. Estimate the activity duration 4. Assemble the activities in the form of a flow diagram 5. Draw the network 6. Analyze the network i.e. compute EST and LST; identify critical events, critical path and critical activities), Project Management tool

5. Network Analysis: (4 Hrs)

Basic concept of Network Analysis, Event numbering. Computation of the Earliest Start Time (EST), Computation of the Latest Start Time (LST), Computation of Earliest Finish Time (EFT), Computation of the Latest Finish Time (LFT), Identification of Critical Path, Computation of Slack or Float

6. Project Crashing & Control (4 Hrs)

Time-Cost Relationship of an activity , Project crashing , Project Control (Fixing up the Review Period , Obtaining Progress Information, Comparing Actual Progress with the Schedule, Taking Appropriate Corrective actions, Reporting to Higher Management, Updating: Conventions for Updating & Frequency of Updating , Redrawing Network , Review, documentation, Fixing up the review period: Obtaining progress information:, Project Management Tools (MS PM tool), Tools for control, Benchmarking, Procedures, Project Scheduling, Gantt charts

7. Interpersonal Relationships (4 Hrs)

Understanding communication, Types of communication, Communication methods ,Communication systems and techniques, verbal communication Miscommunication, Setting up communications systems in projects, identification of stakeholders, Active listening ,Conflict, Conflict management, Finding the right staff, formations of Teams.

Text Books:

1.Project Management Theory And Practice by Gary L. Richardson Brad M. Jackson, Taylor & Francis Ltd,3rd edition
2.Project Management – Nagarajan ,New age International Pvt. Limited Reference

Reference Book:
1.Project Management– Lecture notes by A.Sinha

COURSE OUTCOME(CO)

After completion of this course students are able

1. To learn the definition of project, stages, project development life cycle and the successful development of the project's procedures of initiation, planning, execution, regulation and closure.
2. To learn the concept of project planning, execution, performance monitoring & control and closing.

3. To learn in details about the project objective and life cycle path including work breakdown structure (WBS), estimation of work packages, deliverables & Documentation
4. To learn how to identify a project with specific objectives and justifications and to formulate and present a project idea for the purpose of determining in definitive terms, to learn Network Analysis, Identification of Critical Path and Project Management Tools (MS PM tool, Tools for control, Benchmarking, Procedures and Project Scheduling).
5. To learn different Project Management techniques, to prepare the list of activities and to define the inter relationship among the activities and estimation, to learn interpersonal relationship and Communication techniques among team members as well as stakeholders

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	**2**	**3**	**4**	**5**	**6**
Project Management	1.learn the definition of project, stages, project development life cycle and the successful development of the project's procedures of initiation, planning, execution, regulation and closure.	1	2	2	2	1	1
	2. To learn the concept of project planning, execution, performance monitoring & control and closing.	1	3	2	3	2	1
	3. To learn in details about the project objective and life cycle path including work breakdown structure (WBS), estimation of work packages, deliverables & Documentation	1	3	2	3	2	1
	4. To learn how to identify a project with specific objectives and justifications and to formulate and present a project idea for the purpose of determining in definitive terms, to learn Network Analysis, Identification of Critical Path and Project Management Tools (MS PM tool, Tools for control, Benchmarking, Procedures and Project Scheduling).	1	3	3	3	2	1
	5. To learn different Project Management techniques, to prepare the list of activities and to define the inter relationship among the activities and estimation, to learn interpersonal relationship and Communication techniques among team members as well as stakeholders	2	3	3	3	3	1

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Microelectronics Lab-II **Contact:** 3P / Week **Credit:** 2	**Session:**2021-2022 **Semester:** II **Course Code:** PGMVD291 **Target Student:** PG **Name of the faculty:** Dr. Madhumita Das Sarkar

Course Outcomes:
After completion of this course students are able to
CO1. Familiar about capacitance-voltage characteristics and electrical parameters of the device under test.
CO2. Understand about design and Simulation of the circuit using Multisim software.
CO3. Familiar about HMS3000 Hall Effect Measurement system and how to determination of p-type/n-type semiconductor using the system.
CO4. Understand the capacitance or inductance curve of DUT by varying the frequency.
CO5. Familiar about Surface treatment of silicon wafer.

1. Identify the three pins of the device under test. Draw the capacitance-voltage characteristics across the highly doped and least doped junctions. Extract barrier height, doping concentration, and other parameters. Comment on it and conclude.

Measurement Condition:

a) Device under test: p-n junction Diode(IN4007)
b) Instrumental Frequency: 1Khz ,100KHz, 1MHZ
c) Modes of measurement :Cp-D, Cp-Rp, Cp-Q, Cp, OR Cs-D, Cs-Rs, Cs-Q, Cs
d) BIAS Voltage :0-5V (reverse bias)

2. Identify the components needed to build a low pass filter. Simulate the circuit using analysis program Multisim and build the circuit on NI ELVIS II board to find the output waveform . Comment on it and conclude.

3. Identify the device under test and draw its current-voltage Characteristics and state what electrical parametaers you can find out from the curve. Comment on it and conclude.

4.Identify the three pins of the device. Draw the current -voltage characteristics of the device and state what electrical parameters you can find out from the curve. Comment on it and conclude.

5. Surface treatment of silicon wafer by Annealing process.

6. Determination of p-type/n-type semiconductor and their characteristics using HMS3000 Hall Effect Measurement system.

7.Study on the capacitance or inductance curve of DUT by varrying the frequency up to 1MHz. Find

the dissipation and the quality factor for the components. Comment on the curve to find its functionality?
Measurement Conditions: For DUT

Instrumental Frequency Range : 20Hz to 2MHz
Modes of measurement : Cp-D, Cp-Rp, Cp-Q, Cp or Cs-D, Cs-Rs, Cs-Q, Cs
Measurement Conditions: For DUT

Instrumental Frequency Range : 20Hz to 2MHz
Modes of measurement : Lp-D, Lp-Rp, Lp-Q, Lp or Ls-D, Ls-Rs, Ls-Q, Ls

9.Identify the device and its contacts. Draw the capacitance-voltage characteristics across the junction. Extract barrier height, doping concentration, and other parameters. Comment on it and conclude.
Measurement Conditions:

a) Device under test : p-n junction Diode(IN4007)
b) Instrumental Frequency : 1KHz, 100KHz, 1MHz
c) Modes of measurement : Cp-D, Cp-Rp, Cp-Q, Cp or Cs-D, Cs-Rs, Cs-Q, Cs
d) Bias Voltage : 0 to 5V (reverse bias)

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Microelectronics Lab-II	CO1. Familiar about capacitance-voltage characteristics and electrical parameters of the device under test.	2	2	3	2	3	2
	CO2. Understand about design and Simulation of the circuit using Multisim software.	1	2	3	2	3	3
	CO3. Familiar about HMS3000 Hall Effect Measurement system and how to determination of p-type/n-type semiconductor using the system.	1	2	2	2	3	2
	CO4. Understand the capacitance or inductance curve of DUT by varying the frequency.	1	2	2	3	3	2
	CO5. Familiar about Surface treatment of silicon wafer.	1	2	3	3	3	2

Department: Microelectronics and VLSI Technology Year:1st Course Name: VLSI Design lab II Contact: 3P / Week Credit: 2	Session:2021-2022 Semester: II Course Code: PGMVD292 Target Student: PG Name of the faculty: Dr. Mihir Mahata

Pre-requisites:
Student should have basic familiarity with analog circuit & VLSI design and should have knowledge about the **cadence virtuoso**.

Course Objective:
1. Student will be familiar about VLSI Tools like LT-Spice and cadence virtuoso for Schematic and Layout design.
2. Student will be able to design circuit on cadence virtuoso using the schematic editor window. They will be able to simulate circuit by launching ADE-L in the schematic editor window.
3. Student will be able to do transient, dc and ac analysis.
4. Student will be able to do circuit verification. The layout for the schematic has to be prepared using Layout-XL, and the same has to be physically verified.

COURSE OUTCOMEs(CO)

After completion of this course students are able to
CO1. Familiar about VLSI Tool like cadence virtuoso.
CO2. Design analog circuit using schematic editor window and also able to test the design.
CO3. Extract the Layout of analog circuits and CMOS circuits using Layout-XL.
CO4. Do transient, dc and ac analysis of the designed circuit using cadence virtuoso.
CO5. Understand the DRC check, LVS and RC Extraction, design circuits on LT-Spice Tool and able to test it, familiar about LT-Spice Tool.

List of Lab Assignments:

List of Lab assignments with LT-Spice and cadence virtuoso:

1. i) Familiar with VLSI Design Tools like: LT-Spice and cadence virtuoso, ii) Design the schematic of an Inverter using **cadence virtuoso** and verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

2. Design and simulate the schematic of the common source amplifier. And verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

3. Design and simulate the schematic of the common drain amplifier, and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

4. Design and simulate the schematic of a stage differential amplifier and perform the physical verification for the layout of the same. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

5. Design and simulate the schematic of the operational amplifier and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

6. Design and simulate the schematic of the of cascode current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

7. Design and simulate the schematic of wilson current mirror and perform the physical verification. Verify the following: DC Analysis, Transient Analysis. Extract the layout and verify the DRC, LVS, RC Extraction.

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
VLSI Design Lab-II	CO1. Familiar about VLSI Tool like cadence virtuoso.	2	2	3	2	3	2
	CO2. Design analog circuit using schematic editor window and also able to test the design.	1	2	3	2	3	3
	CO3. Extract the Layout of analog circuits and CMOS circuits using Layout-XL.	1	2	2	2	3	2
	CO4. Do transient, dc and ac analysis of the designed circuit using cadence virtuoso.	1	2	2	3	3	2
	CO5. Understand the DRC check, LVS and RC Extraction, design circuits on LT-Spice Tool and able to test it, familiar about LT-Spice Tool.	1	2	3	3	3	2

SEMESTER – III

Department: Microelectronics and VLSI Technology **Year:** 1st **Course Name:** Algorithms **Contact:** 3L+1T / Week **Credit:** 4	**Session:** 2021-2022 **Semester:** III **Course Code:** PGMVD301A **Target Student:** PG **Name of the faculty:** Mr. Sowvik Dey.

Prerequisite*: Concept of Programming, mathematical concepts such as: Logarithms, Graph Theory.*

Course content:

Module 1: Introduction to Algorithms (7): Concept of Algorithm, The role of algorithm in computing, Fundamentals of Algorithm, Important Types of Algorithm, Fundamental Data Structures. Introduction Analysis Framework, Methodologies for Analyzing Algorithms, Amortization, and Case Studies in Algorithm Analysis. Asymptotic Notations and Basic Efficiency Classes, Mathematical Analysis of Non recursive Algorithms. Mathematical Analysis of Recursive Algorithms, empirical Analysis of Algorithms, Algorithm visualization.

Module 2: Graph Algorithms (7): Graph search Algorithms, Spanning tree Algorithm, Shortest path Algorithm, Matching Algorithm, Min cut and Max cut Algorithms and Steiner Tree Algorithm.

Module 3: NP-Complete Problem (8): NP-class of problems, P-class problems, NP=P question, Polynomial problem reduction (Reducibility), Cook's theorem, NP-hardness and NP-completeness, NP-completeness FAQ including how to handle NP-hard problems, Examples of NP-completeness proofs: SAT to 3-SAT, Polynomial-time non-deterministic algorithms, Maximum Clique Problem.

Module 4: High Level Synthesis (8): Steps of VLSI Design flow, Steps of High Level Synthesis. Data Dependency graphs. Scheduling Algorithms, Allocation and binding: Conflict Graph, Compatibility Graph, left Edge Algorithm, Data path and Controller Synthesis. Secure Design with HLS: different methods of obfuscation. Logic level Synthesis. Line sweep method. Graph Algorithms for physical design: Classes of graphs in physical design, relationship between graph classes, graph problems, Algorithms for interval graphs.

Module 5: Partitioning (2): Group migration Algorithms. Floor planning and Pin assignment: Slicing, Non-Slicing.

Module 6: Placement (2): Simulated annealing, simulated evolutions, force directed placement,

sequence pair technique.

Module 7: Routing (6): Routing Algorithms. Shortest path algorithm, Steiner tree based Algorithm. Single layer routing Algorithms and two layer routing Algorithms. Over the cell routing, Via minimization, clock, power and ground routing. Topological Sort.

Suggested books

1. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation" 3rd edition, Springer international, 1998.
2. Pinaki Mazumber, Elizabeth M Rudnick, "Genetic Algorithms For VLSI Design, Layout & Test Automation", Pearson education, 2007.
3. Ellis Horowitz, sartajsahni, Sanguthevar Rajasekaran, "Fundamentals of Computer Algorithms" Universities Press.
4. Thomas H Cormen, Charles E Lieserson, Ronald L Rivest and Clifford Stein, "Introduction to Algorithms", 4TH Edition, MIT Press/McGraw-Hill.

Suggested references

1. Jon Kleinberg and ÉvaTardos, "Algorithm Design", 1ST Edition, Pearson.
2. Michael T Goodrich and Roberto Tamassia, "Algorithm Design: Foundations, Analysis, and Internet Examples", Second Edition, Wiley.
3. Udi Manber, Addison-Wesley, "Algorithms -- A Creative Approach", 3RD Edition, Addison-Wesley Publishing Company.
4. "C-Based VLSI Design" lecture note of prof. Chandan Karfa, IIT Guwahati.

COURSE OUTCOME(CO)

After completion of this course students are able to

CO1. Understand Different aspects of Algorithms: Complexity, Notations, Analysis.
CO2. Understand and apply graph minimization algorithms on VLSI net-lists in Structural Design.
CO3. Write code for algorithms used in computational and geometrical simplification and optimization using data structures for CAD tools.
CO4. Understand and write code for partitioning, floor planning, chip planning and pin assignment, routing of cells, clock and power supply.
CO5. Understand different algorithms used for placement of cells during the physical design of a chip.

CO-PO Mapping

Subject	Course Outcomes	Program Outcomes					
		1	2	3	4	5	6
Algorithms	CO1. Understand Different aspects of Algorithms: Complexity, Notations, Analysis.	3	3	2	1	2	2
	CO2. Understand and apply graph minimization algorithms on VLSI	3	3	3	2	2	2

	net-lists in Structural Design.						
	CO3. Write code for algorithms used in computational and geometrical simplification and optimization using data structures for CAD tools.	2	2	3	2	3	2
	CO4. Understand and write code for partitioning, floor planning, chip planning and pin assignment, routing of cells, clock and power supply.	3	2	3	3	1	2
	CO5. Understand different algorithms used for placement of cells during the physical design of a chip.	3	2	3	3	1	2