(*) Sequential Logic

^ The outputs of a COMBINATIONAL circuit at ANY instant of time are ENTIRELY dependent upon the inputs present at THAT time, taking into account the PROPAGATION delays.

However, in a SEQUENTIAL circuit, MEMORY elements are present as well.
The information stored in the MEMORY elements at any given time defines the present INTERNAL STATE of the sequential circuit.
The external OUTPUTS and the next INTERNAL STATE of a sequential circuit are both functions of the external INPUTS and the present INTERNAL STATE.
Thus, a sequential circuit is specified by a time sequence of EXTERNAL INPUTS, EXTERNAL OUTPUTS and INTERNAL STATES.

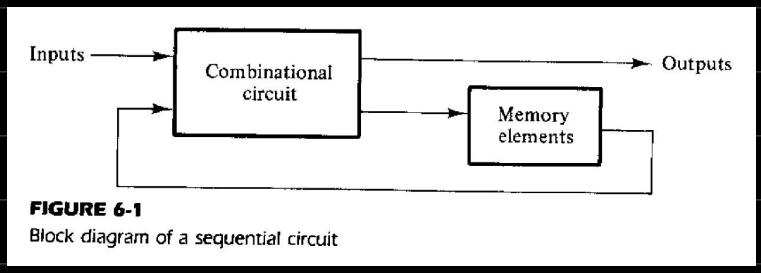

FIGURE 6-1
Block diagram of a sequential circuit

^ A SYNCHRONOUS sequential circuit is a system whose behaviour can be defined from the knowledge of its signals at DISCRETE instants of time.
The behaviour of an ASYNCHRONOUS sequential circuit depends upon the ORDER in which its input signals change and can be affected at ANY instant of time.
So, the behaviour of an ASYNCHRONOUS sequential circuit CANNOT be defined at DISCRETE instants of time.

The MEMORY elements used in ASYNCHRONOUS sequential circuits are TIME-DELAY devices, whose memory capability is due to the FINITE amounts of time it takes for signals to PROPAGATE through devices. Instead of using physical time-delay devices, LOGIC GATES may also be used to produce the SAME effect due to their internal PROPAGATION delays.

Thus, an ASYNCHRONOUS sequential circuit may be regarded as a COMBINATIONAL circuit with FEEDBACK. Because of the feedback among logic gates, an asynchronous sequential circuit may, at times, become UNSTABLE.

In a SYNCHRONOUS sequential circuit, signals may affect the MEMORY elements only at DISCRETE instants of time. One way of achieving this goal is by using a timing device called a MASTER-CLOCK generator, which generates a periodic train of CLOCK PULSES, i.e. an input signal which goes to 0 to 1 to 0 to 1 and so forth PERIODICALLY.
In practical circuits, the MEMORY elements are affected ONLY with the ARRIVAL of a pulse, i.e. IMMEDIATELY after the clock goes from 0 to 1 (i.e. the POSITIVE edge transition) or from 1 to 0 (i.e. the NEGATIVE edge transition), depending upon the implementation, and NOT during the ENTIRE time the clock stays at 1 or 0.
Such circuits are called CLOCKED sequential circuits.

The memory elements used in CLOCKED sequential circuits are called FLIP-FLOPS.
The basic difference between a LATCH and a FLIP-FLOP is that a LATCH is LEVEL-SENSITIVE, i.e. the outputs of a LATCH respond to the new inputs AT ALL TIMES, whereas a FLIP-FLOP is EDGE-TRIGGERED, i.e. the outputs of a FLIP-FLOP respond to the new inputs ONLY during the positive/negative EDGE TRANSITIONS of the clock.
Hence, LATCHES are examples of ASYNCHRONOUS sequential circuits, whereas FLIP-FLOPS are examples of SYNCHRONOUS sequential circuits.

Note that 'DURING an edge transition' means 'IMMEDIATELY AFTER the clock goes to 1 or to 0', depending upon the implementation.

For some reason, the book calls the SR, D, JK and T latches as flip-flops, even though their outputs may change the ENTIRE time the clock is high, and NOT ONLY during the EDGE-TRANSITIONS.

^ A LATCH / FLIP-FLOP is a memory element capable of storing 1 BIT of information.

Each latch / flip-flop has 2 inputs, S & R, and 2 outputs, Q & Q'.

When Q = 1 & Q' = 0, the state is SET, and when Q = 0 & Q' = 1, the state is RESET.

In the beginning, when power is turned on, a latch / flip-flop can result in either the SET state or the RESET state, depending upon the initial values of the signals.

^ SR Latch (aka DIRECT-COUPLED RS Flip-Flop, even though it is technically a LATCH)