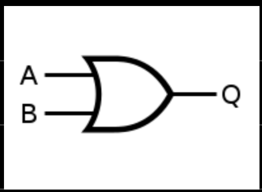
(*) Sequential Logic

^ IMMEDIATELY AFTER a circuit is CLOSED, while the initial PROPAGATIONS have NOT completed, the values on the wires (except for those which are DIRECTLY fixed to 0's/1's) will be FLOATING (at 0, 1 or somewhere between 0 & 1, or oscillating among 0, 1 and somewhere between 0 & 1), including the signal generated by the MASTER-CLOCK generator (discussed later).

In GENERAL, for EVERY logic gate, its OUTPUT will become 0/1 only AFTER its INPUT(s) become(s) 0/1 (including FLOATING at 0/1) and AFTER its PROPAGATION DELAY.
Also, if its INPUT(s) later become FLOATING somewhere between 0 & 1, then AFTER its PROPAGATION DELAY, its OUTPUT will also become FLOATING (at 0, 1 or somewhere between 0 & 1, or oscillating among 0, 1 and somewhere between 0 & 1) if its OUTPUT is NOT being driven by some OTHER component.



For eg., if the PROPAGATION DELAY of this OR gate is 20 ns, if A & B are FIXED to 1's, and if the circuit is CLOSED at t = 0, then Q will be FLOATING from t = 0 to t = 20 and will be 1 AFTER t = 20.

For eg., if ONE input of an OR gate becomes 1 (including FLOATING at 1), then after its PROPAGATION delay, its OUTPUT will become 1 IRRESPECTIVE of the OTHER input (even if that OTHER input is FLOATING (at 0, 1 or somewhere between 0 & 1, or oscillating among 0, 1 and somewhere between 0 & 1)).
However, if ONE input of an OR gate becomes 0 (including FLOATING at 0) and the OTHER input becomes FLOATING somewhere between 0 & 1, or if BOTH inputs become FLOATING somewhere between 0 & 1, then after its PROPAGATION delay, its OUTPUT will become FLOATING (at 0, 1 or somewhere between 0 & 1, or oscillating among 0, 1 and somewhere between 0 & 1) if its OUTPUT is NOT being driven by some OTHER component.

An INPUT of a LOGIC GATE will be FLOATING (at 0, 1 or somewhere between 0 & 1, or oscillating among 0, 1 and somewhere between 0 & 1) if

1. it is DISCONNECTED
2. if the OUTPUT (of some OTHER logic gate) which is driving this INPUT is FLOATING (at 0, 1 or somewhere between 0 & 1, or oscillating among 0, 1 and somewhere between 0 & 1)
3. etc.

A FLOATING value MAY at times float at 0/1, but an ACTUAL 0/1 will REMAIN constant until it gets CHANGED (after, for eg., the corresponding PROPAGATION DELAY(s) due to the INPUTS of logic gates getting changed), whereas a FLOATING value MAY get changed ARBITRARILY.

Thus, an OSCILLATING signal (for eg., from a MASTER-CLOCK generator) oscillating between 0 & 1 oscillates due to, for eg., the INPUTS of logic gates getting CHANGED, which is DIFFERENT from a FLOATING value, which MAY oscillate among 0, 1 and somewhere between 0 & 1 ARBITRARILY.

Also, when a signal gets CHANGED from 0/1 to 1/0, it goes from 0/1 to somewhere between 0 & 1, and then to 1/0.

Again, this TRANSITIONING phase is DIFFERENT from FLOATING, as the DURATION of this phase in NEGLIGIBLE and the signal gets CHANGED from 0/1 to 1/0 almost INSTANTANEOUSLY.

A FLOATING value which is FLOATING at 0/1 is ALSO considered to be 0/1.

So, for eg., when an EXTERNAL input signal (such as the S or R input of an SR latch) is said to be 0/1, it is IMPLIED that this ALSO includes FLOATING at 0/1.

^ The outputs of a COMBINATIONAL circuit at ANY instant of time are ENTIRELY dependent upon the inputs present at THAT time, taking into account the PROPAGATION delays.

However, in a SEQUENTIAL circuit, MEMORY elements are present as well.
The information stored in the MEMORY elements at any given time defines the STATE of the sequential circuit at THAT time.
The external OUTPUTS and the next STATE of a sequential circuit are both functions of the external INPUTS and the present STATE.
Thus, a sequential circuit is specified by a time sequence of EXTERNAL INPUTS, EXTERNAL OUTPUTS and STATES.

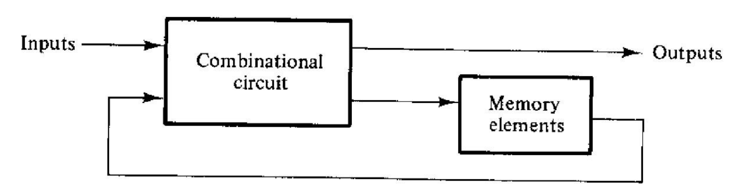


FIGURE 6-1
Block diagram of a sequential circuit

A SYNCHRONOUS sequential circuit is a system whose BEHAVIOUR can be DEFINED from the knowledge of its signals at DISCRETE instants of time.
The BEHAVIOUR of an ASYNCHRONOUS sequential circuit depends upon the ORDER in which its input signals CHANGE and can be affected at ANY instant of time.
So, the BEHAVIOUR of an ASYNCHRONOUS sequential circuit becomes DIFFICULT to be defined at DISCRETE instants of time.

^ The MEMORY elements used in ASYNCHRONOUS sequential circuits are TIME-DELAY devices, whose memory capabilities are due to the FINITE amounts of time signals take to PROPAGATE through devices.
Instead of using PHYSICAL time-delay devices, LOGIC GATES may also be used to produce SIMILAR effects due to their internal PROPAGATION delays.

Thus, an ASYNCHRONOUS sequential circuit may be regarded as a COMBINATIONAL circuit with FEEDBACK. Because of the FEEDBACK among logic gates, an ASYNCHRONOUS sequential circuit MAY, at times, become UNSTABLE.

^ In SYNCHRONOUS sequential circuits, signals may affect the MEMORY elements ONLY at DISCRETE instants of time.
ONE way of achieving this goal is by using a MASTER–CLOCK generator, and a circuit which uses a MASTER–CLOCK generator is known as a CLOCKED SYNCHRONOUS sequential circuit.

A MASTER–CLOCK generator is a TIMING device which generates a PERIODIC train of CLOCK PULSES, i.e. a signal which goes to 0 to 1 to 0 to 1 and so forth PERIODICALLY.
This OSCILLATING signal becomes the MAIN CLOCK of a circuit.

In practical circuits, the MEMORY elements are affected ONLY with the ARRIVAL of a pulse, i.e. IMMEDIATELY after the CLOCK goes from 0 to 1 (i.e. during the POSITIVE edge–transition) or from 1 to 0 (i.e. during the NEGATIVE edge–transition), depending upon the implementation, and NOT during the ENTIRE time the CLOCK stays at 1/0.

The MEMORY elements used in CLOCKED SYNCHRONOUS sequential circuits are MODIFIED GATED LATCHES and FLIP–FLOPS, which are both EDGE–TRIGGERED.

^ The DIFFERENCE between a LATCH and a FLIP–FLOP is that a LATCH is LEVEL–SENSITIVE, i.e. the outputs of a LATCH respond to NEW inputs AT ALL TIMES, whereas a FLIP–FLOP is EDGE–TRIGGERED, i.e. the outputs of a FLIP–FLOP respond to NEW inputs ONLY during the positive/negative EDGE–TRANSITIONS of the CLOCK.

Hence, in addition to TIME–DELAY devices, LATCHES are also examples of MEMORY elements used in ASYNCHRONOUS sequential circuits.

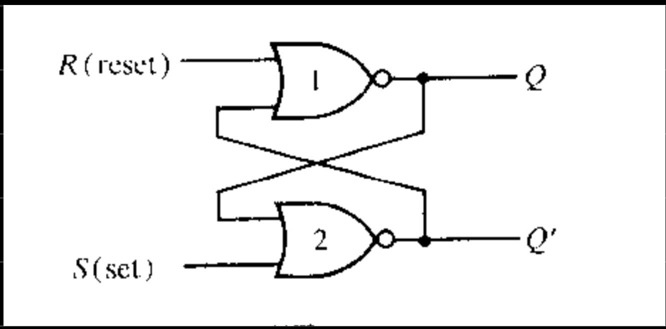
^ Adding a CLOCK input to a LATCH will NOT make it a FLIP–FLOP, as its outputs will respond to NEW inputs during the ENTIRE time the CLOCK stays at 1/0, and will rather make it a GATED LATCH.
Since GATED LATCHES are LEVEL–SENSITIVE but are ALSO used in CLOCKED SYNCHRONOUS sequential circuits, therefore they are MODIFIED in order to become EDGE–TRIGGERED, for eg., by using EDGE–DETECTORS on their CLOCK inputs.

^ A LATCH / GATED LATCH / FLIP–FLOP is a MEMORY element (CELL) capable of storing 1 BIT of information, and can MAINTAIN its state INDEFINITELY (as long as power is delivered to the circuit) UNTIL directed by an input signal to SWITCH states.

Every LATCH / GATED LATCH / FLIP–FLOP has 2 outputs, Q & Q'.
When Q = 1 & Q' = 0, the state is SET, and when Q = 0 & Q' = 1, the state is CLEAR.

Since a LATCH / GATED LATCH / FLIP–FLOP has 2 STABLE states, therefore it is also known as a BISTABLE MULTIVIBRATOR.

^ SR Latch (also known INCORRECTLY as a DIRECT-COUPLED SR/RS Flip-Flop)



After the circuit is CLOSED, the following EDGE cases can occur -

1. Let S, R, Q & Q' be FLOATING somewhere between 0 & 1.
   Now, if S & R both become 0's, even then Q & Q' will remain FLOATING somewhere between 0 & 1, and this behaviour is SIMILAR to the one previously described for an OR gate.
2. Let S & R be FLOATING somewhere between 0 & 1, and let Q & Q' be FLOATING at 0's.
   Now, if S & R both become 0's SIMULTANEOUSLY, then

Explain floating and oscillating states even if S and R become 0.

the initial oscillating state is similar to the oscillating state after s & r simultaneously becoming 0's after the invalid state.
Even then, s and r becoming 1/0 and 0/1, respectively, will make the latch stable again.

In real-world circuits, the latch will settle down because -

1. see keep notes
2. see keep notes

Now, let S & R become 0. This is the base condition of the inpupts.
Now, let S get changed to 1, IRRESPECTIVE of the current state of the latch,

For every GATED LATCH / FLIP-FLOP, - DEFINE THESE PROPERLY

1. The SETUP time is defined as the DURATION of time for which the input(s) must be kept CONSTANT while CP is at 0 IMMEDIATELY BEFORE CP gets changed from 0 to 1.
2. The HOLD time is defined as the DURATION of time for which the input(s) must be kept CONSTANT while CP is at 1 IMMEDIATELY AFTER CP gets changed from 0 to 1.

For eg., if the DURATION of a clock cycle is 20 units, with the clock staying at 1 & 0 for 10 units each and the clock transitioning from 0 to 1 at t = 20 T, where T is an integer, and if the SETUP & HOLD times of a flip-flop are 2 units & 1 unit, respectively, then the input(s) must be kept CONSTANT from t = (20 T - 2) to t = (20 T + 1).

It should be noted that the ARRIVAL of the input(s) EXACTLY at t = (20 T - 2) and the CHANGING of the inputs EXACTLY at t = (20 T + 1) may work IDEALLY, but MAY or MAY NOT work in REAL-WORLD circuits. So, the input(s) must arrive slightly BEFORE t = (20 T - 2) and must be allowed to change only slightly AFTER t = (20 T + 1).

In a circuit, the DURATION of a clock cycle is made LONG ENOUGH for signals to PROPAGATE and for the ENTIRE circuit to become STABLE before the MAIN CLOCK gets changed from 0/1 to 1/0.

In GENERAL, the data to be loaded into GATED LATCHES / FLIP-FLOPS arrive at the inputs and remain CONSTANT such that the SETUP time and the HOLD time constraints are NOT violated.

^

^

In a REAL-WORLD computer, when the POWER SUPPLY is turned on, a very SMALL circuit gets completed whose job is to DETECT when the POWER BUTTON is pressed.
AFTER the POWER BUTTON is pressed, power gets supplied to the ENTIRE circuit of the computer.

IMMEDIATELY AFTER the POWER BUTTON is pressed, the MAIN CLOCK starts (AFTER the initial PROPAGATIONS within the MASTER-CLOCK generator get completed), and a POWER-ON-RESET generator starts sending ASYNCHRONOUS RESET signals to CLEAR ALL of the FLIP-FLOPS.
After a FEW clock cycles, when the power STABILIZES, the initial PROPAGATIONS for the ENTIRE computer get completed and ALL of the FLIP-FLOPS get CLEARED, the POWER-ON-RESET GENERATOR stops sending the ASYNCHRONOUS RESET signals, and the NORMAL operation of the computer begins from the NEXT clock cycle.

The DE-ASSERTION of the ASYNCHRONOUS RESET signals is generally SYNCHRONISED using a RESET SYNCHRONISER circuit in order to adhere to the RECOVERY time and the REMOVAL time constraints.