



# VISHVADEEP GOTHI SIR

**AIR- 19, 119, 440, 682  
in GATE**



ME from IISc Bangalore ✓  
Mtech BITS Pilani in Data  
Science ✓



14+ Years of Teaching Experience,  
10+ Years in GATE/IES



**Subjects Taken:**  
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data structure, operating system,  
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- GATE AIR-19, 119, 440, 682 - ME from IISc, - MTech BITS Pilani (Data Science) - 14 years experience

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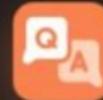
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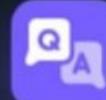


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START DATE

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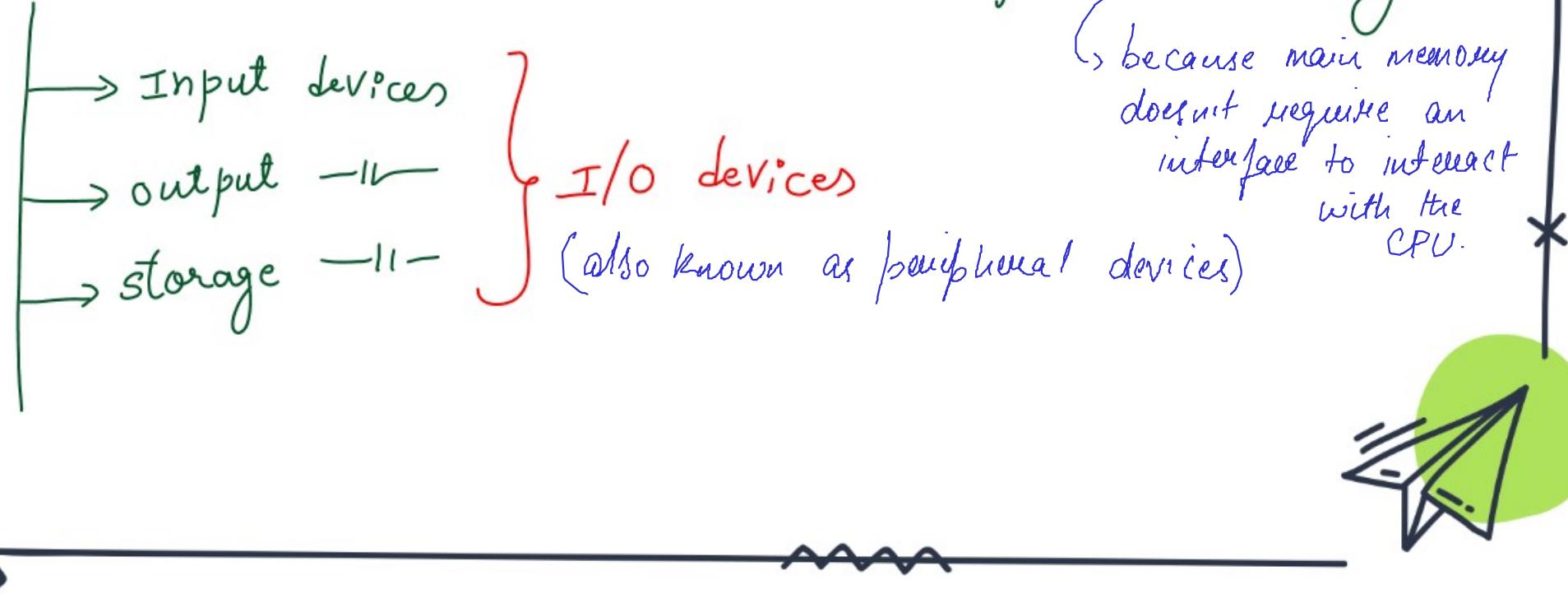
# IO Organization



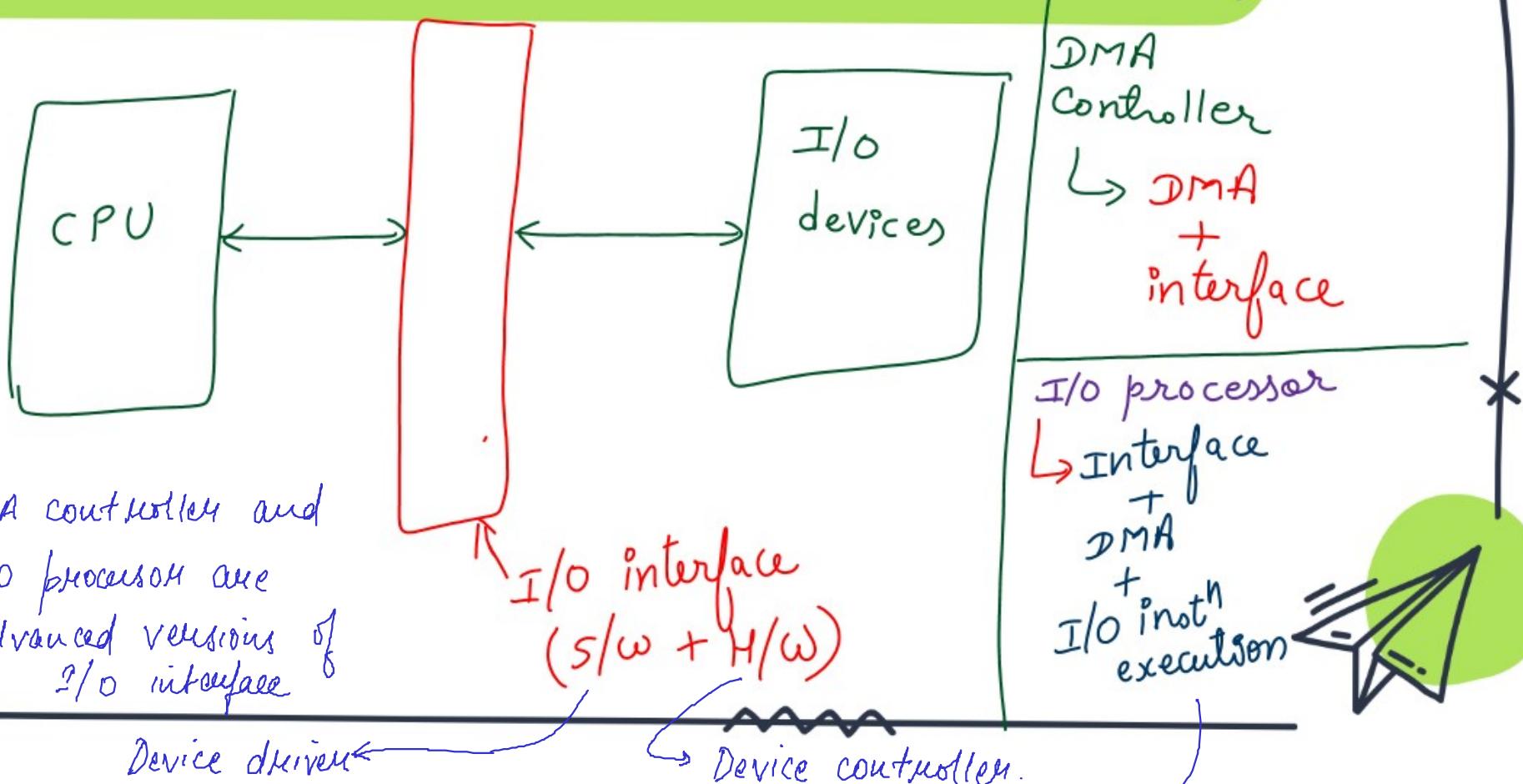
# IO Organization

Peripheral :-

Devices connected to processor externally except main memory



# Can CPU Access IO Directly?



④ For e.g.,  
Graphics card.

Need for

# IO Interface

1. Peripherals are electromechanical or electromagnetic devices; and their manner of operation is different from the operation of the CPU and memory. Which are electronic devices. So conversion of signal required.  
*→ printer                      → hard disk*
2. The data transfer rate of peripherals is usually slow. So synchronization is required. *(to get a common speed of execution)*
3. Data codes and format in peripherals differ from the word format in the CPU and memory. So conversion of formats is required.
4. The operating modes of peripherals are different from each other and each must be controlled so a peripheral does not disturb the operation of other peripherals.



# IO <sup>and</sup> Memory Buses

→ There are 3 ways to connect memory and I/O with CPU through buses.

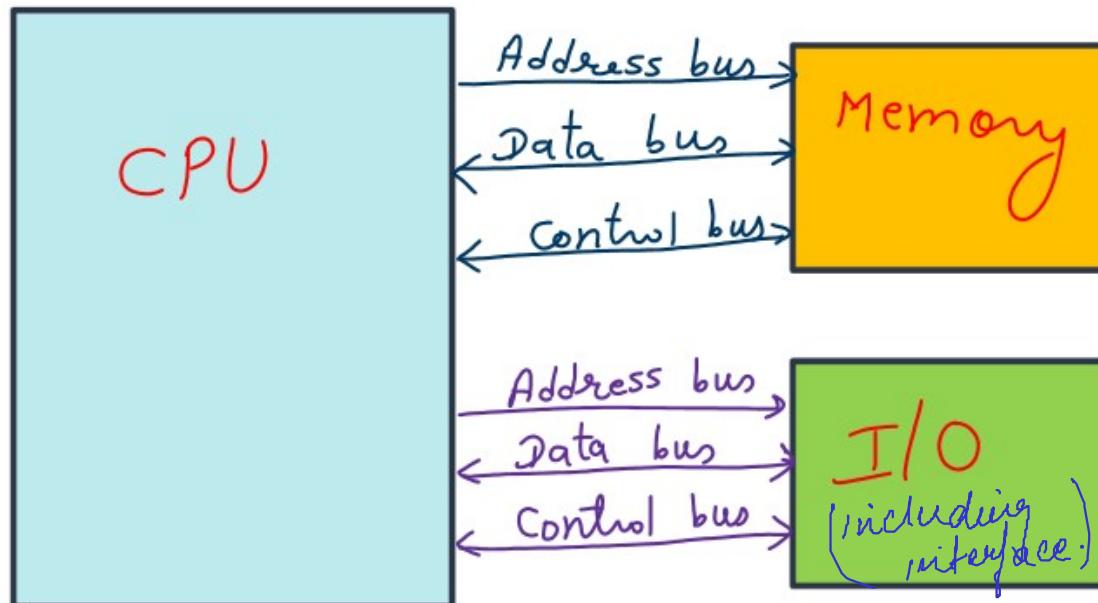
any 1 out of the 3 is used in an actual implementation

① CPU buses - Address, control, data



1.

# Separate Buses for Both



Disadvantage:-



→ Costly

Advantage:-



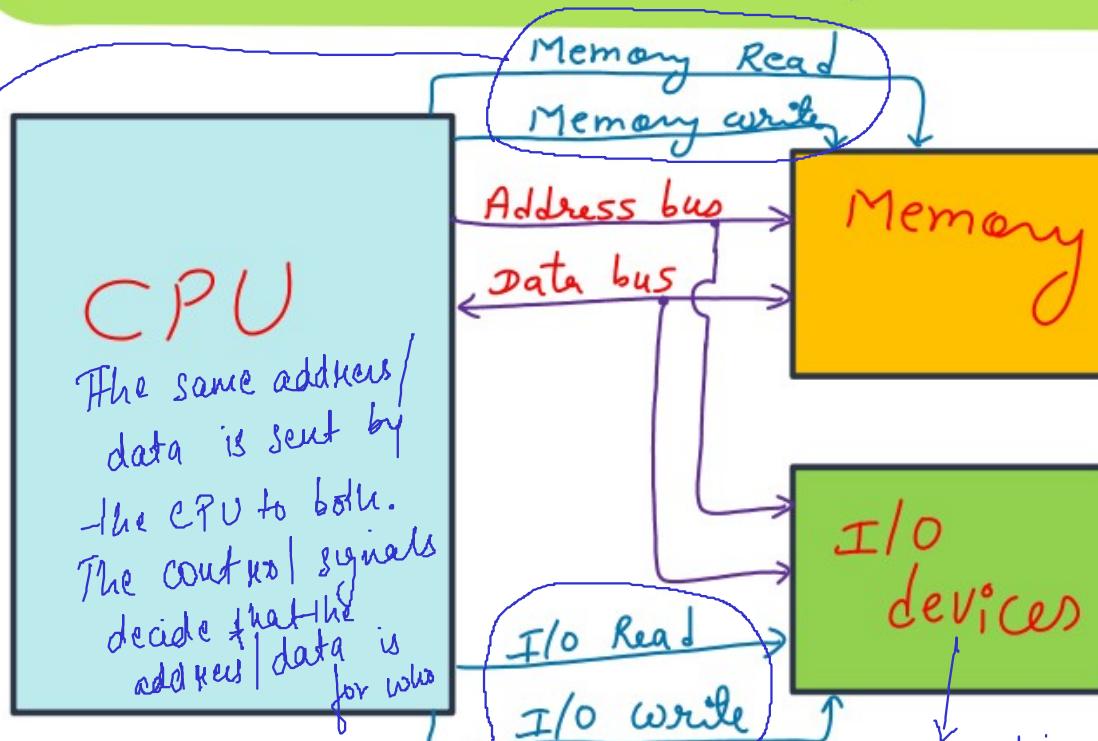
→ Easy to implement



- (K) The control bus is bidirectional, for the CPU to send control signals and to receive response signals / status.

used in most computers

## 2. Common Data, Address Bus

aka  
I/O mapped  
I/O

CPU distinguishes b/w memory and I/O using control signals.

→ I/O devices have their own addresses

↓  
I/O-mapped-I/O  
or  
Isolated I/O

Control signals in addition to these are also present

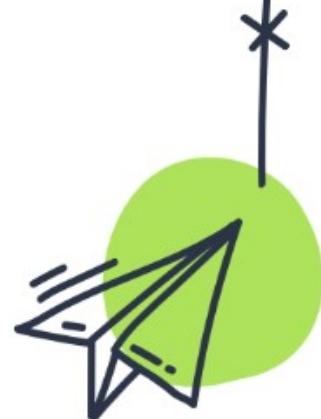
④ In a vertical microprogrammed control unit, these 4 signals can be grouped together, as only 1 out of these will be set to 1 at any time

i.e. the addresses of I/O devices are separate from those of the memory.

# Common Data, Address Bus



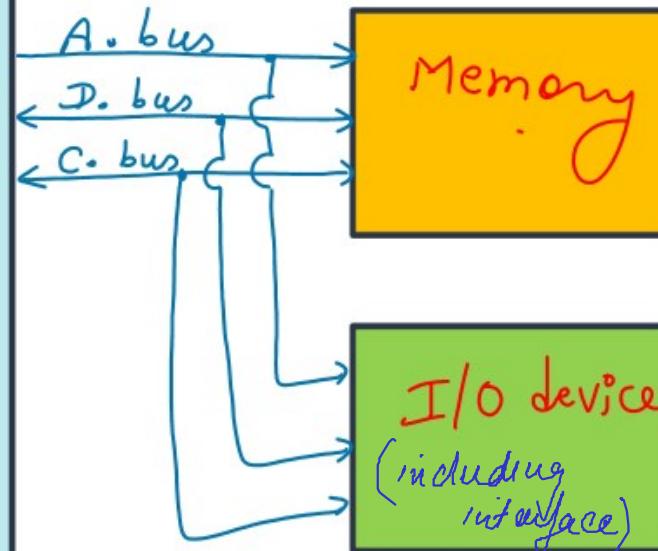
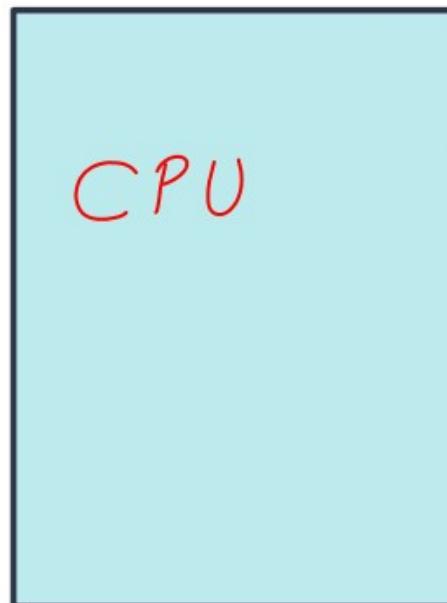
→ No memory wastage, as opposed to the third scheme.



3.

## Common Address, Data & Control Bus

aka  
memory  
mapped  
I/O



wastage of memory space.

### Memory-Mapped I/O

as - the I/O addresses are taken from the memory.



- ④ Memory-mapped I/O uses the same address space to address both main memory and I/O devices. The memory and registers of the I/O devices are mapped to (associated with) address values. So a memory address may refer to either a portion of physical RAM, or instead to memory and registers of the I/O device. Thus, the CPU instructions used to access the memory can also be used for accessing devices.

and addressing modes

# Common Address, Data & Control Bus

Assume memory: 8x8bits, and 2 IO devices D1 and D2

| Memory |   |
|--------|---|
| 000    | ✓ |
| 001    | ✗ |
| 010    | ✓ |
| 011    | ✗ |
| 100    | ✓ |
| 101    | ✓ |
| 110    | ✓ |
| 111    | ✓ |

Some addresses are assigned to I/O devices from memory addresses.

Assume:-

Assigned add      D1      D2      ④ Assuming that D1 and D2 both require only 1 address.

④ The assignment of addresses doesn't mean that those I/O devices will use the memory to store data.

The assignment of addresses is done only for identification.



④ In this scheme, the address bus' value decides whether the read/write is to be done from the I/O devices or from the memory.

# Memory Mapped IO vs IO Mapped IO

| Memory Mapped IO  | IO Mapped IO   |
|---|--|
| 1. Memory wastage   | 1. No Memory wastage   |
| 2. All Memory access instructions used for IO access also | 2. IO access instructions and memory access instructions are different |
| 3. No separate address space for IO                       | 3. IO have their own separate address space                            |
| 4. More Instructions for IO access                        | 4. Less Instructions for IO access                                     |
| 5. More addressing modes for IO access                    | 5. <sup>Less</sup> addressing modes for IO access                      |

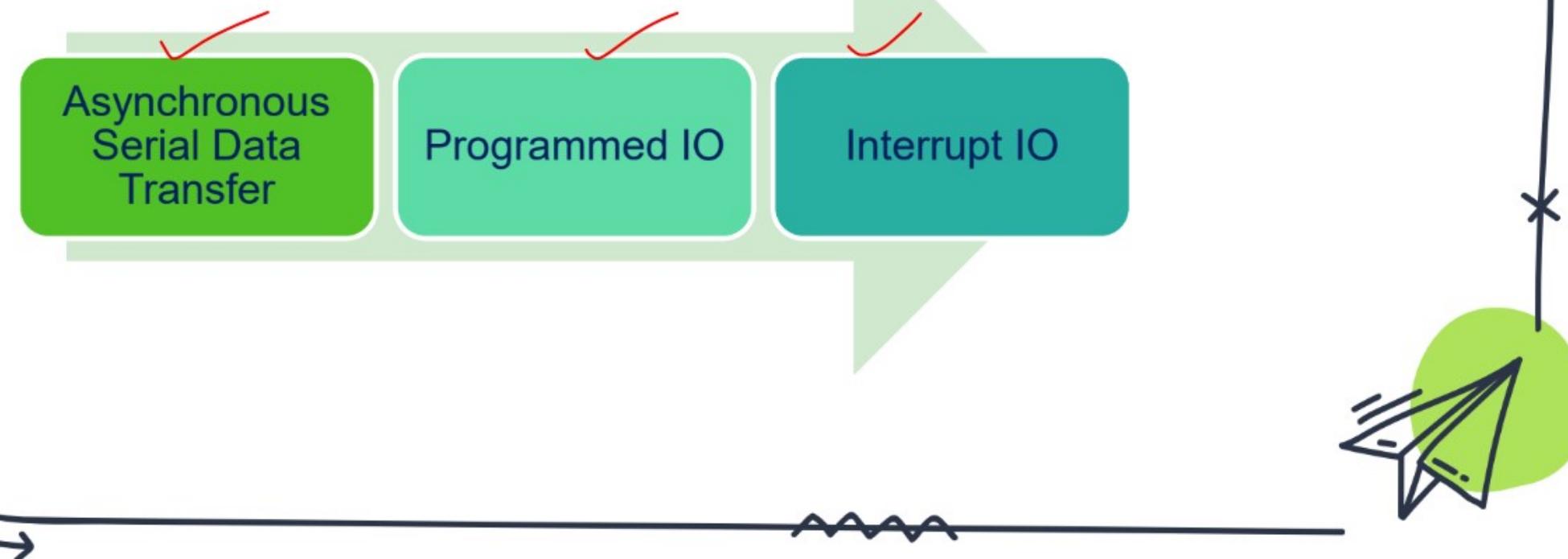


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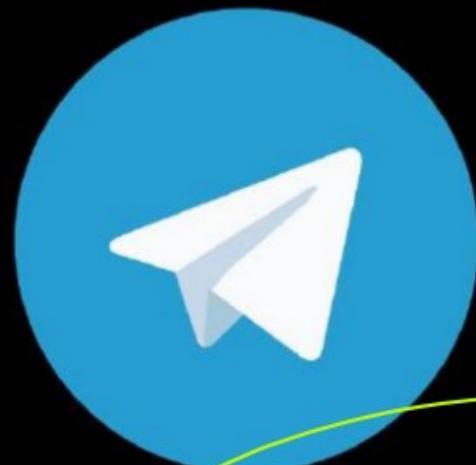


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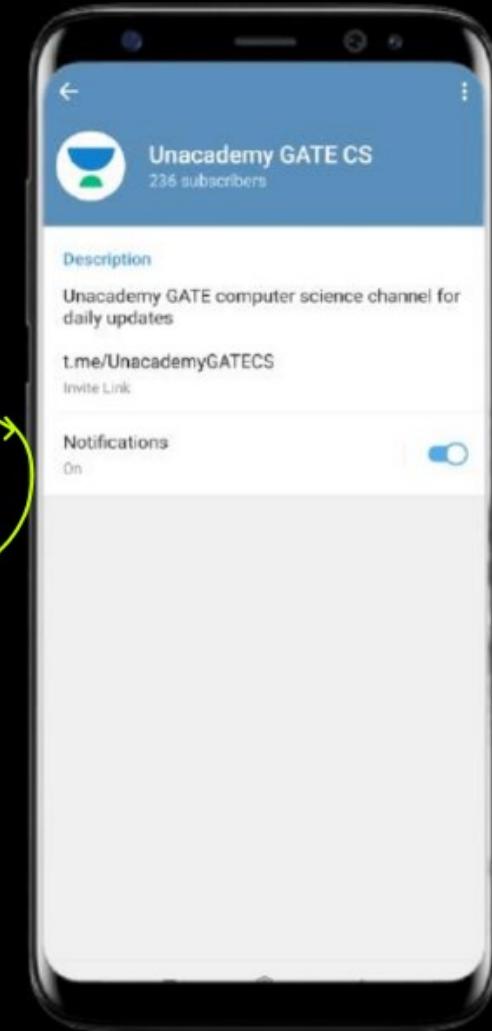
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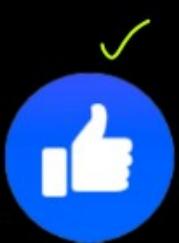
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