(*) Sequential Logic

^ The outputs of a COMBINATIONAL circuit at ANY instant of time are ENTIRELY dependent upon the inputs present at THAT time, taking into account the PROPAGATION delays.

However, in a SEQUENTIAL circuit, MEMORY elements are present as well.
The information stored in the MEMORY elements at any given time defines the present STATE of the sequential circuit.
The external OUTPUTS and the next STATE of a sequential circuit are both functions of the external INPUTS and the present STATE.
Thus, a sequential circuit is specified by a time sequence of EXTERNAL INPUTS, EXTERNAL OUTPUTS and STATES.

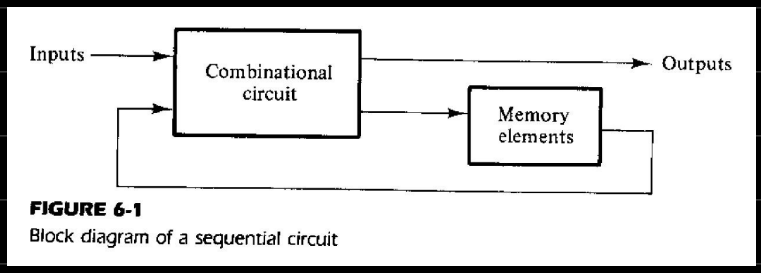

FIGURE 6-1
Block diagram of a sequential circuit

^ A SYNCHRONOUS sequential circuit is a system whose behaviour can be defined from the knowledge of its signals at DISCRETE instants of time.
The behaviour of an ASYNCHRONOUS sequential circuit depends upon the ORDER in which its input signals change and can be affected at ANY instant of time.
So, the behaviour of an ASYNCHRONOUS sequential circuit CANNOT be defined at DISCRETE instants of time.

The MEMORY elements used in ASYNCHRONOUS sequential circuits are TIME-DELAY devices, whose memory capability is due to the FINITE amounts of time it takes for signals to PROPAGATE through devices. Instead of using physical time-delay devices, LOGIC GATES may also be used to produce the SAME effect due to their internal PROPAGATION delays.

Thus, an ASYNCHRONOUS sequential circuit may be regarded as a COMBINATIONAL circuit with FEEDBACK. Because of the feedback among logic gates, an asynchronous sequential circuit may, at times, become UNSTABLE.

In a SYNCHRONOUS sequential circuit, signals may affect the MEMORY elements only at DISCRETE instants of time. One way of achieving this goal is by using a timing device called a MASTER-CLOCK generator, which generates a periodic train of CLOCK PULSES, i.e. an input signal which goes to 0 to 1 to 0 to 1 and so forth PERIODICALLY.
Such circuits are called CLOCKED SYNCHRONOUS sequential circuits.

In practical circuits, the MEMORY elements are affected ONLY with the ARRIVAL of a pulse, i.e. IMMEDIATELY after the clock goes from 0 to 1 (i.e. during the POSITIVE edge transition) or from 1 to 0 (i.e. during the NEGATIVE edge transition), depending upon the implementation, and NOT during the ENTIRE time the clock stays at 1 or 0.
Such circuits are called EDGE-TRIGGERED CLOCKED SYNCHRONOUS sequential circuits, and the MEMORY elements used in such circuits are called FLIP-FLOPS.

The basic difference between a LATCH and a FLIP-FLOP is that a LATCH is LEVEL-SENSITIVE, i.e. the outputs of a LATCH respond to new inputs AT ALL TIMES, whereas a FLIP-FLOP is EDGE-TRIGGERED, i.e. the outputs of a FLIP-FLOP respond to new inputs ONLY during the positive/negative EDGE TRANSITIONS of the clock.
Hence, LATCHES are examples of ASYNCHRONOUS sequential circuits, whereas FLIP-FLOPS are examples of EDGE-TRIGGERED CLOCKED SYNCHRONOUS sequential circuits. Adding a clock input to a latch DOESN'T make it a FLIP-FLOP, as its outputs will respond to new inputs during the ENTIRE time the clock stays at 1, and rather makes it a GATED LATCH, which is an example of a LEVEL-SENSITIVE CLOCKED SYNCHRONOUS sequential circuit.

Note that 'DURING an edge transition' means 'IMMEDIATELY AFTER the clock goes from 0 to 1 or from 1 to 0', depending upon the implementation.

^ A LATCH / FLIP-FLOP is a memory element (CELL) capable of storing 1 BIT of information.

Each latch / flip-flop has 2 outputs, Q & Q'.
When Q = 1 & Q' = 0, the state is SET, and when Q = 0 & Q' = 1, the state is CLEAR.

In the beginning, when power is turned on, a latch / flip-flop GENERALLY results in either a STABLE SET state or a STABLE RESET state.
However, it MAY also result in an UNSTABLE OSCILLATING state.
Thus, in the beginning, GENERALLY, every latch / flip-flop is CLEARED, for eg., by using DIRECT CLEAR inputs, BEFORE the normal operation of the computer begins.

^ For every CLOCKED SYNCHRONOUS memory element (i.e. GATED LATCH / FLIP-FLOP),
1. The SETUP time is defined as the DURATION of time for which the input(s) must be kept CONSTANT while CP is at 0 IMMEDIATELY BEFORE CP gets changed from 0 to 1.
2. The HOLD time is defined as the DURATION of time for which the input(s) must be kept CONSTANT while CP is at 1 IMMEDIATELY AFTER CP gets changed from 0 to 1.

For eg., if the DURATION of a clock cycle is 20 units, with the clock staying at 1 & 0 for 10 units each and the clock transitioning from 0 to 1 at t = 20 T, where T is an integer, and if the SETUP & HOLD times of a flip-flop are 2 units & 1 unit, respectively, then the input(s) must be kept CONSTANT from t = (20 T − 2) to t = (20 T + 1).

It should be noted that the ARRIVAL of the input(s) EXACTLY at t = (20 T − 2) and the CHANGING of the inputs EXACTLY at t = (20 T + 1) may work IDEALLY, but MAY or MAY NOT work in REAL-WORLD circuits. So, the input(s) must arrive slightly BEFORE t = (20 T − 2) and must be allowed to change only slightly AFTER t = (20 T + 1).

In REAL-WORLD circuits, the duration of a clock cycle is MUCH MORE than this.

In GENERAL, the data to be loaded into truly POSITIVE edge-triggered flip-flops in the NEXT clock cycle arrive at the inputs while the clock is 0, while the clock was previously 1, etc., such that the SETUP time constraint is NOT violated.
Then, the data get loaded into those AFTER the clock gets changed to 1 in the NEXT clock cycle.
Finally, the inputs may get changed while the clock is still 1, after the clock gets changed to 0, etc., such that the HOLD time constraint is NOT violated.
These changed inputs MAY or MAY NOT correspond to the data to be loaded in the future.
[Similarly for truly NEGATIVE edge-triggered flip-flops]

Since a latch / flip-flop has 2 STABLE states, therefore it is aka a BISTABLE MULTIVIBRATOR.

^ For some reason, the book calls the gated SR, D, JK and T latches as flip-flops, even though their outputs may change the ENTIRE time the clock is at 1, and NOT ONLY during EDGE TRANSITIONS of the clock.

^ SR Latch (aka DIRECT-COUPLED RS Flip-Flop, even though it is technically a LATCH)