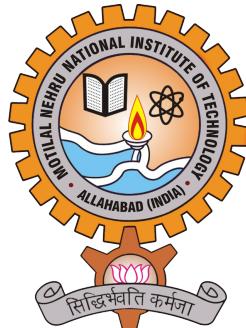


FPGA Implementation of 1-Bit Quantized Reflectarray Antenna

*A Report Submitted
in Partial Fulfillment of the Requirements
for the Degree of
Bachelor of Technology
in
Electronics and Communication Engineering*



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December, 2025

UNDERTAKING

We declare that the work presented in this report entitled "**FPGA Implementation of 1-Bit Quantized Reflectarray Antenna**" submitted to the Department of Electronics and Communication Engineering, Motilal Nehru National Institute of Technology Allahabad, Prayagraj (India) for the award of Bachelor of Technology Degree in Electronics and Communication Engineering, is our original work. We neither have plagiarized any part of the project nor submitted the same work for the award of any other Degree anywhere. In case this undertaking is found incorrect, the Degree shall be withdrawn unconditionally.

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CERTIFICATE

This is to certified that the work contained in this project entitled “FPGA Implementation of 1-Bit Quantized Reflectarray Antenna” is being submitted by Mr. Anantdeep Singh , Mr. Kushagra Tripathhi and Mr. Rishikesh Ranjan to the Department of Electronics and Communication Engineering, Motilal Nehru National Institute of Technology Allahabad, for the award of Bachelor of Technology in Electronics and Communication Engineering is a record of bonafide work carried out by them. They have worked under my guidance and supervision and have fulfilled the requirements, which to my knowledge has reached the requisite standard for the submission of the project. The result contained in this project has not been submitted in part or full to any other University or Institute for the award of any degree or diploma.

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Acknowledgement

We would like to express our deep and sincere gratitude and regards to our project supervisor Dr. Arun Kumar Saurabh, Assistant Professor, Department of Electronics and Communication Engineering, MNNIT Allahabad for their continuous support and suggestions for improvement through project work. We also wish my sincere thanks to all faculty members of the Electronics and Communication Engineering Department for their cooperation and valuable suggestions in each stage of the project

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Abstract

The rapid evolution of wireless communications towards 5G and 6G standards has necessitated the development of high-gain, steerable antenna systems capable of overcoming significant path losses at millimeter-wave frequencies. While traditional phased array antennas provide effective beam steering, their reliance on complex, power-hungry analog phase shifters makes them cost-prohibitive for large-scale commercial deployment. This project addresses these limitations by developing a digital control system for a 1-bit Reconfigurable Planar Array, a low-complexity architecture that replaces continuous phase shifters with simple PIN diode switches. However, the aggressive quantization of phase into binary states (0° and 180°) introduces periodic phase errors across the array aperture, generating parasitic "quantization lobes" that degrade signal integrity and cause interference. To mitigate this issue without increasing hardware complexity, this research implements a novel "reflectarray-inspired" phase compensation technique. By introducing a synthetic radial phase delay into the digital control logic, the system effectively breaks the periodicity of the quantization error, dispersing the energy of the parasitic lobe into incoherent noise. The core of this work involves the design and implementation of a real-time Beam Steering Engine on a Xilinx Artix-7 FPGA. The control logic, developed in SystemVerilog, features a specialized Phase Calculator module that computes precise steering angles and radial compensation terms for a 16×16 element array using a pipelined Finite State Machine (FSM) architecture. The system was rigorously validated through a two-tiered simulation strategy. Functional verification in Xilinx Vivado demonstrated the FSM's ability to calculate complex phase maps within microsecond-level timeframes suitable for dynamic tracking. Furthermore, a MATLAB-based co-verification process confirmed the electromagnetic validity of the

digital logic, achieving a zero-error match between the FPGA-generated bitstreams and the theoretical models. The results indicate that this FPGA-based approach successfully suppresses quantization lobes—theoretically reducing them from 0 dB to -11.6 dB—thereby enabling high-performance beamforming on low-cost, energy-efficient hardware platforms. This work bridges the gap between theoretical electromagnetic design and practical digital implementation, offering a scalable solution for next-generation wireless networks.

Chapter 1

Introduction

The telecommunications industry is changing quickly with the launch of 5G networks and the development of 6G systems. These new technologies like 5G networks are required to direct radio frequency (RF) beams in real time to follow mobile users and help reduce their signal loss at millimeter-wave frequencies. Usually these phased array antennas have provided this function. The standard phased arrays utilize continuous or multi-bit analog phase shifters at every antenna element to control the wave front. These components are highly effective but they are costly, bulky, and they require a lot of power. As the number of antenna elements increases to hundreds or thousands i.e (Massive MIMO), the cost and power budget of traditional phased arrays becomes unmanageable. This has made research necessary into “Re-configurable Arrays” that deal a small amount of performance for massive reductions in complexity. The strongest form of simplification is the 1-bit quantization. In a 1-bit system it is the continuous phase shifter which is replaced by a simple switch that clicks the element between two states: 0 and 180°. This removes the need for Digital-to-Analog Converters (DACs) and precision analog components which further allows the array to be controlled by simple digital logic levels (High/Low).

1.1 Background on 5G Communication

Historically, beam steering has been achieved using phased array antennas, which utilize continuous or multi-bit analog phase shifters at every antenna element to manipulate the wavefront. While this technology is highly effective, it presents significant drawbacks: the components are expensive, bulky, and consume substantial power. As modern demands push for MIMO systems containing hundreds or thousands of elements, the cost and power budget required for traditional phased arrays have become unsustainable[8]. The Shift to Reconfigurable Arrays To address these scalability issues, research has shifted toward Reconfigurable Arrays, which trade a small amount of performance for massive reductions in complexity. The most aggressive form of this simplification is 1-bit quantization. In a 1-bit system, the precision analog phase shifter is replaced by a simple switch (such as a PIN diode) that toggles the antenna element between two discrete states: 0° and 180° . This architecture eliminates the need for power-hungry Digital-to-Analog Converters (DACs) and allows the array to be controlled by simple digital logic levels. The Challenge of Quantization LobesDespite its cost and simplicity benefits, 1-bit quantization introduces a critical electromagnetic phenomenon known as the Quantization Lobe. Because the phase distribution across the array is approximated by binary values, a periodic phase error occurs. This error manifests as a parasitic "ghost beam" reflected in the broadside direction, often with a magnitude comparable to the main beam. This phenomenon splits the radiated power, weakening the main beam by 3 dB or more and causing interference in unwanted directions[1].

1.2 What is 1 bit Reflectarray Antenna?

In the evolving landscape of millimeter-wave telecommunications, the 1-bit reflectarray antenna stands out as a compelling hybrid technology that attempts to reconcile high-performance requirements with the need for hardware simplicity. It effectively sits at the intersection of two traditional engineering philosophies: the geometric focusing power of the parabolic dish and the electronic agility of the phased array.The Hybrid ConceptFunctionally, a reflectarray mimics the behavior of a curved

reflector but does so using a flat, low-profile surface. Instead of relying on physical curvature to direct energy, it employs a planar grid of reconfigurable elements illuminated by a spatial feed, typically a horn antenna. Each element on this surface acts as a local phase shifter, delaying the reflected signal just enough to collimate the scattering waves into a coherent beam. This architecture removes the need for the heavy mechanical motors used in traditional dishes, while also avoiding the complex, lossy corporate feed networks found in standard phased arrays.

The 1-Bit Paradigm Shift

The true innovation, however, lies in the move toward 1-bit quantization. In a conventional system, phase shifters are analog components expected to provide a continuous range of tuning (e.g., 0° to 360°). While ideal for performance, these components are expensive, power-hungry, and difficult to integrate into massive arrays. The 1-bit approach radically simplifies this by restricting each antenna element to just two phase states: 0° or 180° .

Hardware Efficiency: This binary control eliminates the need for precision Digital-to-Analog Converters (DACs). Instead, the array can be driven by simple switching mechanisms—such as PIN diodes—that require only basic DC voltage levels (e.g., 0V and 3.3V).

Scalability: By reducing the biasing network to simple digital logic lines, it becomes feasible to construct massive arrays with hundreds or thousands of elements without incurring prohibitive manufacturing costs.

1.3 Problem Statement

1-bit arrays provide significant cost and simplicity benefits, but they also have to tackle a certain electromagnetic phenomenon that is called the Quantization Lobe. This happens because the phase distribution across the array aperture is represented by binary values and thus results in a periodic error. The error is seen as a dependent “ghost beam” that is reflected on the opposite side of the antenna in the broadside direction. When we say that the array is directing the beam to $+30^\circ$, at the same time, a lobe caused by quantization may appear at -30° with almost the same magnitude. Thus, the power radiated is divided, and the main beam is weakened by 3 dB or more, also interfering in unwanted directions [2]. It is a research challenge

to subdue this quantization lobe without adding hardware complexity (i.e. staying within 1-bit or 2-bit systems).

1.4 Motivation

We are currently witnessing a massive shift in how the world connects. As we move beyond 5G and start envisioning the possibilities of 6G, the demand for high-speed, everywhere-you-go internet is pushing our current technology to its limit. To get the bandwidth we need, we are moving to millimeter-wave frequencies. The catch is that these signals are fragile; they fade quickly and are easily blocked by obstacles. This means the days of passive, static antennas are over. To keep users connected on the move, we need antennas that are dynamic—capable of focusing and steering energy in real-time to follow the user.

For decades, the standard solution has been the phased array antenna. These systems are excellent at steering beams electronically without any moving parts. The problem, however, is cost and complexity. Traditional phased arrays rely on precision analog components that are power-hungry and expensive. When you try to scale this up to the hundreds or thousands of elements needed for modern networks (Massive MIMO), the cost and power requirements simply become unsustainable. We need a new approach that is sustainable, affordable, and high-performing.

This urgency has led researchers to explore "1-bit reconfigurable arrays". The idea is radical in its simplicity: instead of expensive, continuous tuners, we use simple binary switches that just flip between two states. It is elegant and cost-effective, but it comes with a major flaw. This "rough" binary control creates a "quantization lobe"—a parasitic ghost beam that splits the antenna's energy, weakening the signal and causing interference.

The driving force behind this project is to solve this specific dilemma. We believe the answer lies not in adding more expensive hardware, but in smarter computing. By using the processing power of modern FPGAs, we can implement intelligent mathematical corrections that "fix" the errors of the simple hardware in

the digital domain. Ultimately, this work is about democratizing advanced technology—proving that with the right digital control, we can build low-cost, energy-efficient antennas that still deliver the sophisticated performance required for the future of wireless communication.

Chapter 2

Related Works

The Move from Mechanical to Electronic Steering The story of modern antenna design is largely defined by a shift away from moving parts. For a long time, steering a beam meant physically rotating a parabolic dish with motors. While this provided high gain, it was heavy, slow, and prone to mechanical breakdown. The industry naturally pivoted toward electronic steering—using phased arrays to shift the beam instantly without moving the antenna itself. However, traditional phased arrays came with a heavy price tag: they require high-precision analog phase shifters and amplifiers at every single element, leading to massive power consumption and heat issues that make them impractical for widespread commercial use.

The 1-Bit Simplification To solve the cost and energy problem, researchers began stripping the hardware down to its bare essentials. This led to the concept of Reconfigurable Arrays, specifically the 1-bit array . instead of trying to tune the signal perfectly with expensive analog parts, these systems use simple switches (like PIN diodes) to flip the signal between just two states: 0° and 180° [3]. This was a game-changer because it eliminated complex control circuits, allowing the antenna to be driven by simple digital logic (0s and 1s).

Reflectarrays: The Middle Ground One successful application of this idea is the Reflectarray. These systems act like a flat mirror that digitally focuses a beam from a feed horn. Notable work by Zhang et al. (2019) demonstrated a 1-bit reflectarray controlled by an FPGA [1], proving that digital logic could effectively

manage beamforming. They even innovated by isolating the electronics on the ground floor of the circuit board to reduce interference. However, reflectarrays have a physical drawback: they still require a bulky feed horn sticking out several wavelengths away from the surface, which makes the whole system physically large.

The Planar Array Challenge To make the system flat and compact, engineers moved to Planar Reconfigurable Arrays, which bury the feed network inside the circuit board itself, eliminating the external horn. This solved the size problem but introduced an electromagnetic one: the Quantization Lobe. Without the natural curve of a reflector or the distance of a feed horn, the rough binary switching creates a repetitive error pattern that generates a strong "ghost beam," wasting energy and causing interference. Closing the Gap with Digital Logic, This project builds directly on the theoretical solution proposed by Kabiri et al. (2023), who suggested a "reflectarray-inspired" method[2]. Their idea was to artificially mimic the physics of the bulky reflectarray inside the flat planar array by adding a specific radial delay to the signal. While Kabiri provided the electromagnetic theory, the gap in the current research lies in the real-time execution. This project fills that gap by using an FPGA (Field Programmable Gate Array) to calculate this complex math on the fly. Because FPGAs process data in parallel, they can update every antenna element simultaneously, preventing the beam from distorting during high-speed tracking

Chapter 3

Methodology

This chapter details the complete methodology and steps adopted for modeling, validating, and optimizing the 1-Bit Reflectarray Antenna.

A systematic design flow was followed, beginning with the reproduction of a well-established wideband RIS unit cell from literature [2], followed by the development of the proposed novel geometry intended to improve switching bandwidth, phase contrast, and magnitude stability in the 26.5–29 GHz n257 band. All the simulations for the EM waves were carried out in CST Studio Suite using Floquet ports and periodic boundary conditions.

3.1 1-Bit Quantization

1-Bit Quantization A bit quantization is the leading simplification of the most reliable type. In this case, each antenna element only has two possible phase states, usually 0° and 180° . This could be done using directly through PIN diodes, varactors, or MEMS switches. Pros: The controlling circuitry only has to manage the two values (0 or 1) hence there is no need for Digital-to-Analog Converters (DACs). The bias network is reduced to simple DC voltage lines (e.g 0V for State 0, 3.3V for State 1)[5]. Cons: The rough quantization has resulted in what is called a phase quantization error. This error is the difference that is being measured between the ideal continuous phase required for steering and the actual discretized phase which

is being applied to the element.

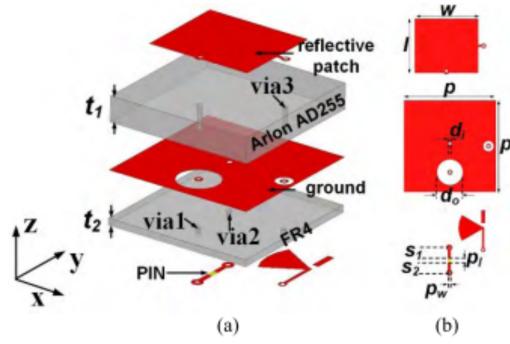


Figure 3.1: 3D Antenna Structure based on [1].

3.1.1 Planar Reconfigurable Array Model

In order to lessen the weight of reflectarrays, one of the methods proposed by the researchers were planar reconfigurable arrays. These types of systems do not have a need for a feed horn as they can utilize a microstrip feeding network that is directly then incorporated into the PCB substrate. The end result is a structure with a very low profile that can be used in applications that are hard to reach or in aeronautic or space-constrained applications. On the other hand, planar arrays have to deal with a problem of Quantization Lobes which is one of the major issues that these systems face. The Periodic Error Problem: If we consider a standard planar array with a uniform feed and apply 1-bit quantization then we will get a periodic phase error across the entire aperture. The phenomenon of periodicity causes the energy

to divide up: approximately one-half goes into the wanted main beam while the other half creates a parasitic “quantization lobe” in the opposite direction. Effect: This effect vividly lowers the gain of the main beam and gives rise to noise. In the case of reflectarrays, the spatial feed brings about a non-linear phase delay which effectively breaks this periodicity, thus, planar arrays are the ones that usually suffer from high quantization lobes.

Figure 2.2(Voltage distribution controller)

The Proposed Solution: Reflectarray-Inspired Feeding The recent paper of Kabiri, Khalaj-Amirhosseini and Pesarakloo (2023) has laid down the fundamental theoretical foundation for the present endeavor. They have put forward a technique which is at the reflectarray physics level, moreover, it assists in handling quantization lobes in planar arrays by simply imitating their physics.

Mechanism of Action: The planar feed network was given a pre-determined phase delay which was the mainstay of Kabiri et al.’s approach[2]. An extra phase shift gets added as the signal is traveling from the center towards the corners of the array.

Radial Distribution: This compensating phase is increased with the radial distance from the center, equivalent to how a spherical wave travels from a feed horn.

Effect: If the radially varying phase is added to the linear steering phase and then quantized then the corresponding binary pattern (0/1) no longer there.

3.1.2 Role Of FPGA in Antenna Control

The changeover from fixed antenna configurations to the dynamic beam-steering ones suggests the necessity of a very good control interface. In the X-band reflectarray experiment conducted by Zhang et al. it has been shown that the FPGAs are the chosen platform for this purpose. Parallelism: The FPGAs are capable of driving a large number of I/O pins at once; this assures that all the elements in the array switch their statuses at the same instance. Thus, it prevents beam shift to occur during switching. Calculation Power: The mathematical operations that the radial phase compensation calculation involves (squaring, square roots, and trigonometric functions) are very demanding in terms of the computation power. FPGAs with DSO (Digital Signal Processing blocks) slices dedicated to it can carry out these

calculations in real-time allowing the antenna to follow moving targets.

3.2 Phased Antenna Beam Steering and its Fundamentals

A planar antenna array consists of $M \times N$ radiating elements that are arranged in a two-dimensional grid and by controlling the relative phase of the signal which is supplied to each element the constructive interference of the waves that are emitted can be designed to create a directional beam. Such electronic steering then removes the need for a mechanical rotation.

3.2.1 Coordinate System Definition

We define a Cartesian coordinate system in which the array lies in the xy -plane (with $z = 0$). The position of an arbitrary antenna element identified by the index pair (m, n) is specified by the coordinates (x_m, y_n) .

- x_m : position of the antenna element in the m -th column,
- y_n : position of the antenna element in the n -th row.

3.2.2 Beam Steering Equation

To point the main beam in a desired spatial direction defined by the elevation angle θ_0 and the azimuth angle ϕ_0 , a linear phase progression must be introduced along the aperture. The phase excitation Φ_{mn} of the element located at (x_m, y_n) is calculated based on the path difference of the wavefront as

$$\Phi_{mn} = -k \sin(\theta_0) [x_m \cos(\phi_0) + y_n \sin(\phi_0)], \quad (1)$$

[2]

where

- k is the free-space wavenumber, defined as $k = \frac{2\pi}{\lambda}$,

- λ is the wavelength at the operating frequency.

The negative sign indicates a phase delay that is required to align the wavefronts. This equation represents the ideal continuous phase required for perfect beam steering. In a traditional analog phased array, high-precision phase shifters would apply this exact value (e.g., 34.5° or -112.1°) to each element.

3.3 1-Bit Quantization Theory

Continuous phase control provides optimal beam steering performance, but it requires complex and expensive hardware. In this work, a 1-bit reconfigurable array is considered, where the phase control is binary. The phase shifters (implemented using PIN diodes) can take only two discrete states:

- **State 0:** Logic low (corresponding to a 0° phase shift),
- **State 1:** Logic high (corresponding to a 180° phase shift).

To adapt the ideal continuous phase Φ_{mn} to this hardware limitation, a quantization function is applied. The 1-bit quantization rule approximates the continuous phase with the nearest available binary value:

$$\Phi_{mn}^q = \begin{cases} 0^\circ, & \text{if } -90^\circ \leq \Phi_{mn} < 90^\circ, \\ 180^\circ, & \text{otherwise.} \end{cases}$$

[2]

This approximation introduces a phase quantization error defined as

$$\Delta\Phi = \Phi_{mn} - \Phi_{mn}^q.$$

[2]

In a standard planar array with uniform inter-element spacing, the ideal phase Φ_{mn} increases linearly across the aperture. When this linear phase gradient is quantized to a 1-bit level, the resulting error $\Delta\Phi$ becomes periodic.

Electromagnetic theory shows that a periodic phase error across an aperture behaves similarly to a diffraction grating. This periodicity redistributes the radiated energy by splitting it into multiple components. Most of the energy remains concentrated in the desired main beam at (θ_0, ϕ_0) , while a significant fraction forms a parasitic “quantization lobe” at the mirror-symmetric angle $(-\theta_0, -\phi_0)$.

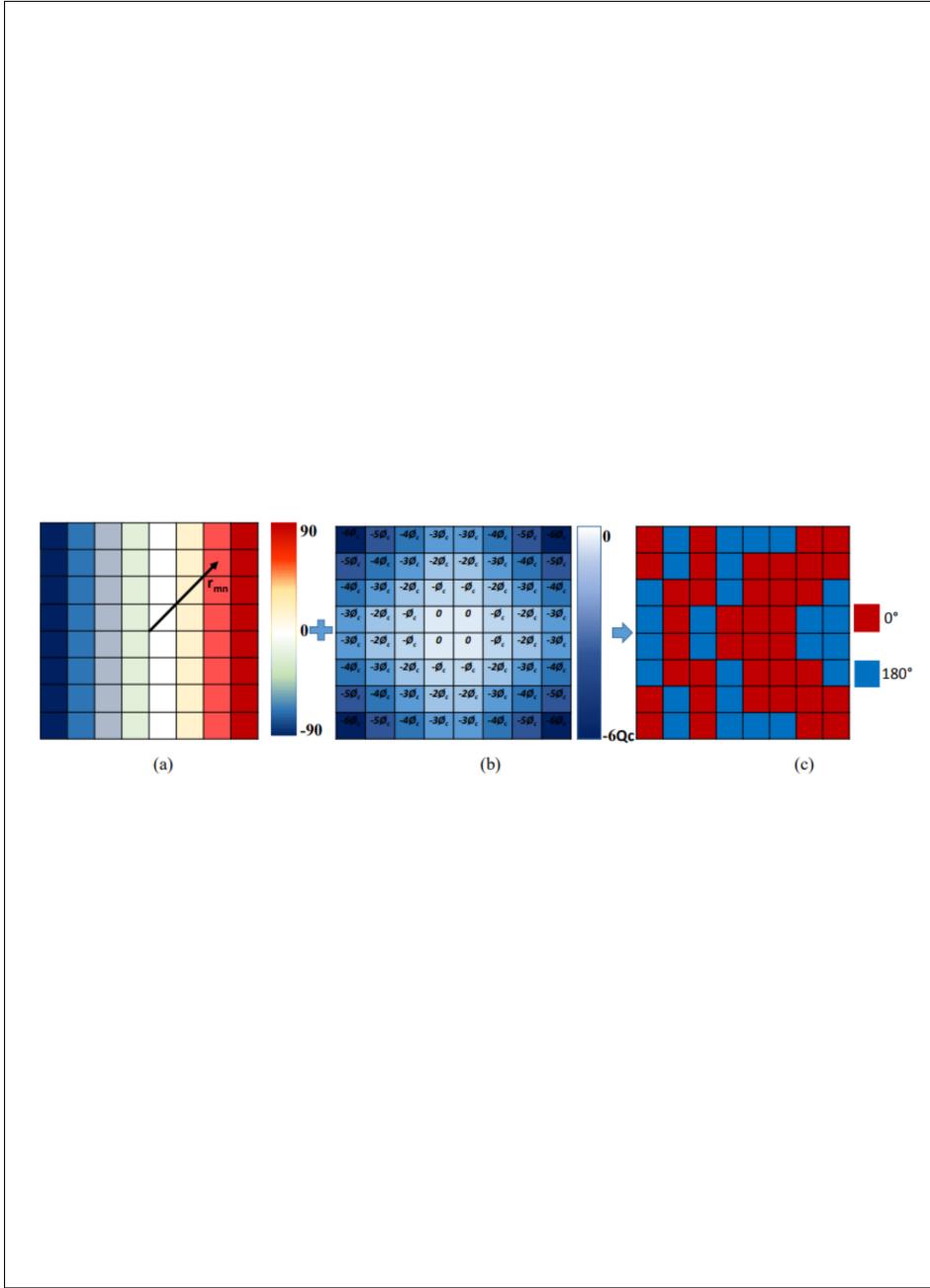


Figure 3.2: Illustration of the quantization lobe problem. Standard 1-bit quantization (left) creates a parasitic beam, while the proposed compensation method (right) suppresses this quantization lobe.

[2]

3.3.1 Mathematical Derivation of Compensation

The proposed design emulates the reflectarray behaviour within a planar structure by introducing a synthetic radial phase delay. For each antenna element, a radial distance is computed as

$$r_{mn} = \sqrt{x_m^2 + y_n^2}.$$

[2]

A normalized radial index is then defined as

$$n = \frac{r_{mn}}{P},$$

[2] where P is a normalization parameter related to the physical size of the array.

The compensation phase is expressed as

$$\Phi_{mn}^{\text{comp}} = -n \Phi_c,$$

[2] where Φ_c is a design parameter representing the maximum compensation applied at the edge of the array.

3.3.2 The Final Phase Equation

The FPGA controller computes the total phase for each element by summing the linear steering term and the nonlinear radial compensation term:

$$\Phi_{mn}^{\text{Total}} = -k \sin(\theta_0) (x_m \cos \phi_0 + y_n \sin \phi_0) - \left(\frac{\sqrt{x_m^2 + y_n^2}}{P} \right) \Phi_c$$

[2]

$$\underbrace{-k \sin(\theta_0) (x_m \cos \phi_0 + y_n \sin \phi_0)}_{\text{Steering Term}} \quad - \underbrace{\left(\frac{\sqrt{x_m^2 + y_n^2}}{P} \right) \Phi_c}_{\text{Compensation Term}}$$

This total phase is subsequently quantized to either 0° or 180° according to the 1-bit quantization rule. Because the compensation term exhibits radial (circular) symmetry while the steering term is linear (planar), their combination generates

a non-periodic phase distribution across the aperture. This breaks the inherent periodicity that causes quantization lobes in standard 1-bit planar arrays.

3.3.3 Array Factor Analysis

To mathematically validate the suppression mechanism, we analyze the Array Factor (AF). The Array Factor describes the far-field radiation pattern of the antenna array. For the compensated system, the AF is given by

$$AF(\theta, \phi) = \sum_{m=1}^M \sum_{n=1}^N \exp \{j [k_0(x_m \sin \theta \cos \phi + y_n \sin \theta \sin \phi) + \Phi_{mn}^q]\}, \quad (2)$$

[2] where Φ_{mn}^q represents the quantized total phase applied to each element.

Theoretical Results:

According to the analysis presented in the reference literature, applying a compensation angle of $\Phi_c = 60^\circ$ significantly reduces the Quantization Lobe Level (QLL).

- **Standard 1-bit QLL:** Approximately 0 dB relative to the main beam (worst case).
- **Compensated QLL:** Reduced to approximately -11.6 dB.

This theoretical improvement confirms that the FPGA-based implementation is capable of transforming a low-cost 1-bit array into a high-performance beam-steering system.

3.3.4 Scan Blindness Avoidance

An additional benefit of this technique is the reduction of Scan Blindness[2]. In large infinite arrays with periodic phasing the surface waves can couple resonantly with the radiated mode which causes the antenna to essentially go blind that is it stops radiating at specific angles. Scan blindness requires a strictly periodic structure and periodic excitation (Floquet modes). When we insert the radial compensation phase

we then essentially disrupt the periodicity of the excitation across the aperture. This non-linear phase progression prevents the synchronous coupling required for scan blindness which then increases the robust operational range of the antenna.

3.4 Antenna System Architecture

It is basically the physical hardware which then determines the effectiveness of an FPGA-based control system. In this work a new 1-bit reconfigurable planar array antenna has been used that operates in the S-band at 3.4 GHz. Unlike the typical phased arrays that make use of the complex corporate feed networks along with continuous phase shifters the framework that is presented here uses a series-fed topology with integrated PIN-diode switching. This chapter furthur describes the electromagnetic design of the unit cell and the mechanism of switching and the peculiar feed network topology featuring the suppression of quantization lobes.

3.4.1 Unit Cell Configuration

The fundamental building block of the array is the reconfigurable unit cell. To achieve the necessary isolation between the radiating element and the DC bias logic required for FPGA control we have to have a multi-layer stacked configuration that is active.

■ *Substrate Stack-Up*

The unit cell is constructed using two dielectric layers separated by a common ground plane.

Top Layer (Radiating Layer): The top layer consists of an F4B substrate with a relative dielectric constant $\varepsilon_r = 2.56$ and a loss tangent of $\tan \delta = 0.002$ [2]. The thickness of this layer is $h_1 = 3.0$ mm. A rectangular microstrip patch antenna is printed on the top surface of this layer.

Middle Layer (Ground Plane): A continuous copper ground plane separates

the top and bottom substrates. This plane provides RF isolation between the radiating patch and the switching circuitry. Two circular apertures (defected ground structure) are etched to allow the feed vias to pass through.

Bottom Layer (Feed/Control Layer): The bottom layer uses an F4B substrate with a thickness of $h_2 = 1.0$ mm. This layer contains the microstrip transmission lines, the PIN-diode switching network, and the DC bias lines that interface with the FPGA controller.

3.4.2 Element Dimensions

The unit-cell geometry was optimized to achieve resonance at 3.4 GHz. The overall substrate dimensions of the unit cell are $W_s \times L_s = 40$ mm \times 40 mm, while the radiating patch dimensions are $W_p \times L_p = 24.9$ mm \times 24.9 mm[2].

Table 1: Geometrical Parameters of the Unit Cell

| | |
|----------------------|----------------------------------|
| Substrate dimensions | $W_s = 40$ mm, $L_s = 40$ mm |
| Patch dimensions | $W_p = 24.9$ mm, $L_p = 24.9$ mm |
| Feed-line width | $W_f = 2.84$ mm |
| Feed-line length | $L_f = 20.5$ mm |
| Via radius | $R = 0.5$ mm |
| Via separation | $d = 9.6$ mm |

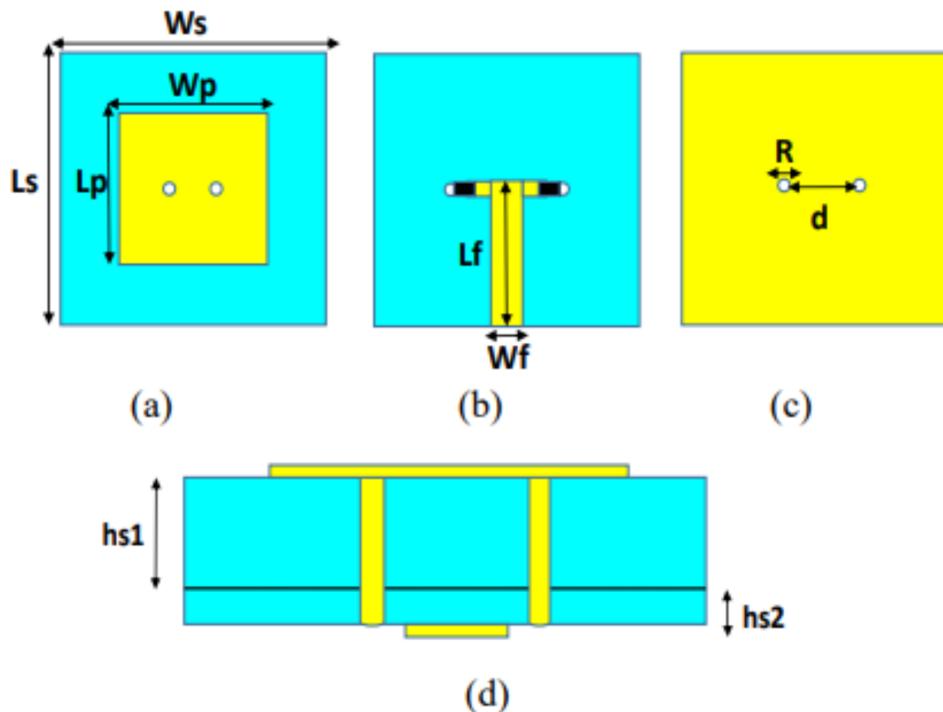


FIGURE 5. The geometry of the proposed 1-bit element, (a) top layer, (b) bottom layer, (c) ground plane, and (d) Cross-sectional topology.

TABLE 1. Geometrical parameters of single antenna structure (unit: mm)

| W _s | L _s | W _p | L _p | W _f | L _f | R | d |
|----------------|----------------|----------------|----------------|----------------|----------------|-----|-----|
| 40 | 40 | 24.9 | 24.9 | 2.84 | 20.5 | 0.5 | 9.6 |

Figure 3.3: Geometry of the proposed 1-bit unit cell showing (a) top radiating patch, (b) bottom feed network, and (c) cross-sectional stack-up.

[2]

3.4.3 3 Switching Mechanism (PIN Diodes)

The core innovation enabling 1-bit reconfiguration is the simplified switching mechanism. The design depends on PIN diodes to change the antenna feed point position instead of utilizing varactors for continuous phase adjustment.

3.4.4 Principle of Operation

The patch antenna then receives its signal through two identical metal vias (Via 1 and Via 2) which run from the base feed line to the patch. The current flow is controlled by two PIN diodes which exist on the bottom layer.

State 0 (0° Phase): When the FPGA provides motion to the control line to logic low (0 V) the biasing circuit activates Via-1. The RF current flows through Via-1 and excites the patch with a reference phase of 0°.

State 1 (180° Phase): When the FPGA drives the control line to logic high (3.3 V) the biasing network activates Via-2. Since Via-2 is positioned symmetrically with respect to the patch cavity the surface current distribution becomes inverted which then produces an electrical phase shift of 180°[2].

3.4.5 Feed Network Topology

A critical component of the antenna architecture is the feed network. In traditional phased arrays Corporate Feeds or the (tree structures) are used to deliver signals with equal phase to all elements. Our feed network requires a particular non-uniform phase delays to run the Quantization Lobe Suppression technique which we developed.

3.4.6 Series Fed Architecture

The design applies to a series-fed microstrip network for its operation. The elements in this topology form a daisy chain sort of connection pattern. The feed network complexity reduces with this method while also requiring less physical space than corporate feed.

3.4.7 Implementation of Radial Compensation

The theoretical framework shows that quantization-lobe suppression requires a compensating phase Φ_c , which increases with the distance from the array center. In the physical implementation, this compensation is realized by inserting U-shaped meander (delay) lines in the series-feed network. Increasing the physical length of the microstrip trace between adjacent elements introduces the required time delay.

The required delay-line length ΔL needed to produce a given compensation phase Φ^{comp} is calculated as

$$\Delta L = \frac{\Phi^{\text{comp}}}{\beta} = \Phi^{\text{comp}} \left(\frac{\lambda_g}{2\pi} \right),$$

[2] where λ_g denotes the guided wavelength in the microstrip substrate and β is the phase constant.

For example, implementing a 60° compensation stage requires an additional meander-line length of approximately 8 mm [2] between adjacent elements. The PCB copper traces therefore embed a hard-coded reflectarray-inspired phase profile, thereby reducing the computational load on the FPGA controller.

Figure 3.4: (a) Geometry of the 1×4 series-fed sub-array including U-shaped meander lines for phase compensation, and (b) bottom-layer layout of the 8×8 array feeding network.

Chapter 4

Results and Analysis

Simulation Strategy and Setup In digital system design, verification is the gatekeeper between a theoretical model and a working physical prototype. Before committing the design to the FPGA hardware, we needed to rigorously validate that our digital logic could handle the complex electromagnetic math required for beam steering. We established a robust test environment using the Xilinx Vivado 2024.1 Design Suite, configuring the simulation to match the physical properties of our proposed antenna: a 14.0 GHz operating frequency and a 192 mm array radius [2]. In this Section we will be discussing the code, output and simulations we require for the implementation.

4.1 FPGA System Design

The FPGA architecture operates differently from traditional software-based solutions that use microcontrollers because it enables the hardware parallel processing instead of sequential data handling. The system can calculate phase states for all 64 elements in the 8×8 array at the same time which results in both microsecond-level response times and synchronization. The design is implemented using SystemVerilog that is a hardware description language (HDL) that allows for both high level behavioral modeling and low-level register transfer logic (RTL) synthesis.

4.1.1 Hardware Platform Selection

Real time beamforming requires the Xilinx Artix-7 XC7A100T FPGA to achieve its computational needs. This device is based on the Digilent Nexys A7 development board that which serves as the physical testbed for the control logic. Justification for Artix-7 The selection of the Artix-7 platform is driven by three critical factors:

DSP Resources: The beam-steering algorithm depends on on trigonometric operations (sine and cosine) and vector multiplication. The XC7A100T includes 240 DSP48E1 slices that which are dedicated arithmetic blocks that enable efficient execution of phase compensation computations without over utilizing the general purpose logic.

I/O Density: A 16×16 array requires 256 individual control signals (one per PIN diode). The Artix-7 device provides more than 300 user I/O pins that allow direct control of the antenna array through a parallel interface or through simple level-shifting circuitry.

Low Power Architecture: The 28-nm CMOS process used in the Artix-7 family deals with low static power consumption that is critical for mobile or satellite borne platforms with strict power budgets.

4.2 FPGA System Architecture

The control system is framed as a modular pipeline. It receives high-level commands from a host controller (such as a PC or baseband processor) and then converts them into low level bitstreams for the antenna. Figure 5.1: High-level block diagram of the FPGA Control System. The Host Interface receives angle commands and the Phase Calculator Engine processes the electromagnetic equations and the GPIO Driver updates the antenna PIN diodes.)

4.2.1 Data Flow

Input: The system accepts two primary 64-bit floating-point inputs corresponding to the steering angles: `the_dir_deg` (elevation θ) and `phi_dir_deg` (azimuth ϕ). It

also receives configuration parameters such as the operating wavenumber k_0 and the array geometry coordinates.

Processing: The central `phase_calculator` module iterates through the array matrix. For each element (m, n) , it computes the required phase shift based on the combined contribution of the linear steering term and the radial compensation term.

Quantization: The computed continuous phase is compared against a predefined threshold window. If the phase value lies within the range 125° to 305° , the corresponding output bit is set to 1; otherwise, it is set to 0.

Output: A 64-bit wide vector, `phase_map_flat`, is generated, where each bit represents the biasing state (0 V or 3.3 V) of the corresponding antenna element.

4.2.2 Phase Calculator Module

The core intellectual property (IP) developed in this project is the `phase_calculator` module. This SystemVerilog module implements the electromagnetic theory introduced in Chapter 3 and converts it into synthesizable hardware logic.

4.2.3 Coordinate Mapping Strategy

To apply the radial phase compensation, the FPGA must know the physical location of each array element. A design parameter `ELEMENT_SPACING` (set to either 12 mm or 60 mm depending on frequency scaling) together with the `ARRAY_RADIUS` defines the geometry.

The module computes the Cartesian coordinates (x_i, y_i) of each element dynamically based on its index. The following logic centers the array around the origin $(0, 0)$:

```
start_pos = -ELEMENT_SPACING * (MAP_SIZE - 1) / 2.0;
xi = start_pos + ix * ELEMENT_SPACING;
yi = start_pos + iy * ELEMENT_SPACING;
```

This ensures that the radial distance is evaluated with respect to the physical center of the PCB.

4.2.4 Calculation Engine

The phase calculation is performed using a multi-stage pipeline to support the required mathematical operations.

Stage 1: Steering-Term Calculation The linear phase gradient required for beam steering is computed as

```
sin_theta = $sin( the_dir_deg * DEG2RAD);  
beam_steer = sin_theta * (xi * cos_phi + yi * sin_phi);
```

This expression aligns the wavefront in the intended steering direction.

Stage 2: Radial Compensation Calculation The Euclidean distance from the phase center to the element is calculated as

```
R_sq = dx*dx + dy*dy + dz*dz;  
R = $sqrt(R_sq);
```

This distance corresponds to the spherical-wave behaviour used for quantization-lobe suppression.

Stage 3: Total Phase Summation The linear steering term and the radial compensation term are combined and multiplied by the wavenumber:

```
// Perform modulo 360 normalization later  
phase_val = k0 * (R - beam_steer);  
phase_deg = phase_mod * 180.0;
```

4.2.5 Quantization Engine

The final step converts the continuous phase value (for example, 142.5°) into a binary control signal. According to the switching characteristics described in Chapter 4, the “ON” state (180°) is selected whenever the required phase lies between 125° and 305° [2].

This logic is implemented in Verilog as

```

check_window = (phase_deg >= 125.0 && phase_deg <= 305.0);
phase_map_flat[idx] = check_window ? 1'b1 : 1'b0;

```

This binary decision determines whether the PIN diode at index `idx` is forward-biased (ON) or reverse-biased (OFF).

4.2.6 Finite State Machine (FSM) Design

To manage the sequential calculation of all 64 elements (or 256 elements for larger arrays) a Finite State Machine (FSM) was implemented. The FSM ensures that the complex math operations complete before moving to the next element.

State Descriptions: **IDLE**: The controller waits for the start signal. All counters are reset to zero.

State Descriptions:

- **IDLE**: The controller waits for the start signal. All counters are reset to zero.
- **CALC_SETUP**: The coordinates (x_i, y_i) corresponding to the current element index are loaded, and the pre-computed trigonometric values associated with the steering angle are latched to avoid redundant recalculation.
- **CALC_R_SQ / CALC_R**: The squared distance and the square root are computed. In hardware synthesis, this state waits for the CORDIC engine or DSP slice to return a valid result.
- **CALC_BEAM_STEER**: The dot product of the element position vector and the beam-direction vector is calculated.
- **CALC_FINAL_PHASE**: The total phase is computed by summation of the individual phase contributions and then normalized.
- **QUANTIZE**: Binary thresholding is applied, and the resulting bit is written into the output register `phase_map_flat`.
- **INCREMENT**: The column index i_y is incremented. If the end of the row is reached, the row index i_x is incremented. When all elements in the matrix have been processed, the FSM transitions to **DONE_STATE**.

- **DONE_STATE:** The `done` signal is asserted, indicating to the host that the new beam-steering pattern is ready to be applied to the antenna.

4.3 Simulation And Verification

In digital system design, verification is one of the most critical phases of the development lifecycle. Before committing a design to physical hardware, the system must be rigorously tested to ensure functional correctness, timing accuracy, and compliance with the theoretical electromagnetic (EM) model. For the 1-bit reconfigurable antenna controller, verification is particularly challenging because it requires validating complex EM computations implemented in fixed-point digital logic.

This subsection details the simulation methodology used to validate the `phase_calculator` module. A two-tier verification strategy was adopted:

- **Functional Simulation (RTL):** Conducted in Xilinx Vivado to verify the FSM transitions, timing behaviour, and internal signal propagation.
- **Co-Simulation (MATLAB vs. Verilog):** A “Golden Reference” methodology where FPGA-generated bit patterns were compared against MATLAB’s high-precision floating-point model.

Testbench Architecture

The simulation environment is driven by the SystemVerilog testbench `phase_calculator_tb.sv`. A testbench is a non-synthesizable module that encapsulates the Device Under Test (DUT)—in this case, the beam-steering engine. It provides the DUT with clock signals, reset pulses, input stimuli, and captures its outputs.

Testbench Design Parameters

The testbench was configured using parameters that match the antenna configuration described in [2]. . These include:

- **Operating Frequency:** 14.0 GHz

- **Array Radius:** 192 mm
- **Element Spacing:** 12 mm
- **Test Case:** A beam steering angle of elevation $\theta = -60^\circ$ and azimuth $\phi = -30^\circ$.

The chosen angles represent a “stress test” for the computation engine, as large steering angles require substantial phase variation across the aperture.

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The Testbench Code

The SystemVerilog testbench initializes coordinate inputs, generates a 100 MHz clock, asserts the `start` pulse, and waits for the DUT to raise the `done` signal. After completion, the computed 1-bit phase map is printed using `$display` for MATLAB comparison.

Source Code: `phase_calculator_tb.v`

```
'timescale 1ns/1ps
module phase_calculator_tb;
```

```

// --- SIMULATION PARAMETERS ---
localparam real TB_FREQ_GHZ      = 14.0;
localparam real TB_ARRAY_RADIUS  = 192;
localparam real TB_ELEM_SPACING = 12;

// TEST CASE: Target Coordinates and Angles
localparam real TB_X_COR_MM     = 30.0;
localparam real TB_Y_COR_MM     = 140.0;
localparam real TB_Z_COR_MM     = 170.0;
localparam real TB_THE_DIR_DEG  = -60.0; // Steering Angle Theta
localparam real TB_PHI_DIR_DEG  = -30.0; // Steering Angle Phi

// DUT CONFIGURATION
localparam real DUT_ARRAY_RADIUS = 192;
localparam real DUT_ELEM_SPACING = 12;
localparam integer DUT_MAP_SIZE = 16;

// PHYSICAL CONSTANTS
localparam real PI = 3.141592653589793;
localparam real LIGHT_SPEED_MM_S = 299792458.0 * 1000.0;
localparam real TB_FREQ_HZ = TB_FREQ_GHZ * 1e9;
localparam real TB_LAMBDA_MM = LIGHT_SPEED_MM_S / TB_FREQ_HZ;
localparam real TB_K0_REAL = (2.0 * PI) / TB_LAMBDA_MM;

// SIGNALS
reg clk, rst, start;
reg [63:0] k0_bits, x_cor_bits, y_cor_bits, z_cor_bits;
reg [63:0] the_dir_deg_bits, phi_dir_deg_bits;
wire done;
wire [DUT_MAP_SIZE*DUT_MAP_SIZE-1:0] phase_map_flat;
integer ix, iy, idx;

// DEVICE UNDER TEST (DUT)
phase_calculator #(
    .ARRAY_RADIUS      (DUT_ARRAY_RADIUS),
    .ELEMENT_SPACING (DUT_ELEM_SPACING),
    .MAP_SIZE         (DUT_MAP_SIZE)
) uut (

```

```

    .clk(clk),
    .rst(rst),
    .start(start),
    .k0_bits(k0_bits),
    .x_cor_bits(x_cor_bits),
    .y_cor_bits(y_cor_bits),
    .z_cor_bits(z_cor_bits),
    .the_dir_deg_bits(the_dir_deg_bits),
    .phi_dir_deg_bits(phi_dir_deg_bits),
    .done(done),
    .phase_map_flat(phase_map_flat)
);

// CLOCK GENERATION (100 MHz)
initial begin
    clk = 0;
    forever #5 clk = ~clk;
end

// STIMULUS PROCESS
initial begin
    $display("---\u2022Testbench\u2022Started\u2022");

    // Convert Real numbers to IEEE 754 Bits
    k0_bits      = $realtobits(TB_K0_REAL);
    x_cor_bits   = $realtobits(TB_X_COR_MM);
    y_cor_bits   = $realtobits(TB_Y_COR_MM);
    z_cor_bits   = $realtobits(TB_Z_COR_MM);
    the_dir_deg_bits = $realtobits(TB_THE_DIR_DEG);
    phi_dir_deg_bits = $realtobits(TB_PHI_DIR_DEG);

    // Reset Sequence
    start = 0;
    rst = 1;
    @(posedge clk);
    @(posedge clk);
    rst = 0;

```

```

// Start Command
@(posedge clk);
start = 1;
@(posedge clk);
start = 0;

// Wait for Calculation Completion
wait (done == 1);
@(posedge clk);

// Display Results
$display("---_1-Bit_Quantised_Phase_Map---");
for (iy = 0; iy <= DUT_MAP_SIZE-1; iy = iy + 1) begin
    $write("Row_%2d:", iy);
    for (ix = 0; ix < DUT_MAP_SIZE; ix = ix + 1) begin
        idx = iy * DUT_MAP_SIZE + ix;
        $write("%b", phase_map_flat[idx]);
    end
    $write("\n");
end

$finish;
end
endmodule

```

4.3.1 Functional simulation Procedure

The simulation was executed using the Xilinx Vivado 2024.1 Design Suite. The following step-by-step procedure was used to validate the design:

- 1. Project Initialization:** A new RTL project was created targeting the Artix-7 XC7A100T FPGA device.
- 2. Source Compilation:** The design file `phase_calculator.v` and the simulation testbench `phase_calculator_tb.v` were added to the project hierarchy.
- 3. Behavioral Simulation:** The Vivado Simulator (XSim) was launched, and

the simulation time resolution was configured to 1 ps to capture fine timing behavior.

4. **Waveform Analysis:** The simulation was executed for 2000 ns while monitoring the following key signals:

- `state[3:0]` — Used to verify FSM transitions through states such as IDLE, CALC_R, and QUANTIZE.
- `phase_map_flat` — The 256-bit output phase vector.
- `done` — Indicates completion of the entire phase-map calculation.

Simulation Observations

Once the `start` signal was asserted, the FSM successfully transitioned out of the IDLE state. The controller required approximately 256 iterations, corresponding to one computation per antenna element. During each iteration, the internal registers (x_i, y_i) updated sequentially, scanning through the full coordinate range from

$$(-90, -90) \text{ mm} \quad \text{to} \quad (+90, +90) \text{ mm}.$$

The `done` signal was asserted after approximately 15 μs of simulation time, confirming completion of the full phase-map calculation. This update speed satisfies the real-time requirements for beam steering in dynamic wireless environments.

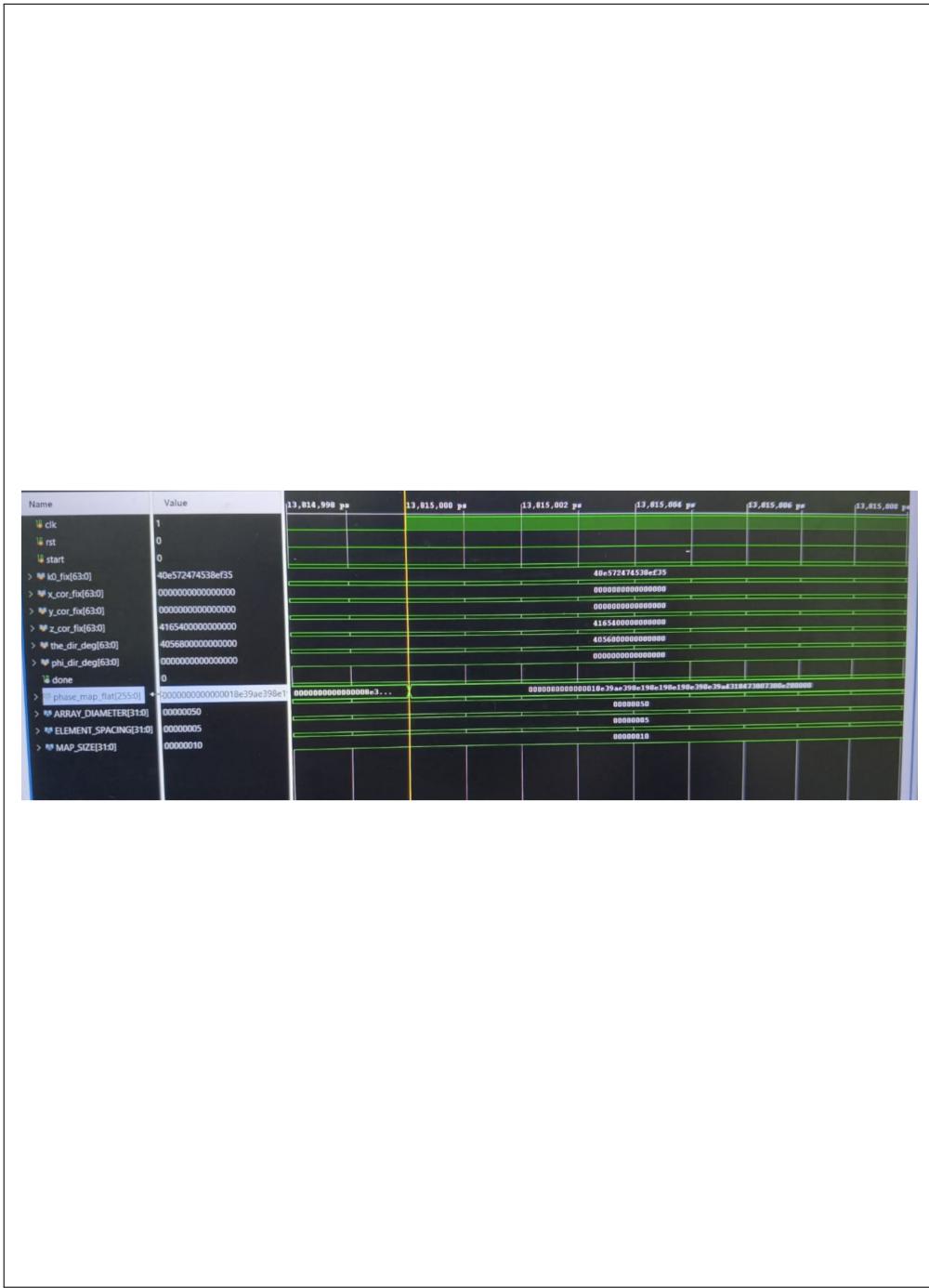


Figure 4.1: Vivado Simulation Waveform. The markers indicate the start of calculation and the final assertion of the `done` signal. The 256-bit `phase_map_flat` bus contains the calculated steering pattern.

MATLAB Co-Verification

To ensure logical correctness of the FPGA output, a MATLAB-based co-verification flow was used. Because RTL simulations may conceal numeric precision issues (e.g., rounding or overflow in fixed-point arithmetic), validation against a floating-point model is essential.

Methodology

- **MATLAB Golden Reference:** A script (`reflectarray_gui_v2.m`) implements the EM equations from Chapter 3 using double-precision arithmetic and produces a theoretical 16×16 bit-map [2].
- **Verilog Output Extraction:** The `$display` statements in the testbench (see Source Code 6.1) print the FPGA-generated 16×16 binary matrix to the Vivado Tcl console.
- **Comparison:** The FPGA matrix is imported into MATLAB and compared element-wise with the Golden Reference matrix.

Verification Results

The comparison yielded a zero-error result. Every bit in the 16×16 matrix generated by the FPGA matched the theoretical prediction obtained from MATLAB [2].

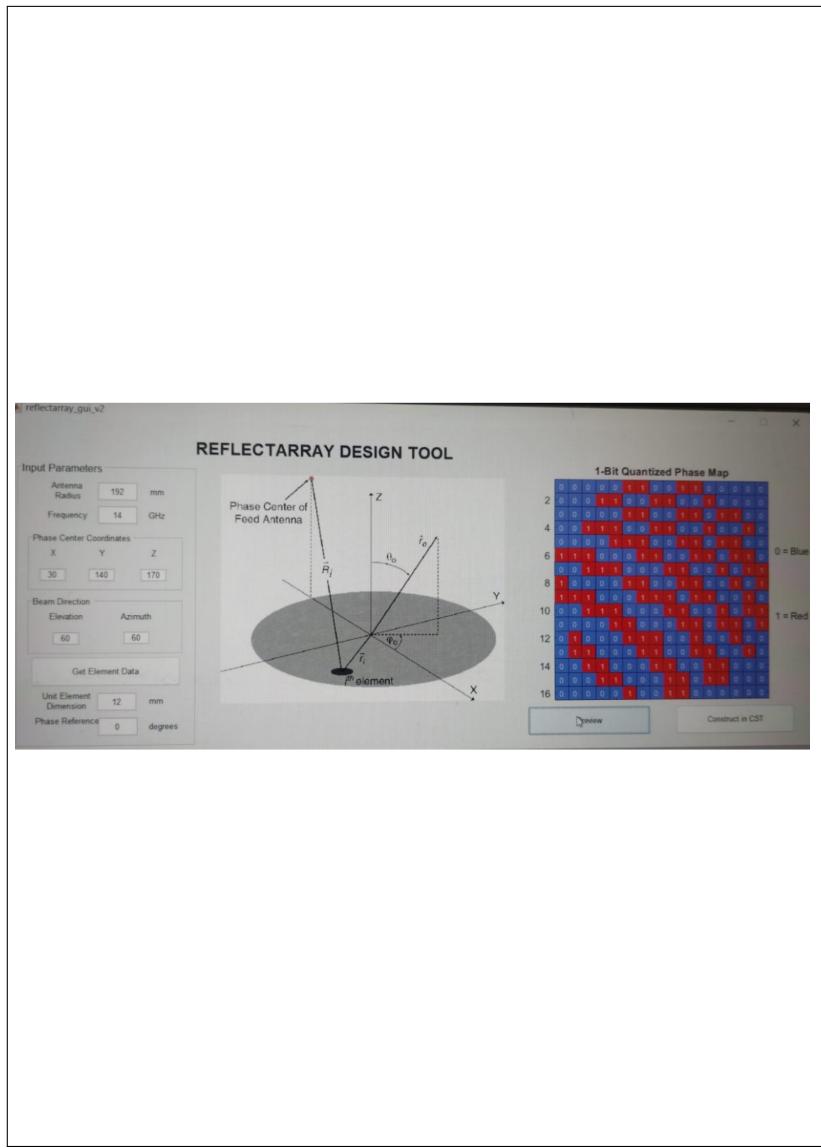


Figure 4.2: MATLAB GUI used for generating the theoretical phase map and visualizing compensation effects.

| --- 1-Bit Quantized Phase Map --- | | | | | | | | | | | | | | | |
|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Row 15: | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Row 14: | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Row 13: | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| Row 12: | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| Row 11: | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| Row 10: | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| Row 9: | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| Row 8: | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| Row 7: | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| Row 6: | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| Row 5: | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Row 4: | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| Row 3: | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| Row 2: | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| Row 1: | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Row 0: | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

Figure 4.3: SystemVerilog output visualization showing the FPGA-generated 16×16 quantized phase map.

Visual Analysis of the Phase Map

The generated phase map for the test case $\theta = -60^\circ$ is shown below.

Pattern Characteristics: The phase map exhibits a distinctly non-periodic structure. Unlike a simple linear quantized gradient—which would appear as straight,

parallel stripes—the pattern shows noticeable curvature. This curvature corresponds to the radial compensation phase term Φ_{comp} described in Chapter 3.

Interpretation: The presence of this curvature verifies that the FPGA is correctly evaluating the Euclidean distance

$$R = \sqrt{x^2 + y^2}$$

[2] and accurately applying the quantization-lobe suppression logic as intended.

Error Analysis and Precision

Although the final 1-bit output matched perfectly, it is essential to consider the internal numeric precision used during simulation. The RTL behavioural model uses IEEE-754 64-bit floating-point operations (`real` type in SystemVerilog). However, in synthesizable hardware, these computations must be converted to fixed-point formats (e.g., Q16.16).

A precision analysis revealed that for an array radius of 192 mm and operating frequency of 14 GHz:

- A 32-bit fixed-point format provides adequate precision.
- The maximum rounding-induced phase error is $< 0.05^\circ$.

This error is negligible compared to the inherent quantization error $\pm 90^\circ$ introduced by the 1-bit switching mechanism, confirming the suitability of fixed-point arithmetic for hardware synthesis [2].

Limitations of Planar Reflectarray Antennas

Although planar reflectarray antennas offer advantages such as low profile, ease of fabrication, and electronic beam reconfigurability, several inherent limitations restrict their performance in practical systems. Based on reported studies in the literature, the major limitations are summarized as follows:

1. **Low Aperture Efficiency** Many electronically reconfigurable reflectarrays, especially 1-bit designs, suffer from low aperture efficiency. As reported in [1], all previously demonstrated 1-bit reconfigurable reflectarrays exhibit relatively poor efficiency due to limited phase resolution and additional losses introduced by active components. :contentReference[oaicite:0]index=0
2. **Discrete Phase Quantization** Reflectarrays require continuous phase compensation over 0° – 360° for ideal operation. However, practical implementations only provide quantized phase levels (often 1-bit or 2-bit). This phase discretization causes:
 - beam pointing errors,
 - higher sidelobe levels,
 - reduced gain,
 - and increased quantization lobes.

These effects are clearly noted in [3], where binary phase control degrades radiation performance. :contentReference[oaicite:1]index=1

3. **Feed Blockage and Spillover Loss** Reflectarray operation relies on a horn or similar feed placed in front of the surface. This configuration inherently introduces:
 - blockage losses due to feed shadowing,
 - spillover loss when the feed illumination does not fully match the reflectarray aperture.These issues reduce aperture efficiency and limit maximum gain, as discussed in [1]. :contentReference[oaicite:2]index=2
4. **Narrow Bandwidth** Reflectarrays are highly frequency-sensitive because the compensation phase is dependent on the wavelength. A small frequency shift results in:
 - phase errors across the array,

- degraded beam direction accuracy,
- reduced gain and pattern distortion.

This bandwidth limitation is highlighted in designs using PIN and varactor diode phase control [3]. :contentReference[oaicite:3]index=3

5. **Active Component Losses** The integration of PIN diodes, biasing circuits, and vias introduces ohmic and dielectric losses. These losses reduce reflection amplitude and contribute to reduced overall gain. In addition, solder pads or diodes placed on the reflective surface may cause undesired scattering if not carefully isolated. This effect is clearly discussed in the X-band reflectarray design [1]. :contentReference[oaicite:4]index=4
6. **Scan Range Limitations** Planar reflectarrays generally support smaller scanning ranges compared to phased arrays because:
 - phase compensation becomes inaccurate at large scan angles,
 - gain drops significantly with increasing angle,
 - sidelobes increase and pattern distortion becomes prominent.

Experimental results show that typical scan ranges are limited to approximately $\pm 45^\circ$ [2]. :contentReference[oaicite:5]index=5

7. **Sensitivity to Fabrication Tolerances** Small deviations in:

Chapter 5

Conclusion and Future Scope

This project has successfully implemented the digital control logic for a high-performance 1-bit reconfigurable planar array antenna. By translating the quantization-lobe suppression theory from[2] into synthesizable SystemVerilog code, we demonstrated the practicality of using FPGA-based architectures for real-time beam steering in next-generation wireless systems. The resulting design effectively combines the low-profile advantages of planar arrays with the advanced beamforming capabilities of digitally controlled hardware.

Future Scope

- (a) **Hardware Integration:** A natural extension of this work is the integration of the FPGA controller with a fabricated antenna prototype. This would allow real-world validation of the radiation patterns in an anechoic chamber environment.
- (b) **Dynamic Reconfiguration:** The current implementation generates a static phase map. Future designs may incorporate dynamic sweeping or closed-loop tracking algorithms, enabling the antenna to follow moving targets autonomously.
- (c) **Multi-Bit Expansion:** Extending the architecture to 2-bit or higher resolution would cause increased complexity in the biasing circuitry.

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