PROJECT WORK

"Verilog Implementation of Digital Circuit Designs on FPGA using Vivado"

Topic: Traffic Light Controller Design using Verilog

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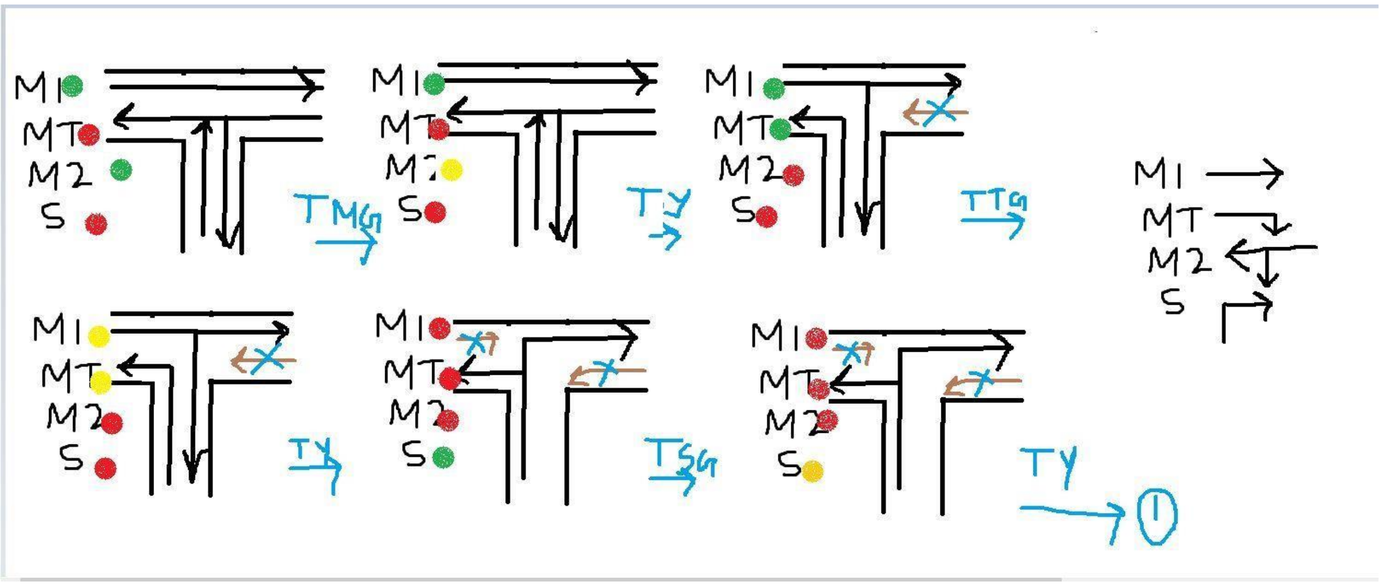
Semester:6

PROBLEM STATEMENT

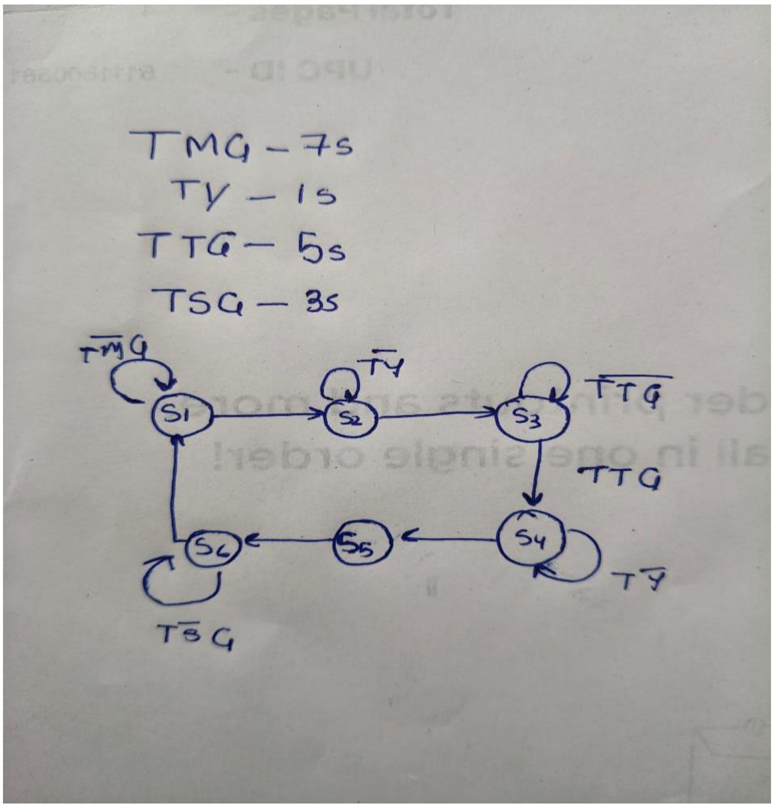
The aim of the project is to design a traffic controller for a T-intersection.

Let’s understand the problem statement through the image given below.

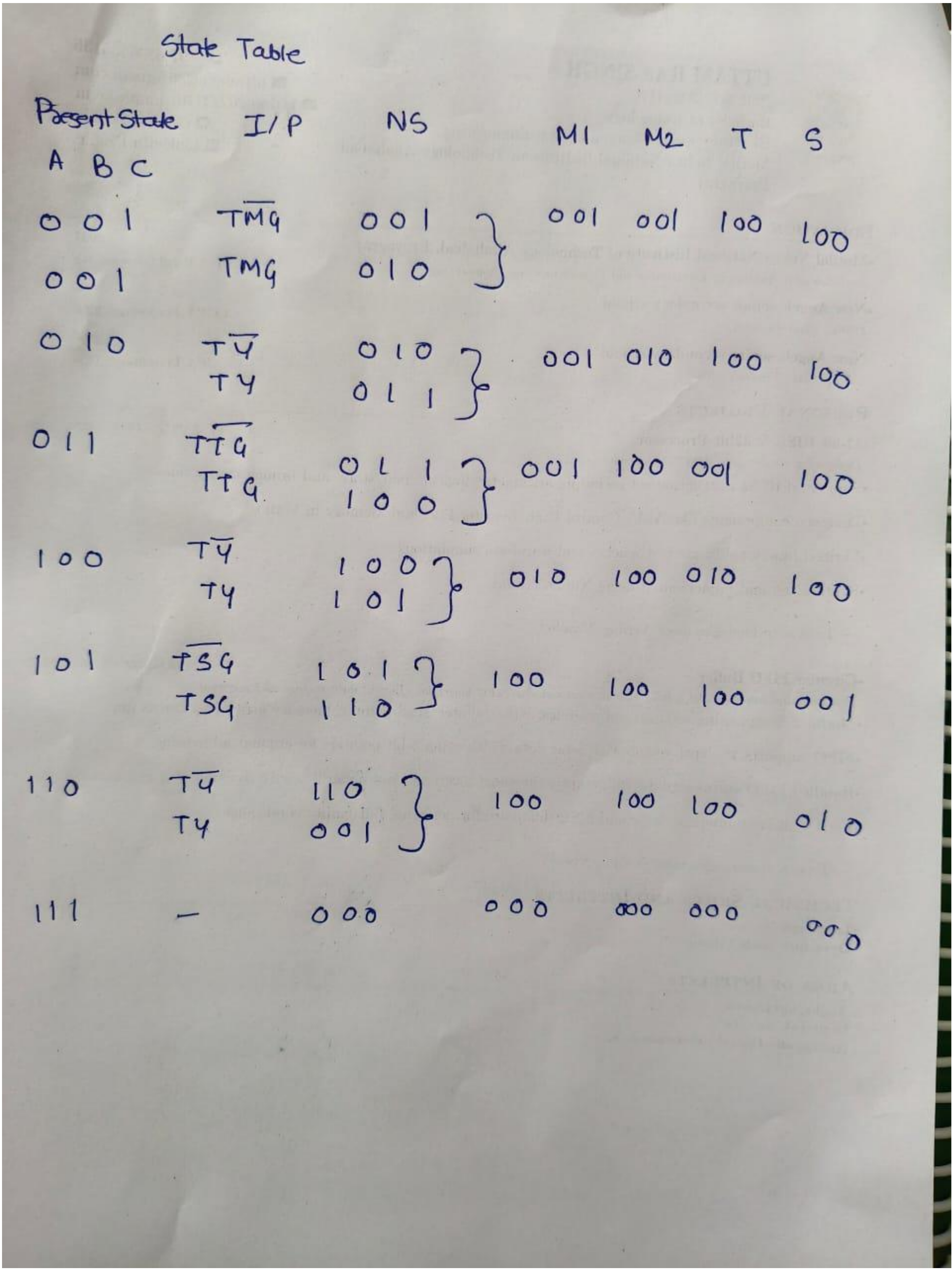


The six cases present here eventually turn to the six states .

This is the state diagram:



From the state diagram we for the state table:



State Table

Present State A B C	I/P	NS	M1	M2	T	S
0 0 1	$T\overline{MG}$	0 0 1	001	001	100	100
0 0 1	TMG	0 1 0				
0 1 0	$T\overline{Y}$	0 1 0	001	010	100	100
	TY	0 1 1				
0 1 1	$T\overline{TG}$	0 1 1	001	100	001	100
	TTG	1 0 0				
1 0 0	$T\overline{Y}$	1 0 0	010	100	010	100
	TY	1 0 1				
1 0 1	$T\overline{SG}$	1 0 1	100	100	100	001
	TSG	1 1 0				
110	$T\overline{Y}$	110	100	100	100	010
	TY	001				
111	–	000	000	000	000	000

VERILOG CODE

```
`timescale 1ns / 1ps


module Traffic_Light_Controller(


    input clk,rst,
    output reg [2:0]light_M1,
    output reg [2:0]light_S,
    output reg [2:0]light_MT,
    output reg [2:0]light_M2
    );

    parameter  S1=0, S2=1, S3 =2, S4=3, S5=4,S6=5;
    reg  [3:0]count;
    reg[2:0] ps;
    parameter  sec7=7,sec5=5,sec2=2,sec3=3;



    always@(posedge clk or posedge rst)
       begin
       if(rst==1)
       begin
       ps<=S1;
       count<=0;
       end
       else




          case(ps)
             S1: if(count<sec7)
                   begin
                   ps<=S1;
                   count<=count+1;
                   end
                else
                   begin
```

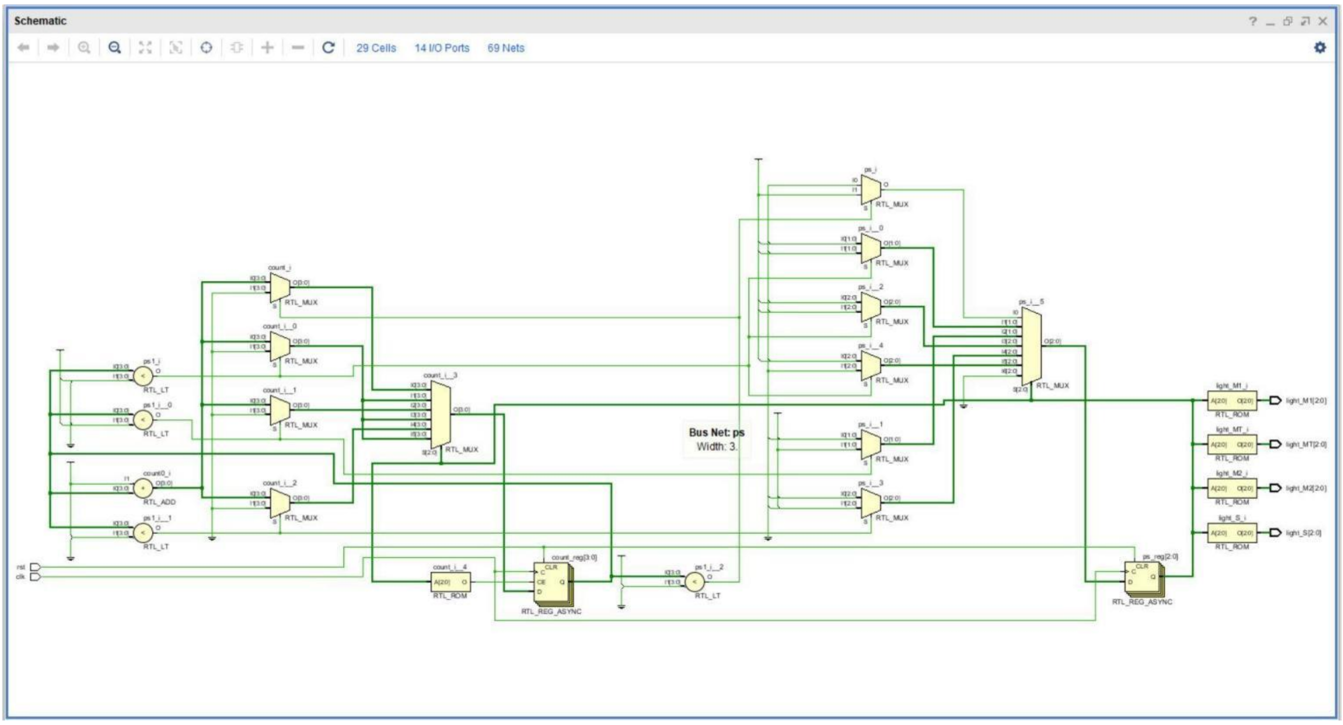
```
        ps<=S2;
        count<=0;
        end
S2: if(count<sec2)
        begin
        ps<=S2;
        count<=count+1;
        end

    else
        begin
        ps<=S3;
        count<=0;
        end
S3: if(count<sec5)
        begin
        ps<=S3;
        count<=count+1;
        end

    else
        begin
        ps<=S4;
        count<=0;
        end
S4:if(count<sec2)
        begin
        ps<=S4;
        count<=count+1;
        end
```

```
   else
       begin
       ps<=S5;
       count<=0;
       end
S5:if(count<sec3)
       begin
       ps<=S5;
       count<=count+1;
       end

   else
       begin
       ps<=S6;
       count<=0;
       end

S6:if(count<sec2)
       begin
       ps<=S6;
       count<=count+1;
       end

   else
       begin
       ps<=S1;
       count<=0;
       end
default: ps<=S1;
```

```
    endcase
end

always@(ps)
begin
    case(ps)

        S1:
        begin
           light_M1<=3'b001;
           light_M2<=3'b001;
           light_MT<=3'b100;
           light_S<=3'b100;
        end
        S2:
        begin
           light_M1<=3'b001;
           light_M2<=3'b010;
           light_MT<=3'b100;
           light_S<=3'b100;
        end
        S3:
        begin
           light_M1<=3'b001;
           light_M2<=3'b100;
           light_MT<=3'b001;
           light_S<=3'b100;
        end
        S4:
        begin
```

```
              light_M1<=3'b010;
              light_M2<=3'b100;
              light_MT<=3'b010;
              light_S<=3'b100;
            end
            S5:
            begin
              light_M1<=3'b100;
              light_M2<=3'b100;
              light_MT<=3'b100;
              light_S<=3'b001;
            end
            S6:
            begin
              light_M1<=3'b100;
              light_M2<=3'b100;
              light_MT<=3'b100;
              light_S<=3'b100;
            end
            default:
            begin
              light_M1<=3'b000;
              light_M2<=3'b000;
              light_MT<=3'b000;
              light_S<=3'b010;
            end
            endcase
end

endmodule
```

RTL-SCHEMATIC

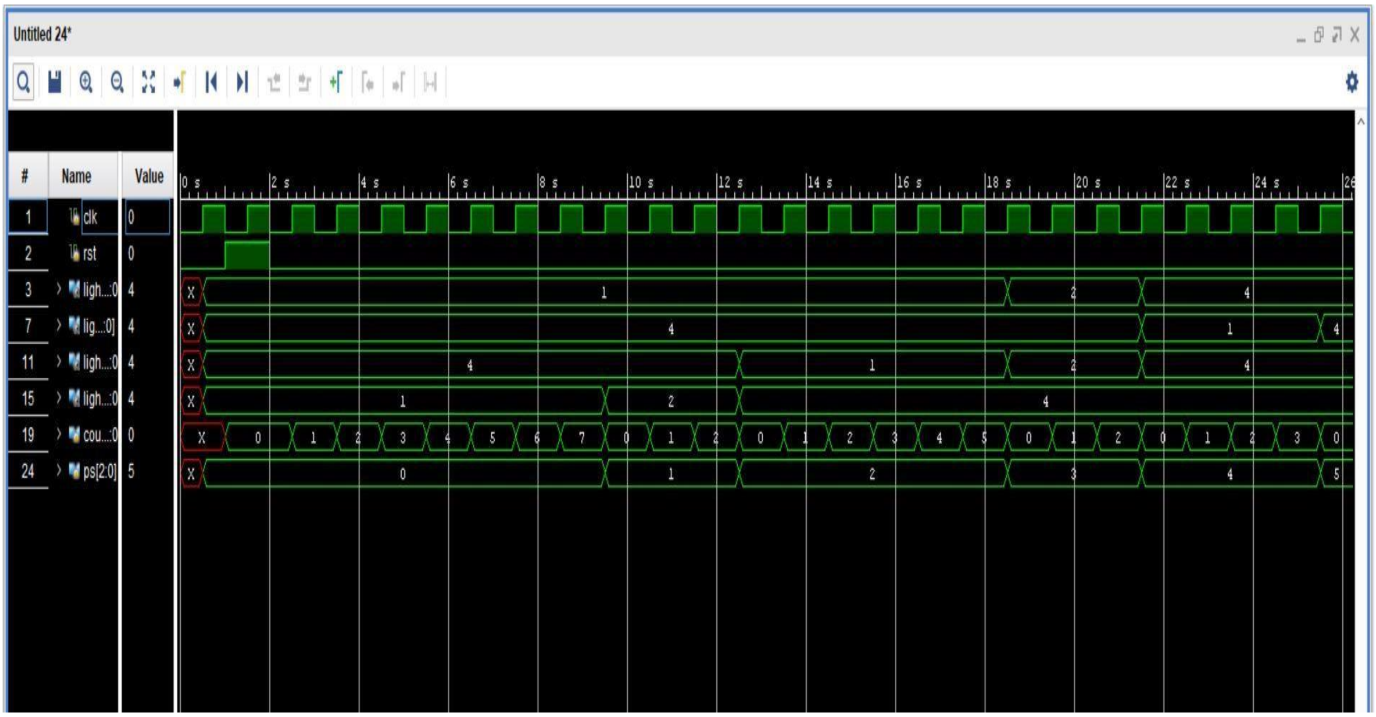


TESTBENCH

```
`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 16.07.2020 23:44:40

// Design Name:

// Module Name: Traffic_Light_Controller_TB

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:
```

```
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module Traffic_Light_Controller_TB;
reg clk,rst;
wire    [2:0]light_M1;
wire       [2:0]light_S;
wire    [2:0]light_MT;
wire [2:0]light_M2;
Traffic_Light_Controller dut(.clk(clk) , .rst(rst) , .light_M1(light_M1) , .light_S(light_S)
,.light_M2(light_M2),.light_MT(light_MT)           );
initial
begin
   clk=1'b0;
   forever   #(1000000000/2)   clk=~clk;
end
initial
begin
   rst=0;
   #1000000000;
   rst=1;
   #1000000000;
   rst=0;
   #(1000000000*200);
   $finish;
   end
endmodule
```

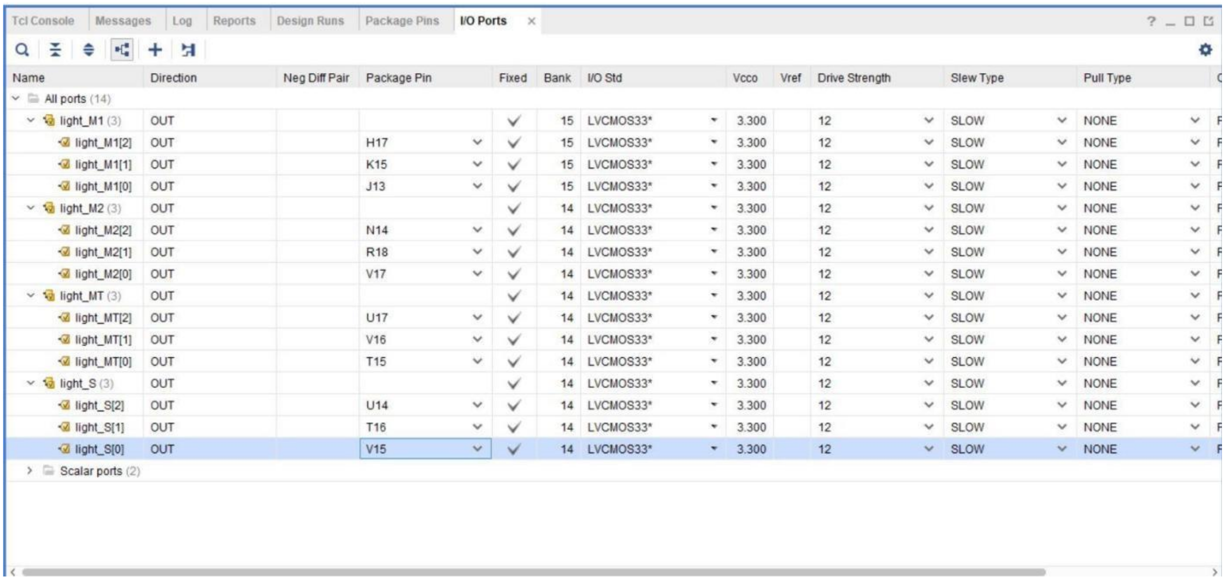
SIMULATED WAVEFORM



#	Name	Value
1	clk	0
2	rst	0
3	ligh...:0	4
7	lig...:0]	4
11	ligh...:0	4
15	ligh...:0	4
19	cou...:0	0
24	ps[2:0]	5

Upon analysing the waveform we can clearly see that the FSM works perfectly.

IO PORT ASSIGNMENT



Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	C
All ports (14)												
light_M1 (3)	OUT			✓	15	LVCMOS33*	3.300		12	SLOW	NONE	F
light_M1[2]	OUT		H17	✓	15	LVCMOS33*	3.300		12	SLOW	NONE	F
light_M1[1]	OUT		K15	✓	15	LVCMOS33*	3.300		12	SLOW	NONE	F
light_M1[0]	OUT		J13	✓	15	LVCMOS33*	3.300		12	SLOW	NONE	F
light_M2 (3)	OUT			✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_M2[2]	OUT		N14	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_M2[1]	OUT		R18	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_M2[0]	OUT		V17	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_MT (3)	OUT			✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_MT[2]	OUT		U17	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_MT[1]	OUT		V16	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_MT[0]	OUT		T15	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_S (3)	OUT			✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_S[2]	OUT		U14	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_S[1]	OUT		T16	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
light_S[0]	OUT		V15	✓	14	LVCMOS33*	3.300		12	SLOW	NONE	F
Scalar ports (2)												

The ports are assigned from the ucf file .