Kushal Dalal
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# LAB01 – CPS590

1.

**FETCH STAGE**

Memory

| | |
|---|---|
| 300 | **3705** |
| 301 | **5305** |
| 302 | **7706** |
| 303 | 0000 |
| 304 | 0000 |
| 305 | 0002 |

CPU Registers

| | |
|---|---|
| 300 | PC |
| 0000 | AC |
| 3705 | IR |

| | |
|---|---|
| 0003 | Device 5 |
| 0000 | Device 6 |

**EXECUTE STAGE**

Memory

| | |
|---|---|
| 300 | **3705** |
| 301 | **5305** |
| 302 | **7706** |
| 303 | 0000 |
| 304 | 0000 |
| 305 | 0002 |

CPU Registers

| | |
|---|---|
| 301 | PC |
| 0003 | AC |
| 3705 | IR |

| | |
|---|---|
| 0003 | Device 5 |
| 0000 | Device 6 |

**FETCH STAGE**

Memory

| | |
|---|---|
| 300 | **3705** |
| 301 | **5305** |
| 302 | **7706** |
| 303 | 0000 |
| 304 | 0000 |
| 305 | 0002 |

CPU Registers

| | |
|---|---|
| 301 | PC |
| 0003 | AC |
| 5305 | IR |

| | |
|---|---|
| 0003 | Device 5 |
| 0000 | Device 6 |

**EXECUTE STAGE**

Memory

| | |
|---|---|
| 300 | **3705** |
| 301 | **5305** |
| 302 | **7706** |
| 303 | 0000 |
| 304 | 0000 |
| 305 | 0002 |

CPU Registers

| | |
|---|---|
| 302 | PC |
| 0005 | AC |
| 5305 | IR |

| | |
|---|---|
| 0003 | Device 5 |
| 0000 | Device 6 |

**FETCH STAGE**

Memory

| | |
|---|---|
| 300 | **3705** |
| 301 | **5305** |
| 302 | **7706** |
| 303 | 0000 |
| 304 | 0000 |
| 305 | 0002 |

CPU Registers

| | |
|---|---|
| 302 | PC |
| 0005 | AC |
| 7706 | IR |

| | |
|---|---|
| 0003 | Device 5 |
| 0000 | Device 6 |

**EXECUTE STAGE**

Memory

| | |
|---|---|
| 300 | **3705** |
| 301 | **5305** |
| 302 | **7706** |
| 303 | 0000 |
| 304 | 0000 |
| 305 | 0002 |

CPU Registers

| | |
|---|---|
| 303 | PC |
| 0005 | AC |
| 7706 | IR |

| | |
|---|---|
| 0003 | Device 5 |
| 0005 | Device 6 |

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2.

a) If the OS disables interrupts while an interrupt is being processed,

| Interrupt Number | Interrupt Start Time | Interrupt Finish Time |
|---|---|---|
| I1 | t = 10 | t = 40 |
| I2 | t = 20 | t = 50 |
| I3 | t = 30 | t = 100 |

b) If the OS processes multiple interrupts using a priority scheme,

| Interrupt Number | Interrupt Start Time | Interrupt Finish Time |
|---|---|---|
| I1 | t = 10 | t = 90 |
| I2 | t = 20 | t = 100 |
| I3 | t = 30 | t = 80 |

3. At 0.5 hit ratio would we be better off with just level 2 memory. We considered the average time as 1.0t which is same as level 2's access time because it would be greater than.