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MATHURA
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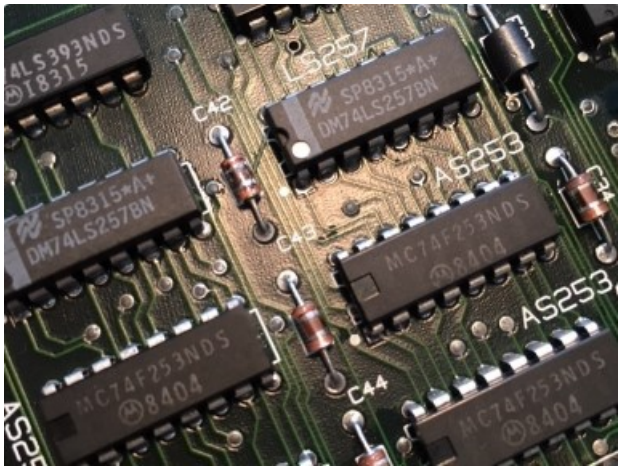
Fundamentals of Computer Science (MCAC-0017)

COMBINATIONAL CIRCUITS



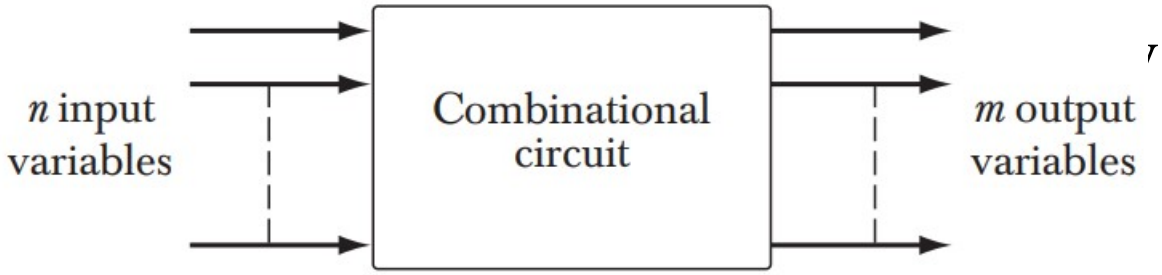
Overview

- Introduction to Combinational Circuits
- Adder
- Ripple Carry Adder
- Subtraction
- Adder/Subtractor

Combinational Circuits

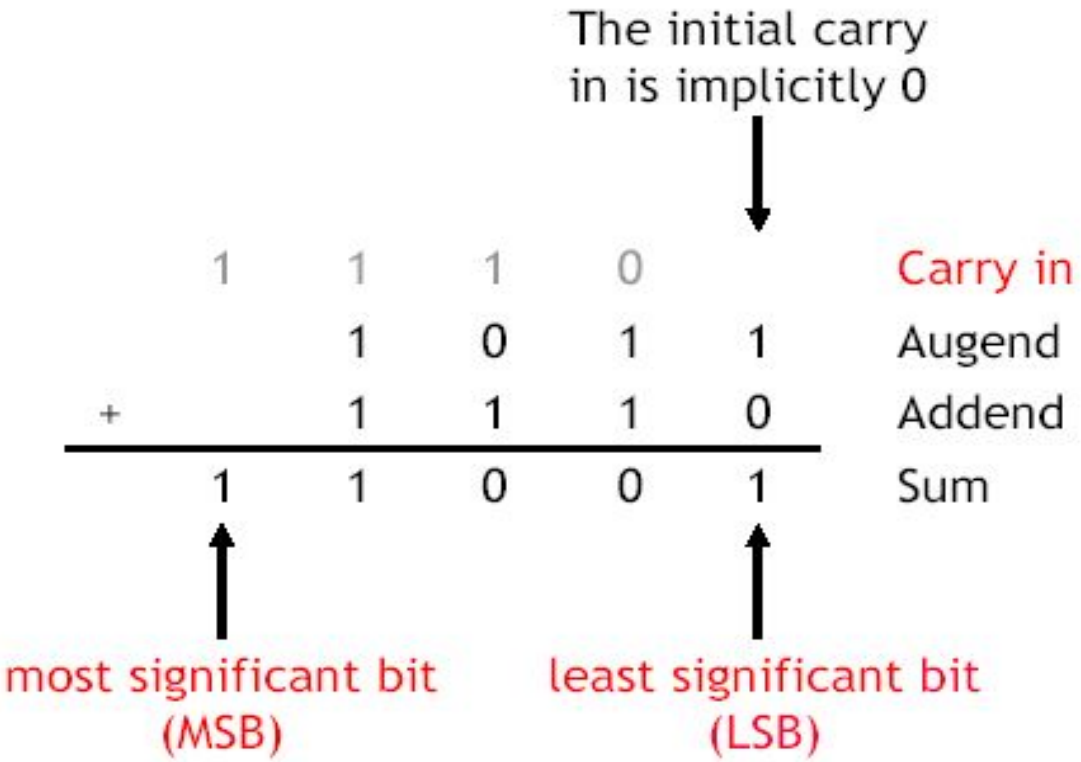
Digital logic circuits are basically categorized into two types:

1. Combinational circuits in which there are no feedback paths from outputs to inputs and there is no memory.
2. Sequential circuits in which feedback paths exist from ou[illegible].



Binary addition by hand

- You can add two binary numbers one column at a time starting from the right, just like you add two decimal numbers.
- But remember it's binary. For example, 1 + 1 = 10 and you have to carry!



Adder

- Design an Adder for 2-bit numbers?
- **1. Specification:**
  2 inputs (X,Y)
  2 outputs (C,S)

Adder

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  2 outputs (C,S)
- **2. Formulation:**

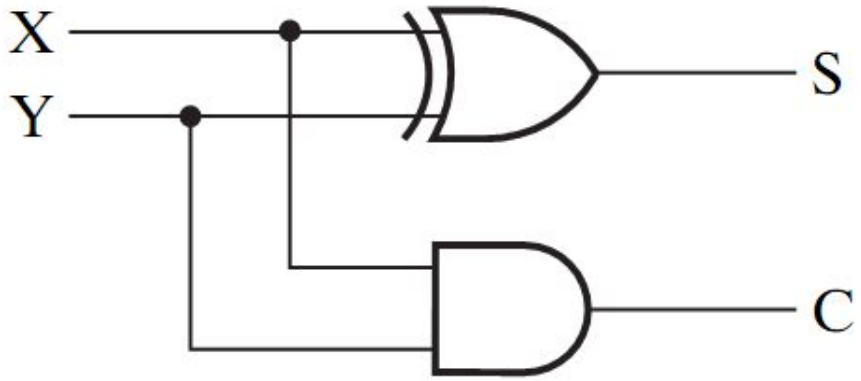
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Adder

- Design an Adder for 2-bit numbers?
- **1. Specification:**
  2 inputs (X,Y)
  2 outputs (C,S)
- **2. Formulation:**

3. Optimization/Circuit

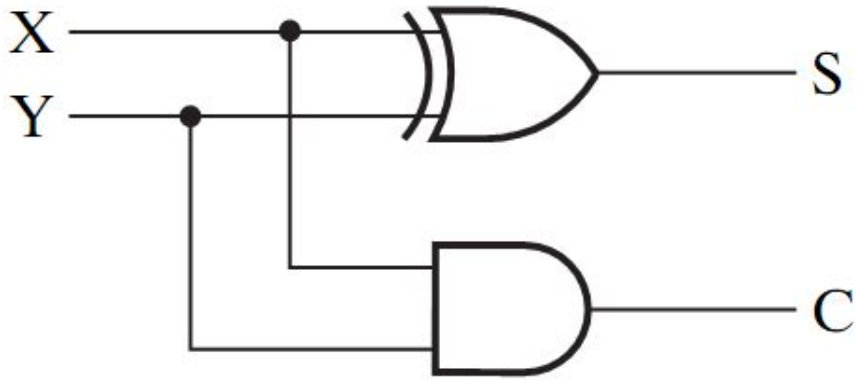
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Half Adder

- This adder is called a Half Adder
- **Q: Why?**

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Full Adder

- A combinational circuit that adds 3 input bits to generate a Sum bit and a Carry bit

- A truth table and sum of minterm equations for C and S are shown below.

0 + 1 + 1 = 10 →

1 + 1 + 1 = 11 →

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$C(X,Y,Z) = \Sigma m(3,5,6,7)$

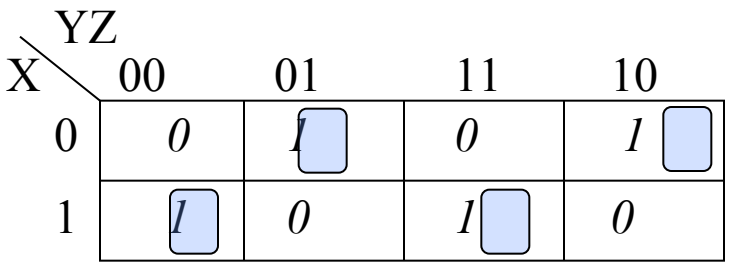
$S(X,Y,Z) = \Sigma m(1,2,4,7)$

Full Adder

- A combinational circuit that adds 3 input bits to generate a Sum bit and a Carry bit

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

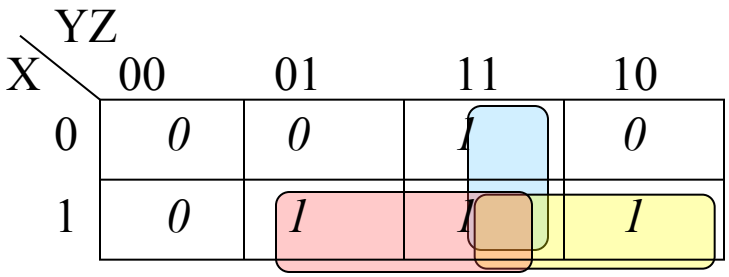
Sum



$S = X'Y'Z + X'YZ' + XY'Z' + XYZ$

$= X \oplus Y \oplus Z$

Carry



$C = XY + YZ + XZ$

Full Adder = 2 Half Adders

Manipulating the Equations:

$S = X \oplus Y \oplus Z$

$C = XY + XZ + YZ$

Full Adder = 2 Half Adders

Manipulating the Equations:

$$S = (X \oplus Y) \oplus Z$$

$$C = XY + XZ + YZ$$

$$= XY + XYZ + XY'Z + X'YZ + XYZ$$

$$= XY(1 + Z) + Z(XY' + X'Y)$$

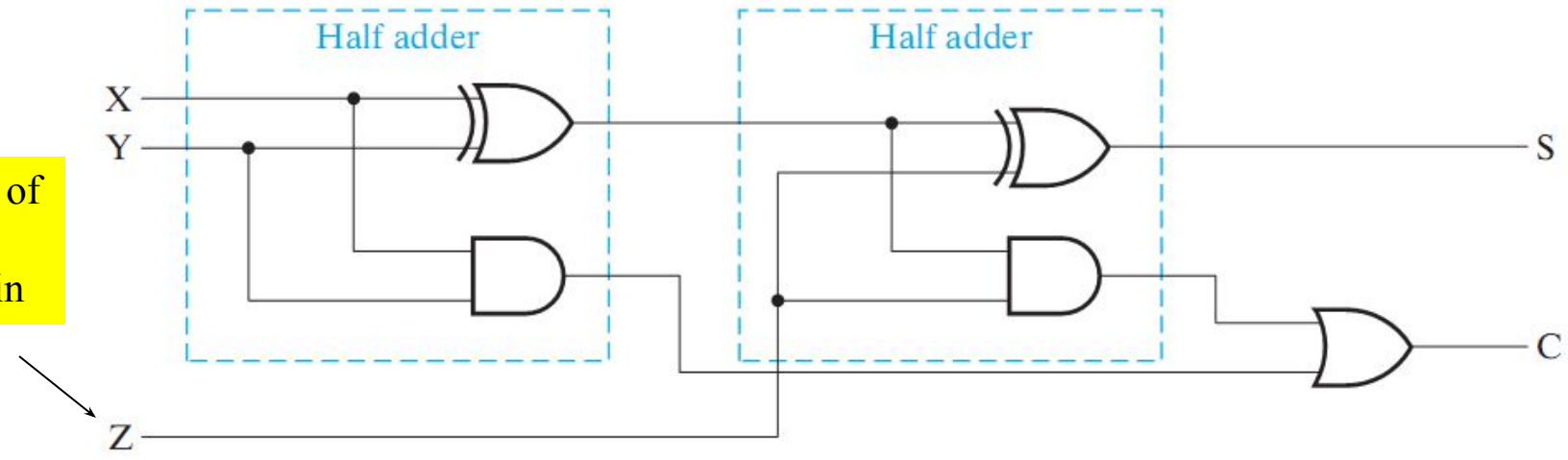
$$= XY + Z(X \oplus Y)$$

Full Adder = 2 Half Adders

Manipulating the Equations:

$$S = (X \oplus Y) \oplus Z$$

$$C = XY + XZ + YZ \; = XY + Z(X \oplus Y)$$



Think of Z as a carry in

Src: Mano's Book

Bigger Adders

- How to build an adder for n-bit numbers?
  - Example: 4-Bit Adder
    - Inputs ?
    - Outputs ?
    - What is the size of the truth table?
    - How many functions to optimize?

Bigger Adders

- How to build an adder for n-bit numbers?
  - Example: 4-Bit Adder
    - Inputs ? 9 inputs
    - Outputs ? 5 outputs
    - What is the size of the truth table? 512 rows!
    - How many functions to optimize? 5 functions

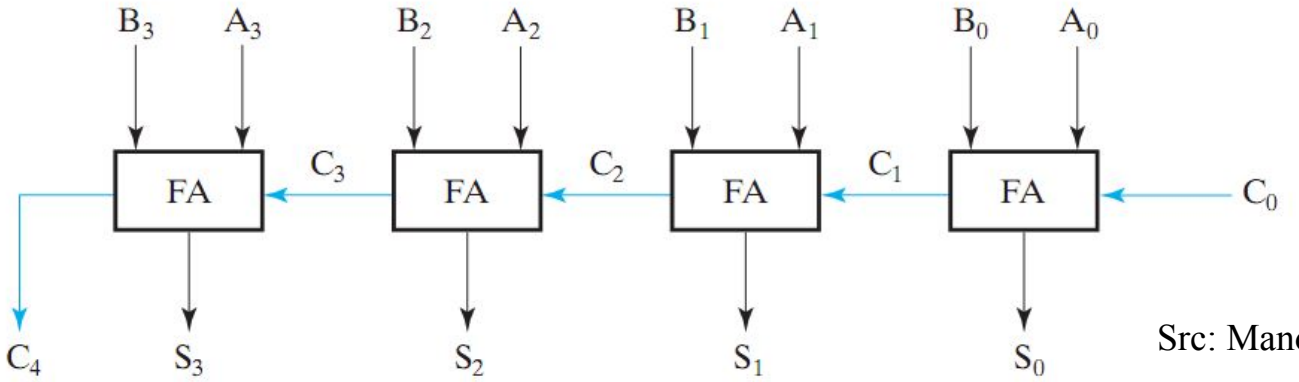
Ripple Carry Adder

- To add n-bit numbers:
  - Use n Full-Adders in parallel
  - The carries propagates as in addition by hand
  - Use Z in the circuit as a C_{in}

- 1 0 0 0
- 0 1 0 1
- 0 1 1 0
- 1 0 1 1

Binary Parallel Adder

- To add n-bit numbers:
  - Use n Full-Adders in parallel
  - The carries propagates as in addition by hand



Src: Mano's Book

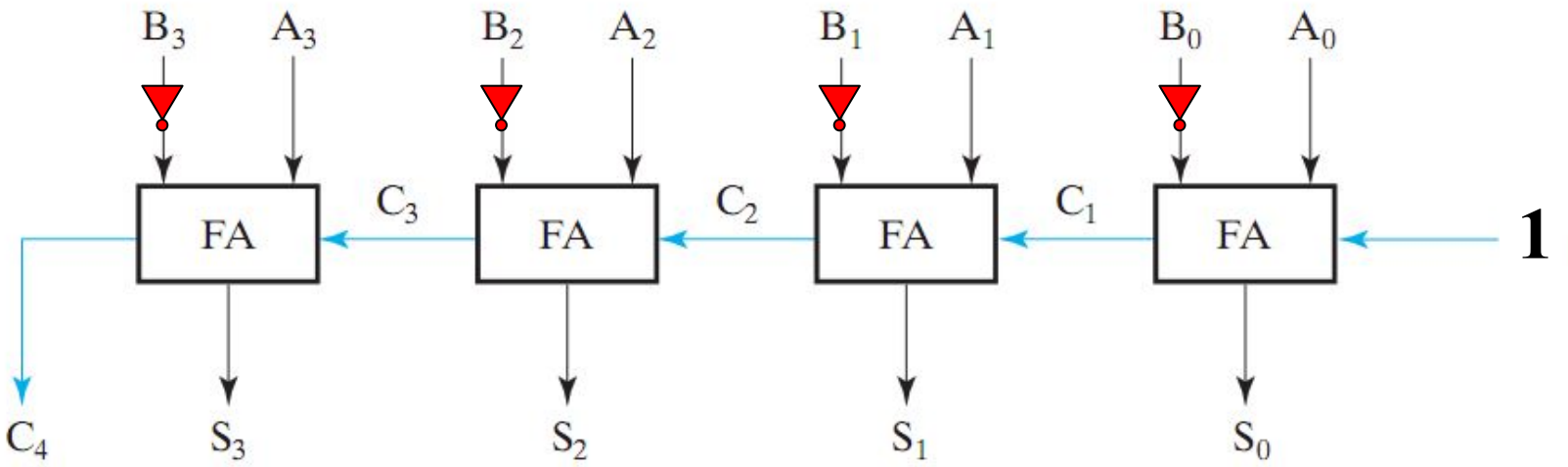
This adder is called ***ripple carry adder***

Subtraction (2’s Complement)

- How to build a subtractor using 2’s complement?

Subtraction (2's Complement)

- How to build a subtractor using 2's complement?



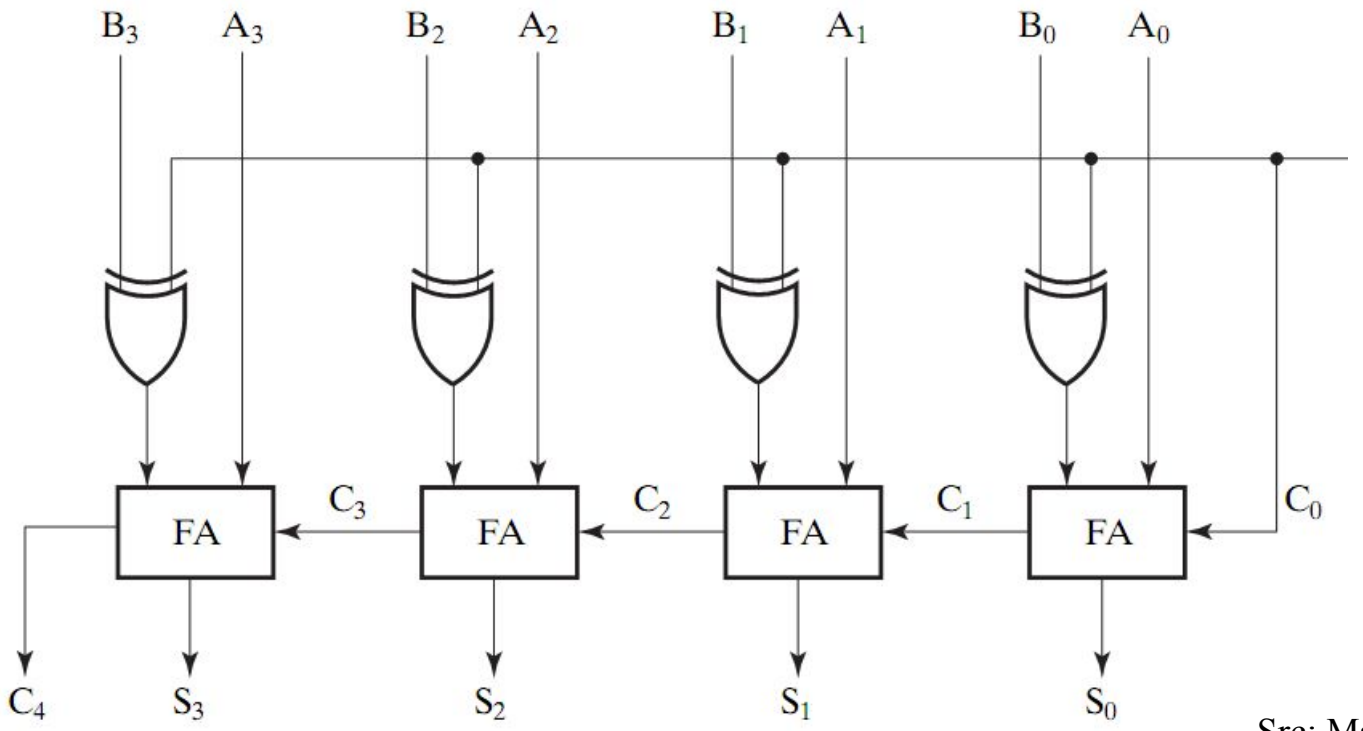
Src: Mano's Book

$$S = A + (-B)$$

Adder/Subtractor

- How to build a circuit that performs both addition and subtraction?

Adder/Subtractor

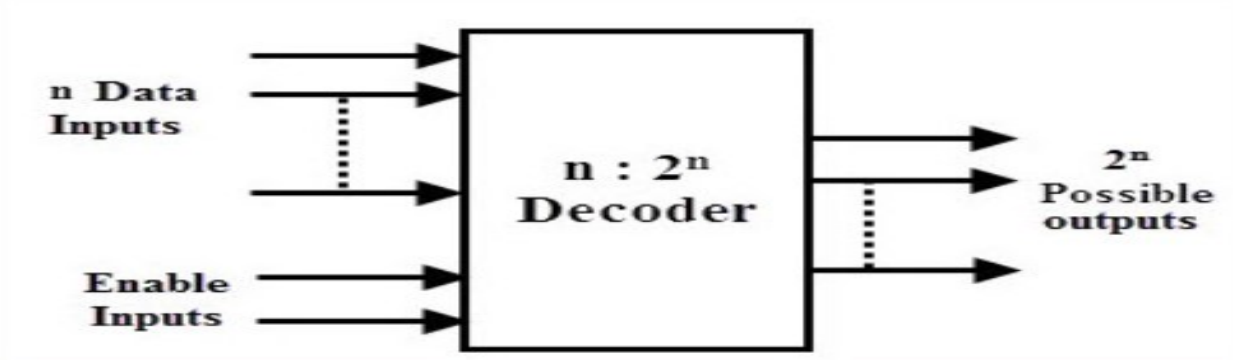


Src: Mano's Book

Using full adders and XOR we can build an Adder/Subtractor!

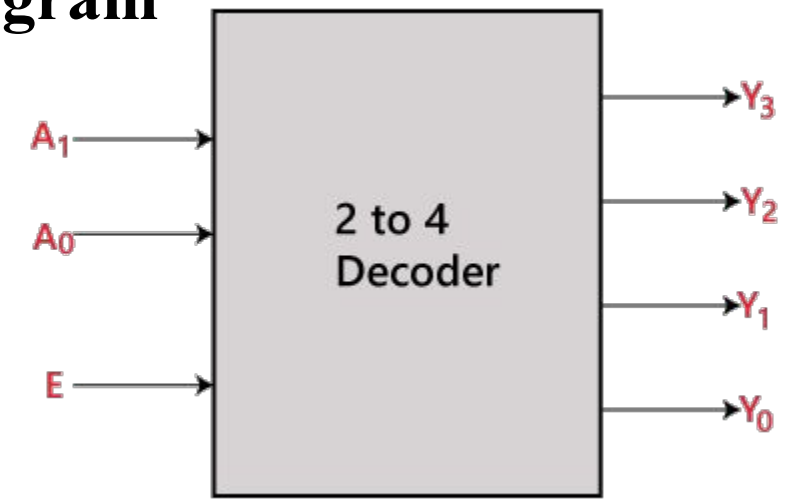
Decoders

- A decoder is a combinational circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs.
- The decoders presented are called n-to-m line decoders, where m<= 2^n . Their purpose is to generate the 2^n (or fewer) binary combinations of the n input variables. A decoder has n inputs and m outputs and is also referred to as an n x m decoder



2 to 4 line decoder

- In the 2 to 4 line decoder, there is a total of three inputs, i.e., A_0, and A_1 and E and four outputs, i.e., Y_0, Y_1, Y_2, and Y_3. For each combination of inputs, when the enable 'E' is set to 1, one of these four outputs will be 1.
- **Block Diagram**



Truth Table

Enable	INPUTS		OUTPUTS			
E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

The logical expression of the term Y0, Y0, Y2, and Y3 is as follows:

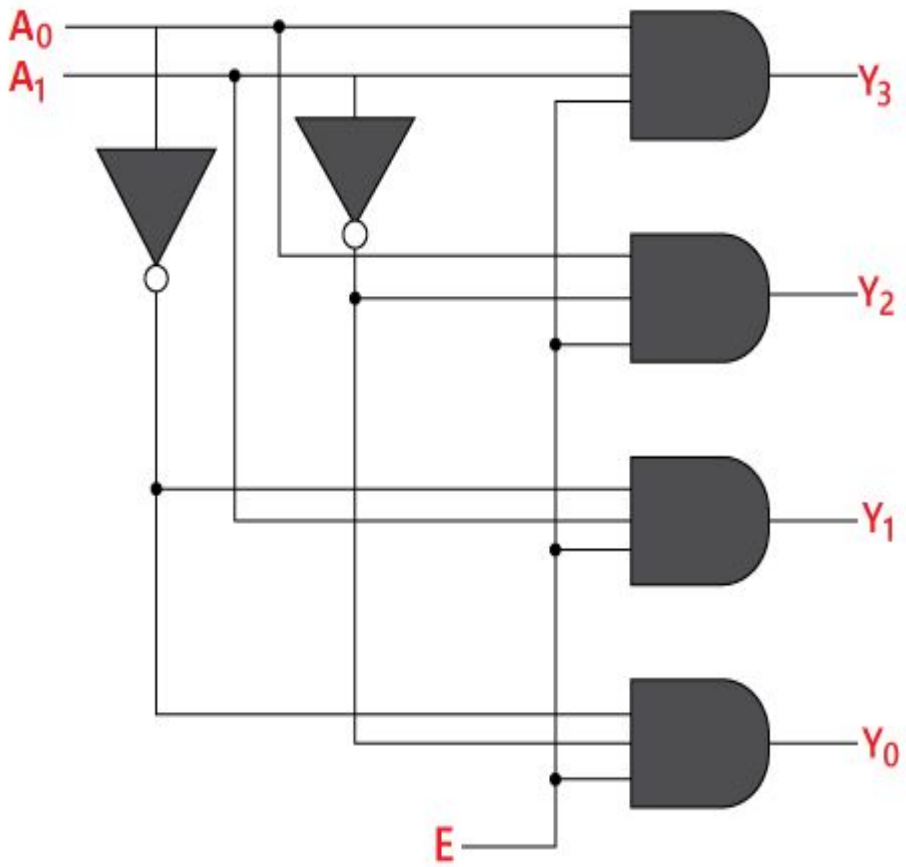
$Y_3=E.A_1.A_0$

$Y_2=E.A_1.A_0$,

$Y_1=E.A_1'.A_0$

$Y0=E.A_1'.A_0'$

Logical circuit of the above expressions is given below:

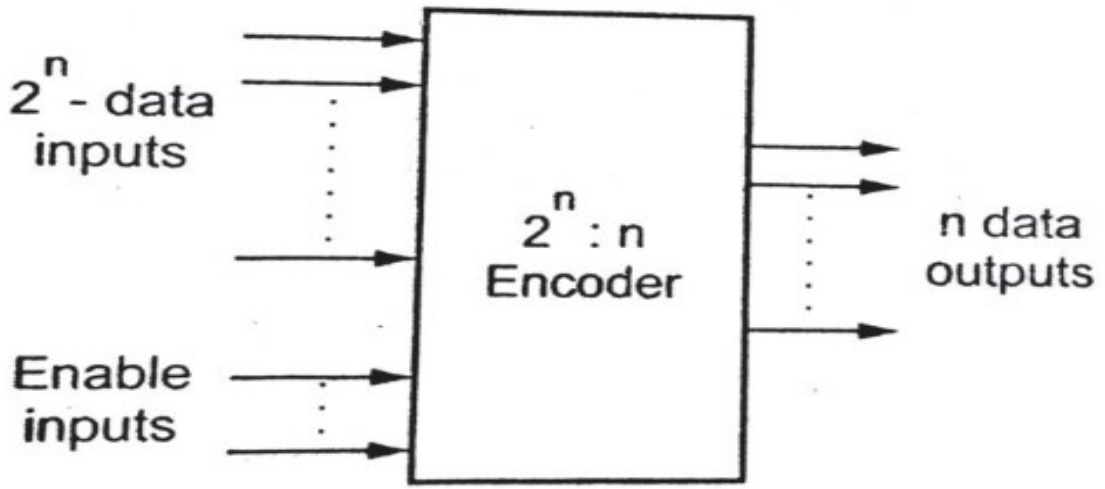


Applications of Decoders

- They may be used to route input data to a specified output line for example addressing for memory.
- Decoders are used in audio systems to convert analogue audio into digital data.
- Used as a decompressor to convert compressed data like images and videos into decompressed form.
- Decoders are also used as building blocks in implementing arbitrary switching functions.

Encoders

- An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2n (or less) input lines and n outputs lines. The output lines generate the binary code corresponding to the input value.
- An example of an encoder is the octal-to-binary encc



Block diagram of encoder

TABLE 2-2 Truth Table for Octal-to-Binary Encoder

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$$A0 = D1 + D3 + D5 + D7$$

$$A1 = D2 + D3 + D6 + D7$$

$$A2 = D4 + D5 + D6 + D7$$

- The encoder can be implemented with three OR gates.

Multiplexer (Data Selectors)

- The term Multiplexer means many into one.
- Multiplexing is the process of transmitting a large number of information over a single line.
- A Digital Multiplexer (MUX) is a combinational Circuit that select one digital information from several sources and transmits the selected information on a single output line.
- A Multiplexer is also called a Data Selector.
- The Multiplexer has several data input line and a single output line.

Cont.

- MUX directs one of the inputs to its output line by using a control bit word (*selection line) to its select lines.*
- Multiplexer contains the followings:

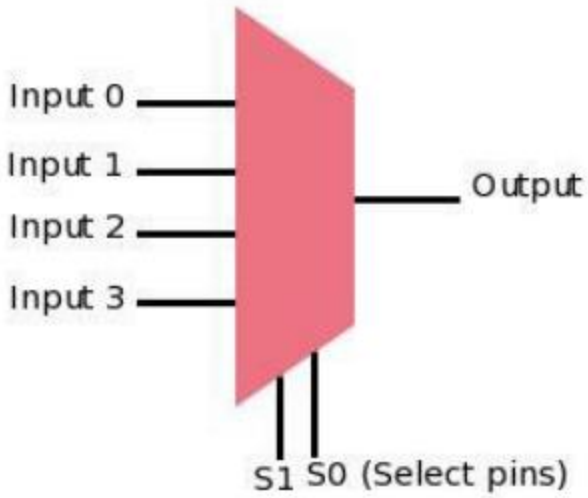
❖ data inputs

❖ selection inputs

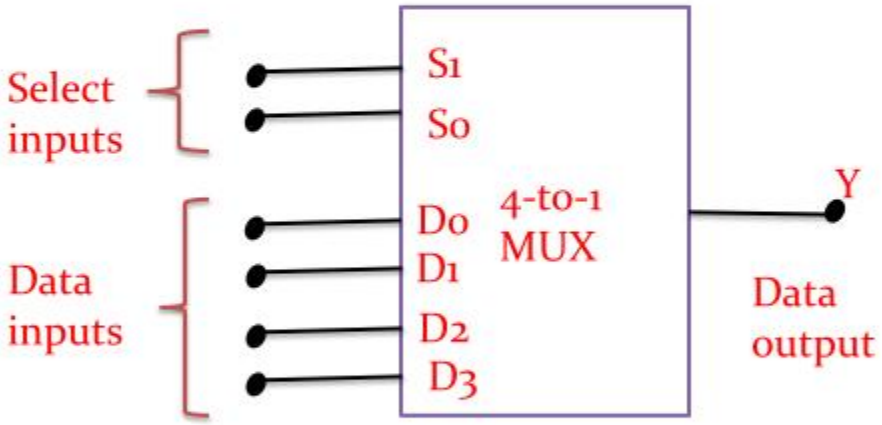
❖ a *single output*

- Selection input determines the input that should be connected to the output.
- The multiplexer acts like an electronic switch that selects one from different.

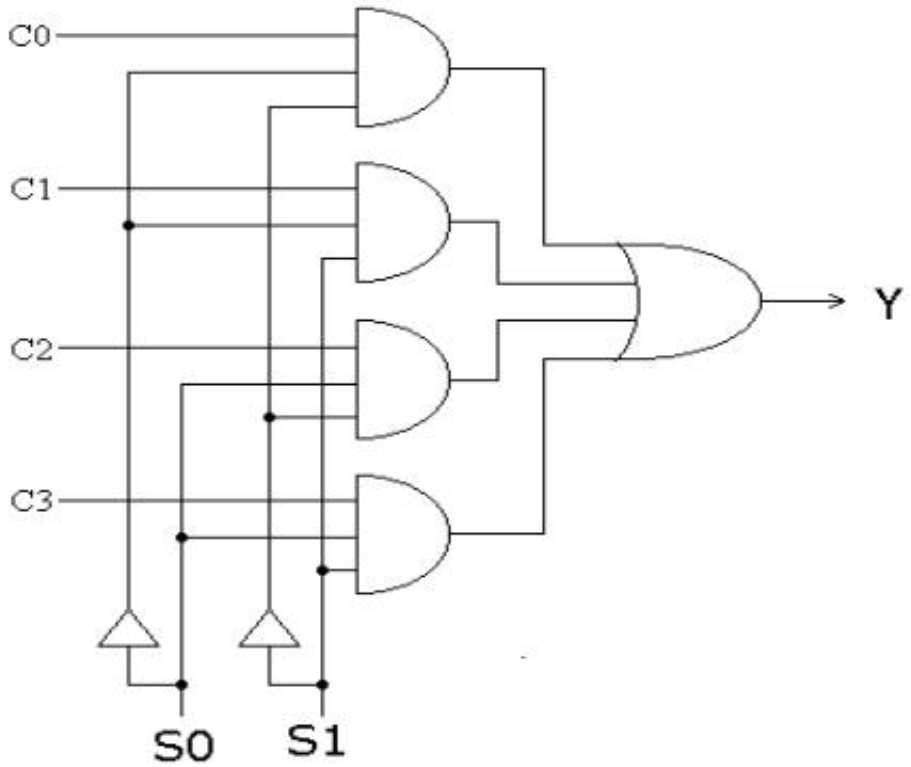
Block diagram of Multiplexer



4 to 1 Multiplexer Logic Symbol



4 to 1 Multiplexer Logic diagram



Cont.,

- To demonstrate the operation of the circuit, consider the case when S1 So =00.
- If S1 So =00 is applied to the select lines, the AND gate associated with Do will have two of its input equal to 1 and the third input connected to Do.
- The other three AND gates have 0 in at least one of their inputs, which make their output equal to 0.
- Hence, the OR output (Y) is equal to the value of Do.

Cont.,

- Thus, it provides a path from the selected input and the data on the input Do appears on the data-output line (Y).
- If S1 So =01 (binary 1) applied to the select lines , the data on the input D1 appears on the data output line.

Cont.,

- If S1 So =10 (binary 2) is applied, the data on the input D2 appears on the output line (Y).
- Similarly, if S1 So =11 is applied, the data on D3 is switched to the output line (Y).
- The AND gates and the inverters resemble a decoder circuit, and indeed they decode the input select lines.
- In general, a 2^n–to-1 multiplexer is constructed from n-to -2^n decoder by adding to it 2^n input lines, one each AND gate.

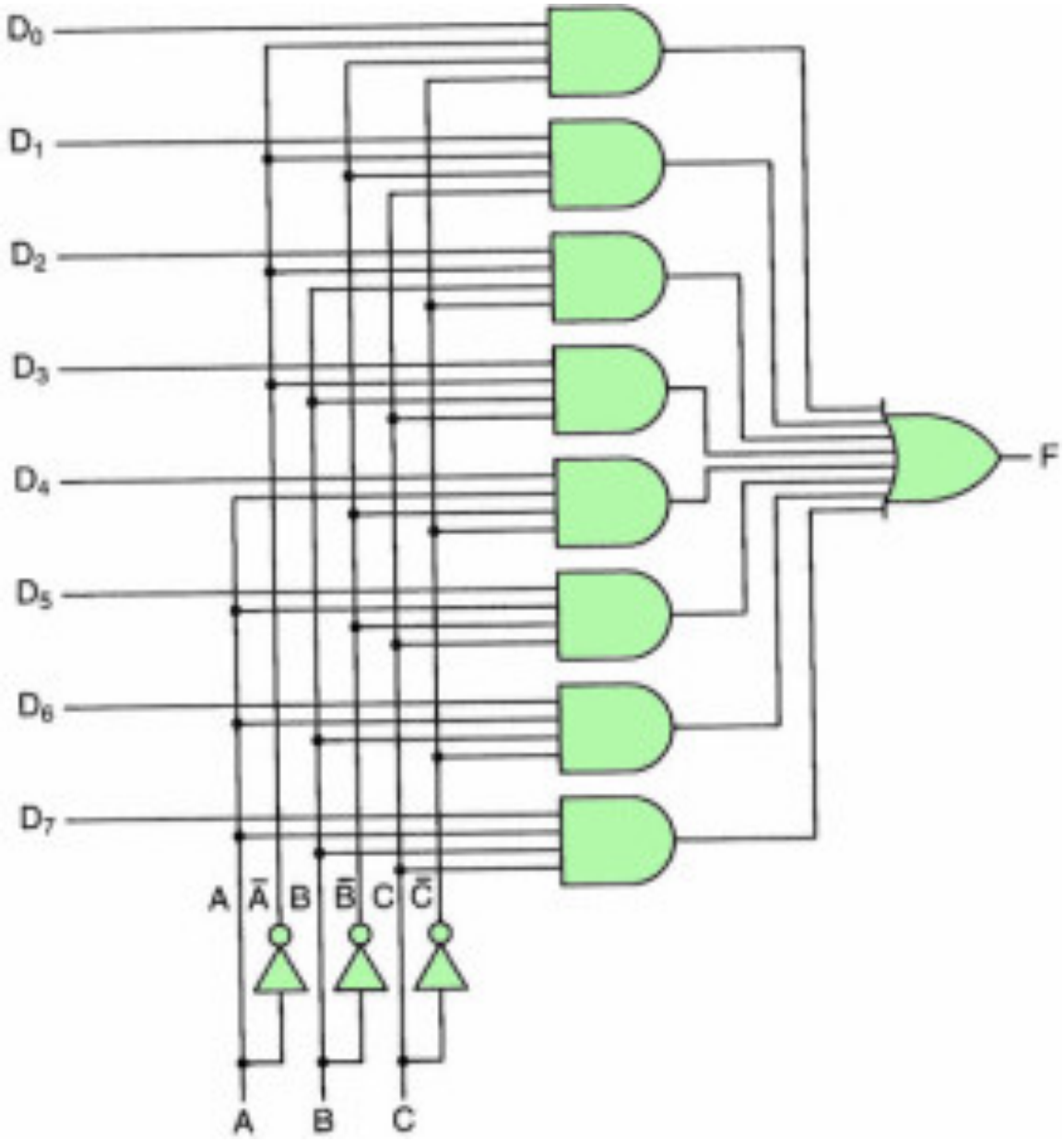
Cont.,

- The output of the AND gates are applied to a single OR gate to provide a single output.
- The size of the multiplexer is specified by the number 2^n of input lines and the single output line.
- Multiplexer ICs have an enable input to control the operation of the unit.
- The enable input (also called strobe) can be used to cascade two or more multiplexer ICs to construct a multiplexer with larger number of inputs

Truth table of 4-to-1 Multiplexer

Data select inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

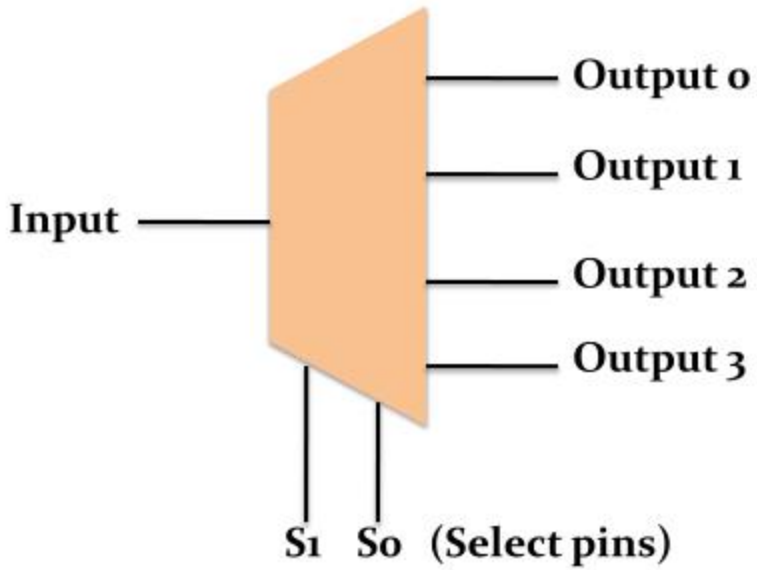
8-1 Multiplexer Circuit



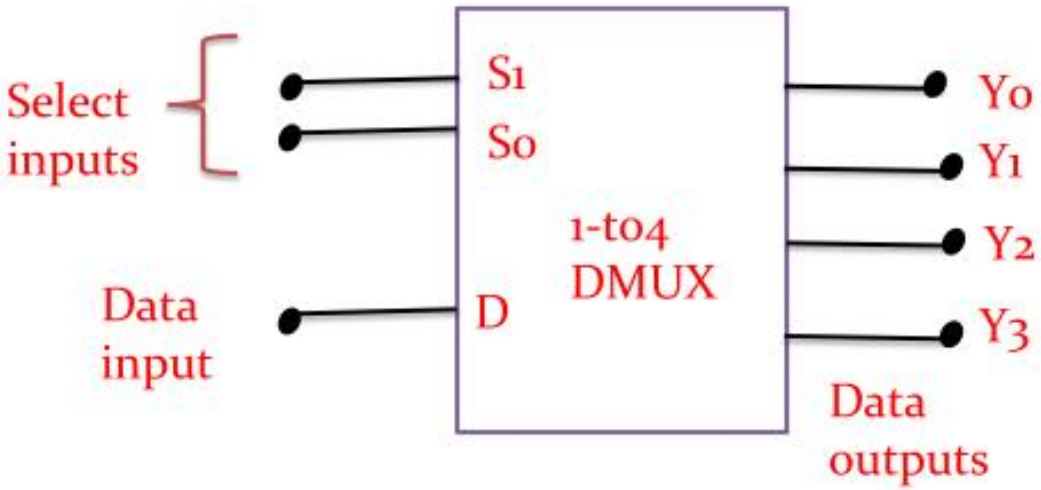
De-Multiplexer

- The De-Multiplexer is a combinational logic circuit that performs the reverse operation of multiplexer (Several output lines, one input line).
- De -Multiplexer means one to many. A De-Multiplexer is a circuit with one input and many output. By applying control signal, we can steer any input to the output. Few types of De -Multiplexer are 1-to 2, 1-to-4, 1-to-8 and 1-to 16 De -Multiplexer .
- De-Multiplexer is the process of taking information from one input and transmitting the same over one of several outputs.

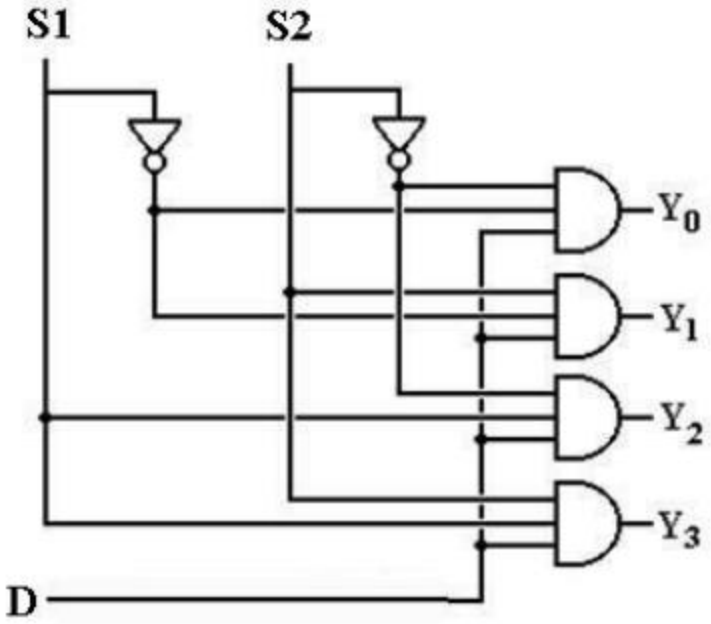
Block diagram of DeMultiplexer



1 to 4 DeMultiplexer Logic Symbol



1 to 4 DeMultiplexer Logic diagram



Truth Table of 1 to 4 DeMultiplexer

Data Input	Select Inputs		Output			
D	S_1	S_0	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

Thankyou

Any Query

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