

## Exercise 2

1. Use Karnaugh map for optimizing the following logical function  $d = f(a,b,c) = \cup(3, 5, 6, 7)$  and draw the circuit.
2. Replace all components in the diagram from point 1 with NAND gates
3. Using laboratory panels check whether circuits designed in point 1 and 2 work correctly (according to the table of truth).