Exercise 4

Design the cyclic counter using D or JK flip-flops, which counts clock pulses modulo 4. The output value is incremented by each pulse. NAND, NOR and NOT gates are also available.

If the input X=0, the counter counts up clock pulses (0,1,2,3,0,1,2,3,etc.); if the X=1 then the counter counts down (0,3,2,1,0,3,2,1, etc.).

During classes you will have to assemble the logic circuit using breadboard. Connect to LED bar the output of each flip-flop. Before the classes research the technical details and usage of flip-flops from the breadboard (i.e. 7474, 7476) including the truth table for D and JK flip-flops.