數位電路設計

Lab3 – 同步循序電路之 HDL 模組撰寫與測試

1. 目標(Goal)

在這次 Lab 中，我們希望同學們可以熟悉 Latch、正反器、同步循序電路的設計原理。以 **state-diagram-based model 與 structural model** 等不同方式撰寫同步循序電路之 Verilog HDL 電路模組，並撰寫測試模組。分別模擬後，繳交模組檔案與波形圖。

The main purpose of this Lab Unit is to be familiar with the design of latch, flip-flop, and synchronous sequential circuit. Please write the Verilog HDL circuit modules of synchronous sequential circuits by state-diagram-base model and structural model, and write the testbench for these circuit modules. After simulation, upload the files of the modules and the waveforms of the simulation results.

2. 撰寫 HDL 電路模組與測試模組(Design of the HDL Circuit Modules and Testbench)

A. SR-Latch: 下圖為一 SR-Latch 的電路圖，請設計其 Verilog HDL 電路模組。

The circuit diagram of a SR-Latch is shown in the following figure. Please write the Verilog circuit module for it.

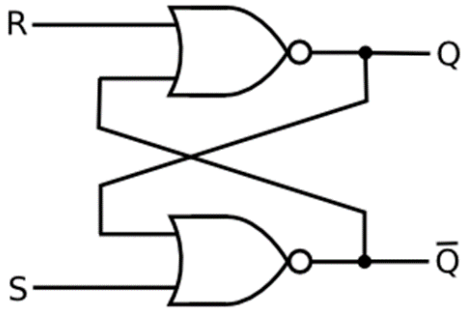


圖 1：S R -Latch 的電路圖

Figure 1: The circuit diagram of an SR-Latch.

i. 請根據上述電路圖(圖 1)，以 gate-level modeling 的方式撰寫其電路模組。假設每個 NOR gate 的 delay 為 2ns。模組名稱與 port list 請訂為 Lab3_SR_Latch_gatelevel(output Q, NQ, input S, R)，檔案則請命名為 Lab3_SR_Latch_gatelevel.v。

According to the logic diagram shown in Figure 1, please write the Verilog

circuit module in gate-level modeling. Assume that the delay of an NOR gate is 2ns. The circuit module and port list should be named as Lab3_SR_Latch_gatelevel(output Q, NQ, input S, R), and its file should be named as Lab3_SR_Latch_gatelevel.v.

ii. 請撰寫此SR-Latch 之測試電路模組，必須包含下述指定之六組測資。請將此測試電路模組命名為 t_Lab3_SR_Latch_gatelevel，檔案則命名為 t_Lab3_SR_Latch_gatelevel.v。

Please write the testbench of the SR-Latch in which six test data shown in the following table must be included. The testbench module should be named as t_Lab3_SR_Latch_gatelevel, and its file should be named as t_Lab3_SR_Latch_gatelevel.v.

Time (ns)	S	R
0	1	0
10	0	0
20	0	1
30	0	0
40	0	0
50	1	1
60	0	0

B. Negative Edge Trigger D-Flip-Flop: 下圖為一正緣觸發的 D-Flip-Flop，請設計其 Verilog HDL 電路模組。

The circuit diagram of a negative-edge triggered D-Flip-Flop is shown in the following figure. Please design the Verilog circuit module for it.

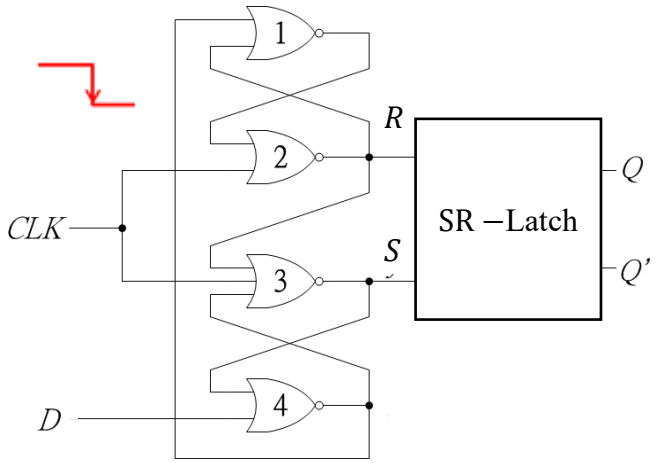


圖 2：負緣觸發的 D-Flip-Flop 電路圖

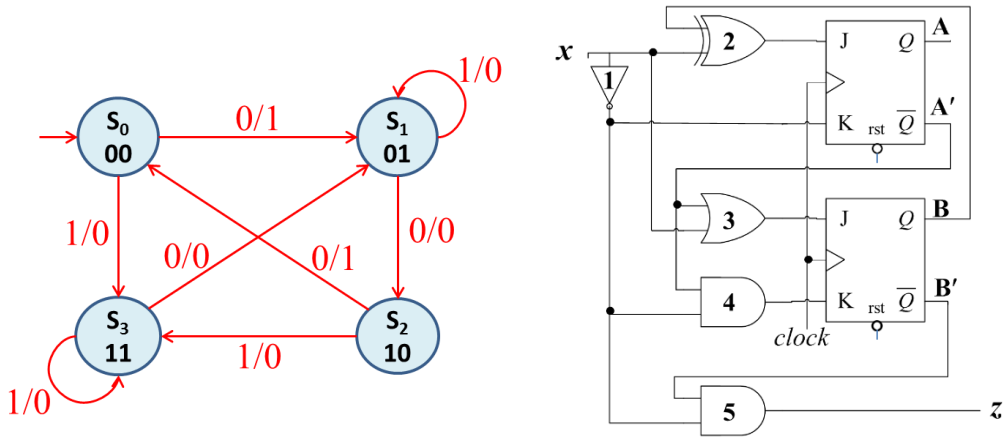
Figure 2: The circuit diagram of a negative-edge triggered D-Flip-Flop.

i. 請根據上述電路圖(圖 2)，利用 A(i)的 module，以 gate-level modeling 的方式撰寫其電路模組。假設每個 NOR gate 的 delay 為 2ns。模組名稱與 port list 請訂為 Lab3_Neg_Edge_D_FF_gatelevel(output Q, NQ, input D, clock)，檔案則請命名為 Lab3_Neg_Edge_D_FF_gatelevel.v。
According to the logic diagram shown in Figure 2, please write the Verilog circuit module in gate-level modeling by using the module in A(i). Assume that the delay of an NOR gate is 2ns. The circuit module and port list should be named as Lab3_Neg_Edge_D_FF_gatelevel(output Q, NQ, input D, clock), and its file should be named as Lab3_Neg_Edge_D_FF_gatelevel.v.

ii. 請撰寫此 D-flip-flop 之測試電路模組，clock 之週期為 20 ns (10 ns 為 HIGH、10 ns 為 LOW)，且至少必須包含下述指定之五組測資。請將此測試電路模組命名為 t_Lab3_Neg_Edge_D_FF_gatelevel，檔案則命名為 t_Lab3_Neg_Edge_D_FF_gatelevel.v。
Please write the testbench of the D-flip-flop in which five test data shown in the following table must be included. The period of the clock is 20 ns, HIGH for 10 ns and then LOW for 10 ns. The testbench should be named as t_Lab3_Neg_Edge_D_FF_gatelevel, and its file should be named as t_Lab3_Neg_Edge_D_FF_gatelevel.v.

Time(ns)	D
0	0
15	1
35	0
65	1
88	0
125	1
130	0

C. Mealy-Type Synchronous Sequential Circuit: 設計一個 Mealy-type 的同步順序電路，圖 3 為其狀態圖(state diagram)與電路圖。
Design a Mealy-type synchronous sequential circuit of which the state diagram and circuit diagram are shown in Figure 3.



(a) (b)

圖 3：Mealy-type 同步順序電路之 (a)狀態圖 與 (b)電路圖

Figure 3: The (a) state diagram and (b) circuit diagram of a Mealy-type synchronous sequential circuit.

i. 請根據此電路之狀態圖(圖 3a)，以 State-diagram-based model 方式撰寫其 Verilog HDL 電路模組。假設此電路圖有 reset 輸入訊號，此 reset 訊號為 Active LOW，可設定電路至初始狀態 S_0(00)。模組名稱與 port list 請訂為 Lab3_Mealy_state_diagram (output z, input x, clock, reset)，檔案則請命名為 Lab3_Mealy _state_diagram.v。

According to the state diagram shown in Figure 3(a), write the Verilog circuit module for this synchronous sequential circuit by state-diagram-based model. Assume that this circuit has an active-LOW *reset* signal which may reset the circuit to its initial state S_0 (00). The circuit module and port list should be named as Lab3_Mealy_state_diagram (output z, input x, clock, reset), and its file should be named as Lab3_Mealy_state_diagram.v.

ii. 請根據此電路之電路圖(圖 3b)，以 Structural model 方式撰寫其 Verilog HDL 電路模組。假設此電路圖有 reset 輸入訊號，可設定電路至初始狀態 S_0 (00)。模組名稱與 port list 請訂為 Lab3_Mealy_structural (output z, input x, clock, reset)，檔案則請命名為 Lab3_Mealy_structural.v。請注意，此電路模組中需要用到有 asynchronous reset 之 JK flip-flop 的電路模組，可自行撰寫或使用課本上之模組，檔案請命名為 JK_ff_AR.v。假設此 *reset* 訊號為 Active-LOW。

According to the circuit diagram shown in Figure 3(b), write the Verilog circuit module for this synchronous sequential circuit by structural model. Assume that the circuit can be reset to its initial state S_0 (00) by input signal *reset*. The circuit module and port list should be named as Lab3_Mealy_structural (output z, input x, clock, reset), and its file should be named as Lab3_Mealy_structural.v . Note that this circuit module requires to

instantiate the circuit module of a JK flip-flop with asynchronous reset. You may design the JK flip-flop module by yourself or apply the module provided in the textbook. The file of the JK flip-flop should be named as JK_ff_AR.v . Assume that the *reset* signal is active-LOW.

iii. 請撰寫一測試模組來完整測試上述兩個電路模組。請將此測試模組命名為 t_Lab3_Mealy，檔案則請命名為 t_Lab3_Mealy.v。
Please write a testbench to test the two circuit modules designed above thoroughly. The testbench module should be named as t_Lab3_Mealy, and its file should be named as t_Lab3_Mealy.v .

*** 注意事項 ：**

- 請用 ModelSim Student Edition 10.4a 做為開發環境。
  Develop your lab in ModelSim Student Edition 10.4.a.
- 請務必依照上述各項目之規定命名模組及檔案。
  Be sure to name the modules and files as described above.
- 禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。
  Any assignment work by fraud will get a zero point.
- 助教會以其他測資去測試上述作業。
  TA will use similar testbench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

3. 作業及 HDL 模組繳交(Hand in)

A. 作業報告繳交：word 檔，命名為 Lab3_學號_姓名

包含下列項目：

Hand in a word file, named Lab3_StudentID_Name, including the following items:

(1) 2A 之模擬結果波形圖，並說明其模擬結果波形圖是否正確。(20%)
Give the waveform of the simulation results in 2A, and explain whether it is correct or not.

(2) 2B 之模擬結果波形圖，並說明其模擬結果波形圖是否正確。(20%)
Give the waveform of the simulation results in 2B, and explain whether it is correct or not.

(3) 2C 之模擬結果波形圖，並說明其 testbench 如何設計、針對 input stimulus 預期之狀態轉換與輸出值為何、及 i.和 ii.兩種電路模組之模擬結果波形圖是否正確。(50%)
Give the waveform of the simulation results in 2C, explain how you design your testbench, show the state transitions and outputs for the input stimuli, and determine whether the circuit modules of i. and ii. designed by you are correct or not.

(4) 心得與感想、及遭遇到的問題或困難 (10%)

Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab.

B. Verilog modules 檔案繳交：8 files

Hand in the following Verilog modules: 8 files

Lab3_SR_Latch_gatelevel.v、
t_Lab3_SR_Latch_gatelevel.v、
Lab3_Neg_Edge_D_FF_gatelevel.v、
t_Lab3_Neg_Edge_D_FF_gatelevel.v、
Lab3_Mealy_state_diagram 、
Lab3_Mealy_structural.v、
JK_ff_AR.v、
t_Lab3_Mealy.v

4. DEADLINE

- 本實驗單元為一人一組， 作業請上傳至 E3 平台。
  This lab unit is one student per group. Please upload your Lab Report (word file) and the corresponding HDL code (.v files) onto e-Campus platform.
- **作業繳交截止日期為 2018/6/11 (一) 23:59。不接受逾期繳交。**
  The deadline for handing in lab report and Verilog files is **2018/6/11 (Monday) 23:59. No late hand-in is allowed.**
- 請將上述作業報告及 Verilog 電路模組與測試模組檔案(.v)全部壓縮成一個 **zip 檔** (禁止上傳 rar 檔或是其他檔案格式)，並以「Lab3_學號_姓名」的方式命名，如 ： 「Lab3_0416000_王大明」。
  Please compress the word file of lab report and the Verilog circuit modules and testbench described above all into one **zip** file (rar file or other format is not accepted), and name the zip file as "Lab3_StudentID_Name" , for example, "Lab3_0416000_Kent Chang"
- 上機演示 Demo 時間暫定為 **2018/6/13 (三) 1:00PM~9:30PM**，之後會再發公告通知大家上網填寫 Demo 時間表。未繳交作業者，將不予 Demo; 有繳交作業但未 Demo 者，亦不予計分。
  The time for on-line demo is arranged at **2018/6/13 (Wed.) 1:00PM~9:30PM** tentatively, and we will send an announcement to inform you to fill the Demo schedule online. Those who have not hand-in their lab reports and Verilog files will not be able to demo their work.
- 程式碼請勿抄襲別人或讓別人抄襲，經查證後此次 lab 總分一律以 0 分計算。
  Any assignment work by fraud will get a zero point