CS 223

DIGITAL DESIGN

SECTION 5

PROJECT REPORT

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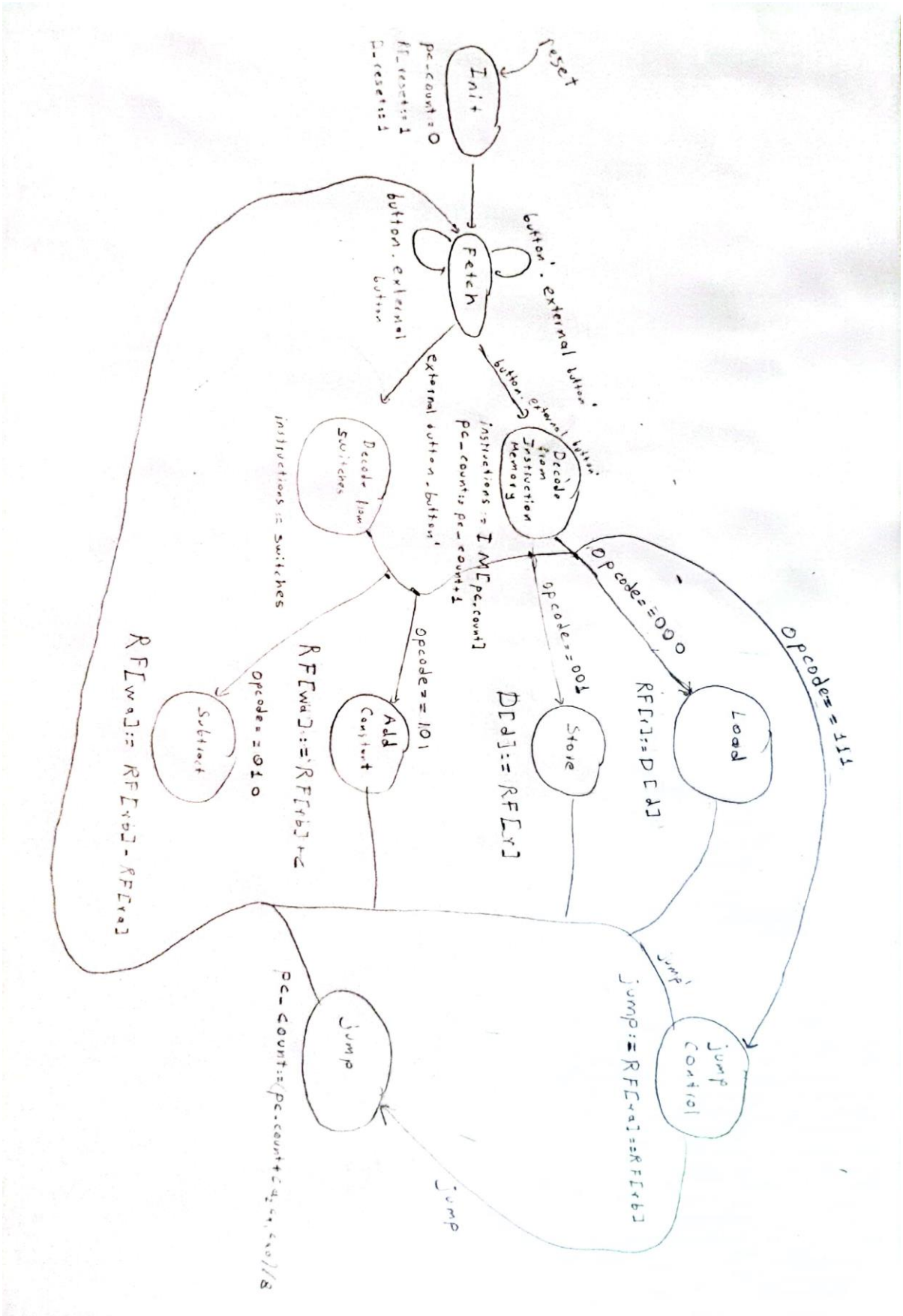
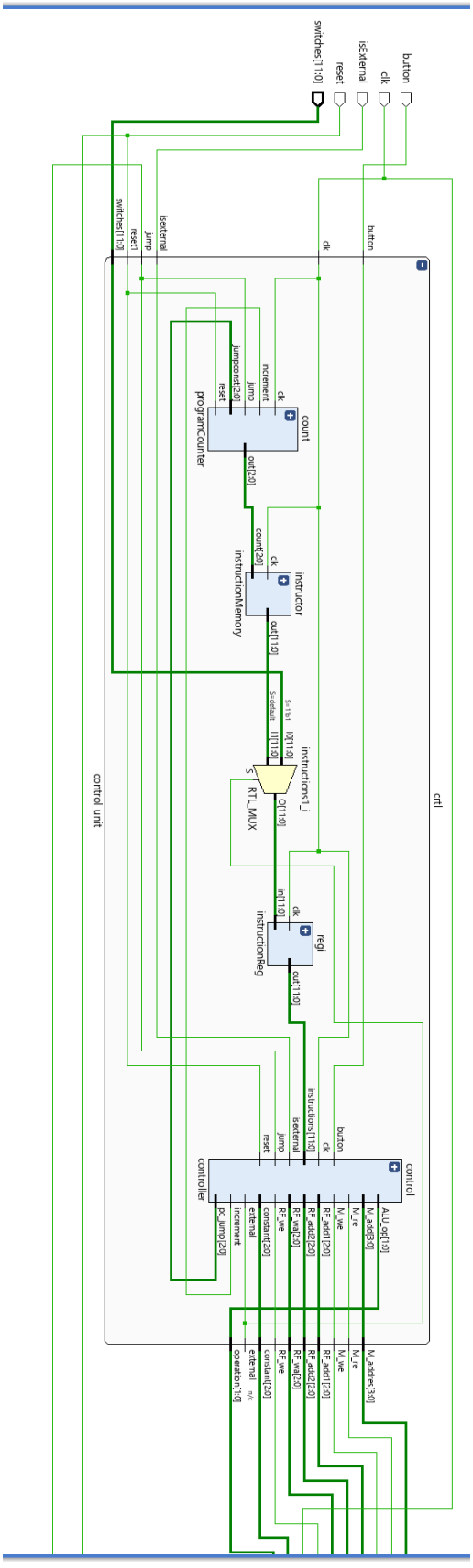
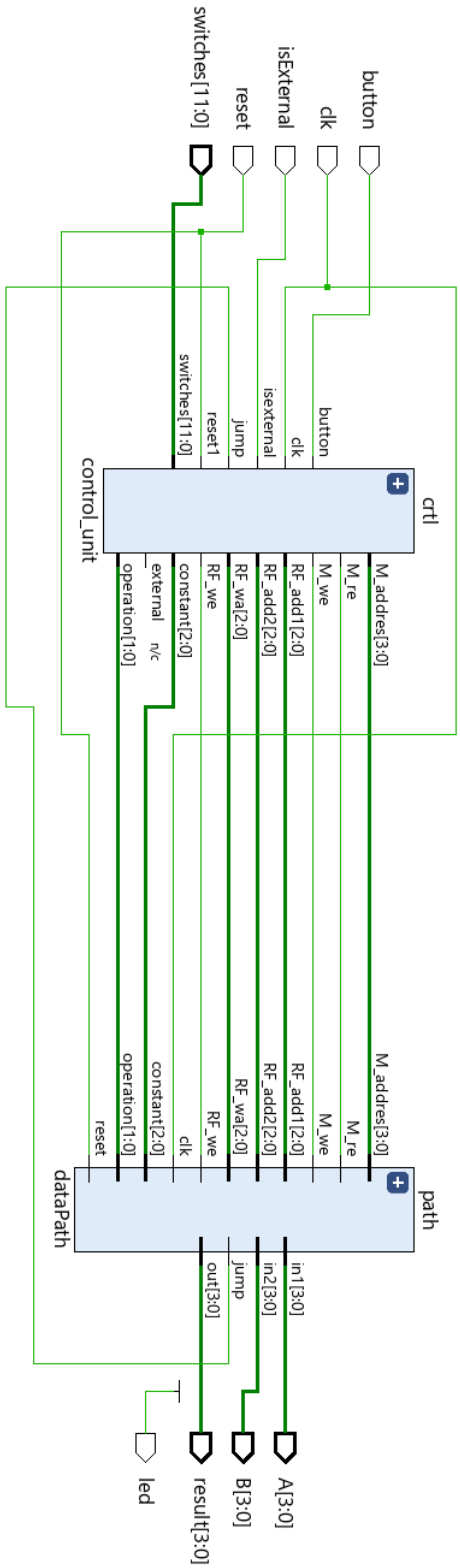
Controller High Level State Machine Diagram



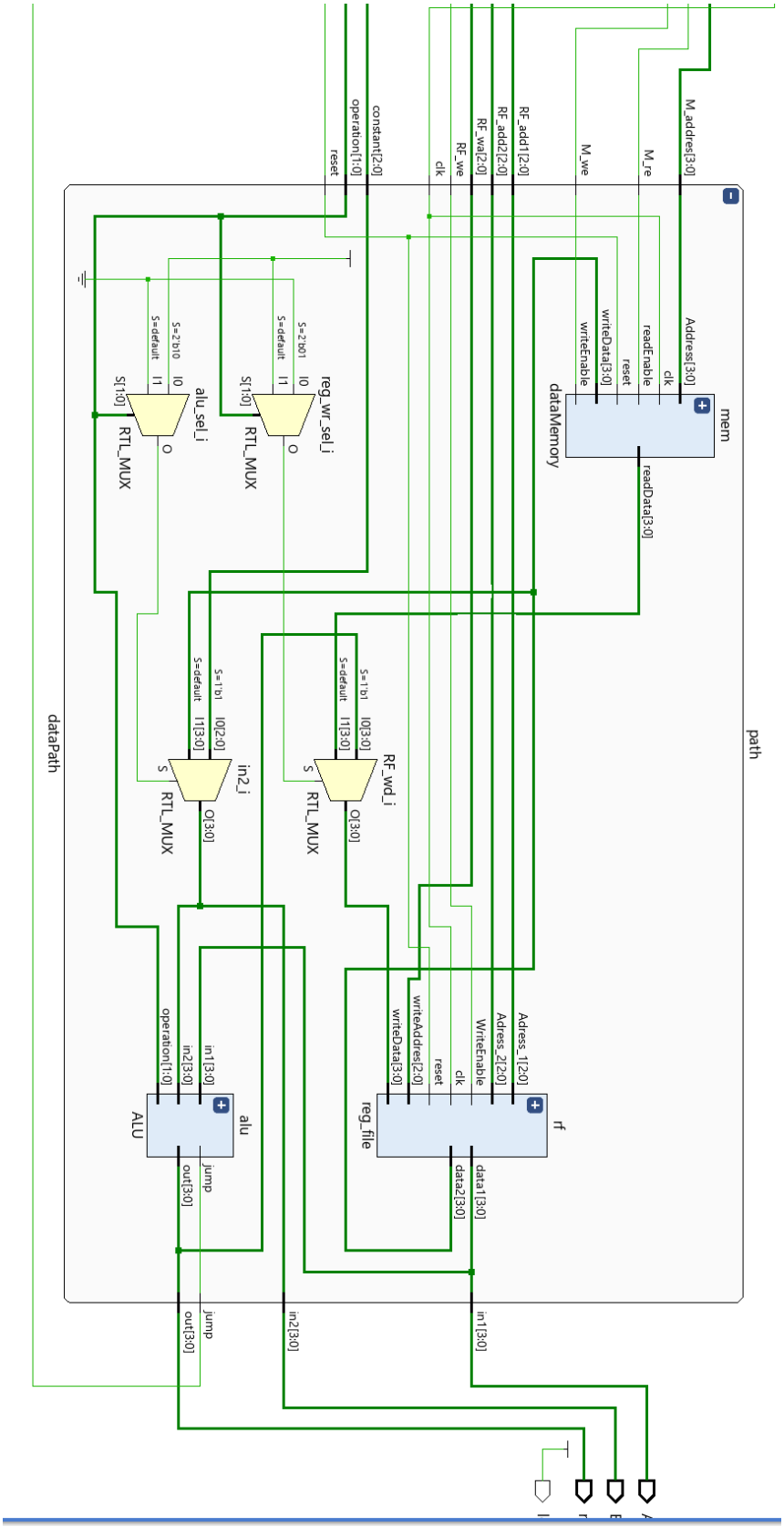
Controller Block Diagram



Top module block diagram



Datapath Block Diagram



Testbenches

```
/*module test();
    logic clk;
    logic[11:0] switches;
    logic button;
    logic isexternal;
    logic reset;
    logic[3:0] A;
    logic[3:0] B;
    logic[3:0] result;
    logic[6:0] segments;
    logic[2:0] count;
    top dut(clk, switches, button, isexternal, reset,
    //segments,count,
     A, B, result);

    initial begin
    clk = 0;#1;
    reset = 0;#1;
    clk = 1;#1;
    reset = 1;#1;
    clk = 0;#1;
    clk = 1;#1;
    isexternal = 0;#1
    clk = 0;#1;
    clk = 1;#1;
    reset = 0; #1;
    clk = 0;#1;
    clk = 1;#1;
    clk = 0;#1;
    clk = 1;#1;
```

```
clk = 0;#1
button = 1;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1;
reset = 0;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1
reset = 0;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1
switches = 12'b101_000_000_110;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1
button = 1;#1;
reset = 0;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1
button = 0;#1;
```

```
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1
button = 1;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1
reset = 0;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1
switches = 12'b101_001_000_010;#1
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1
button = 0;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1;
switches = 12'b101_001_000_001;#1;
button = 1;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1;
```

```
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1;
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clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
clk = 0;#1;
button = 0;#1;
clk = 1;#1;
clk = 0;#1;
clk = 1;#1;
```

```
    clk = 0;#1;
    isexternal = 1;#1;
    clk = 1;#1;
    clk = 0;#1;
    clk = 1;#1;
    clk = 0;#1;
    clk = 1;#1;
    clk = 0;#1;
    clk = 1;#1;
    clk = 0;#1;
    end
endmodule
```