Self-Project

Topic: Design of Low Noise Amplifier

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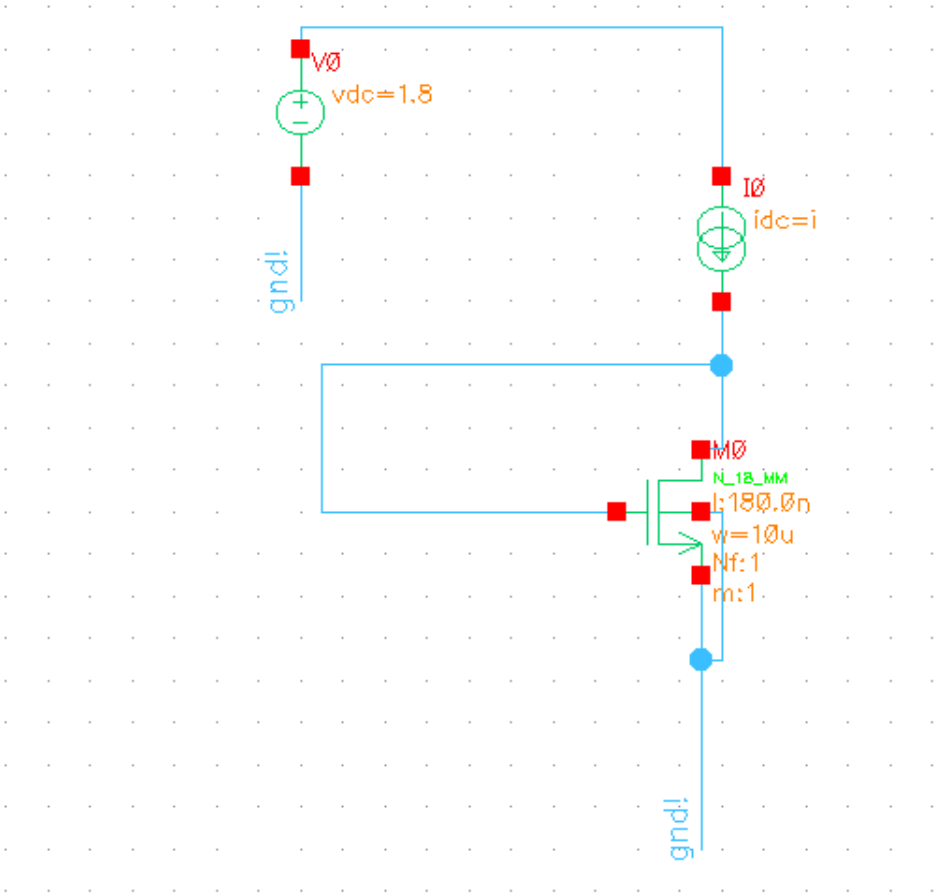
Mtech 2nd year - EE7(SSD)

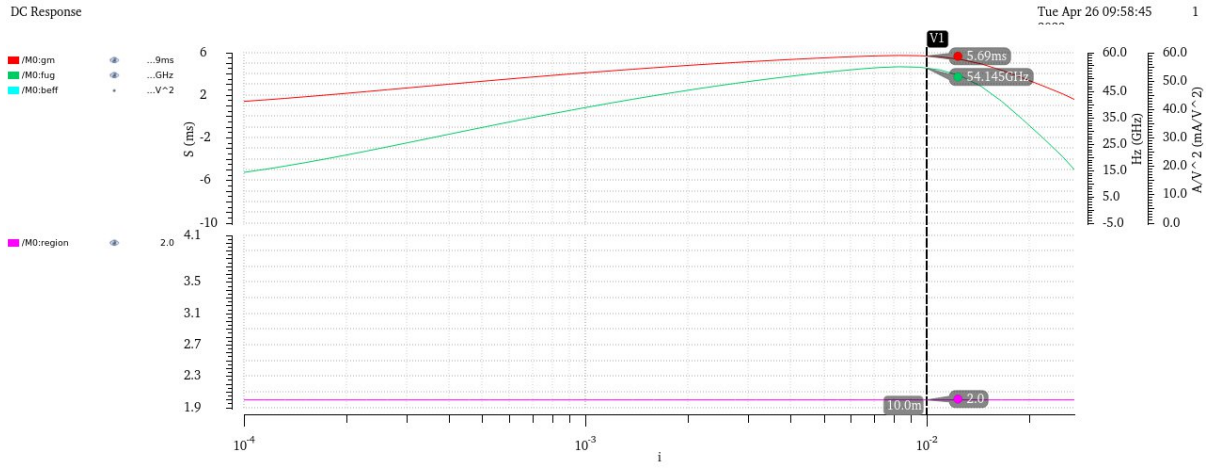
We start with the following circuit to get an estimate on gm and ugf with respect to the current.

Channel length is kept at a minimum of 180nm and width is kept arbitrarily at 10um.



The transistors drain and gate are shorted to keep transistor in saturation

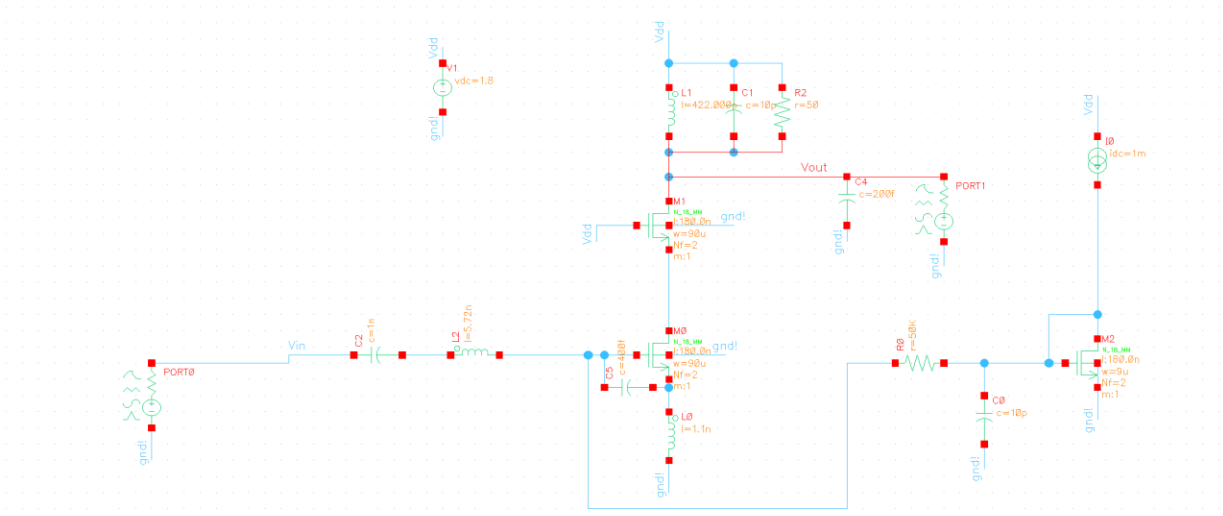
We vary id from 0.1mA to 100mA as shown by the spectre state below and get the following results



as annotated in the graph we get a maximum of gm = 5.7mS and fugf = 54 GHz at id = 10 mA.

this will be used as a reference value for further iterations.

Now we go into the main LNA circuit along with its bias circuitry as shown below



Here M0 forms the input transistor, M1 acts as a cascode device to improve gain and provides isolation, M2 is the biasing transistor carrying a current of 1mA. The Gate of M2 is connected to the gate of M0 through a RC circuit which provides DC bias while keeping ac isolated.

the values of these R0 and C0 is kept arbitrarily high to achieve good performance.

L0 is connected to source of M0 to provide inductive degeneration. C5 is connected in parallel to Cgs of M0 to reduce the fugf of M0 without increasing its channel length.

L2 is connected at the gate of M0 to give proper matching of input impedance to 50ohms.

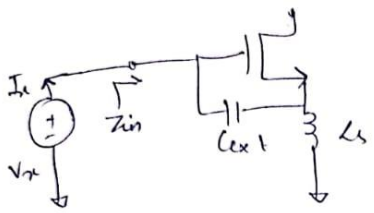
C2 is placed just after input port so that it block any dc current to flow from the bias circuit into port0.

Port0 is the input port while port1 is the output port.

L1, C1 are connected in parallel to provide resonance at frequency of operation while R2 is connected in parallel to provide an output resistance of 50ohms.

We now delve into the design iterations.

ignoring C_{gd}, we calculate the input impedance of the following circuit.



I_x flows through C_{ext} to generate

$V_{gs} = I_x \cdot \frac{1}{sC_{ext}}$

this V_{gs} generates a current $g_m V_{gs}$. $\therefore$ current through L_s is $g_m V_{gs} + I_x$.

$\therefore$ applying KVL in loop

$$\Rightarrow V_x = I_x \cdot \frac{1}{sC_{ext}} + \left(I_x + g_m \cdot \frac{I_x}{sC_{ext}}\right) sL_s$$

$$\Rightarrow \frac{V_x}{I_x} = \frac{1}{sC_{ext}} + sL_s + g_m \frac{L_s}{C_{ext}}$$

C_{ext} also includes C_{gs}

$$\therefore \boxed{Z_{in} = \frac{1}{sC_{ext}} + sL_s + g_m \frac{L_s}{C_{ext}}}$$

If $C_{ext} \gg C_{gs}$, $\therefore Re\{Z_{in}\} = g_m \frac{L_s}{C_{gs}}$

We know that $\frac{g_m}{C_{gs}} = \omega_T = 2\pi f_{ugf}$ of the transistor

$$\therefore \boxed{Re\{Z_{in}\} \sim \omega_T L_s}$$

At frequency of operation; $Im\{Z_{in}\} = 0$

$$\therefore j\omega_0 L_s = \frac{j}{\omega_0 C_{ext}} \Rightarrow \omega_0^2 = \frac{1}{L_s C_{ext}}$$

If we connect an external inductor "L_g" to match the input impedance

we get

$$Z_{in} = \frac{g_m L_s}{C_{gs1} + C_{ext}} + s(L_s + L_g) + \frac{1}{s(C_{gs1} + C_{ext})}$$

Taking $Re\{Z_{in}\} = 50\,\Omega$
$Im\{Z_{in}\} = 0\,\Omega$

we get

$$\frac{g_m L_s}{C_{gs1} + C_{ext}} = 50 \quad ; \quad \omega_0^2 = \frac{1}{(L_s + L_g)(C_{gs1} + C_{ext})}$$

We need, gain = $A_v = g_m R_D \geq 15\,dB \sim 6\ V/V$

For output impedance to be matched to 50 Ω, we keep

$R_D = 50\,\Omega$.

$\therefore g_m \sim \frac{6}{50} \simeq 120\,mS$

$\therefore$ $g_m \simeq 120\,mS$

Let $L_s = 0.25\,nH$

For $Re\{Z_{in}\} = 50\,\Omega \Rightarrow \frac{g_m L_s}{C_{gs} + C_{ext}} = 50 \Rightarrow C_{gs} + C_{ext} = \frac{120m \times 0.25n}{50}$

$\Rightarrow$ $C_{gs} + C_{ext} = 600\,fF$

From simulations, we find that for $\frac{10\mu m}{180nm}$, $C_{gs} = 11\,fF$

$\therefore C_{ext} \sim 590\,fF$

Also, $\omega_0^2 = \frac{1}{(L_s + L_g)(C_{gs} + C_{ext})} \Rightarrow L_g = \frac{1}{600\times10^9 \times 10^{-15} \times (2.4\times10^9)^2 \times 4\pi^2} - 0.25$ (3)

$\Rightarrow L_g = 7.32 - 0.25 = 7.079\,nH \sim 7\,nH$

$\therefore \boxed{L_g = 7\,nH}$

From the graph that we plotted above; we see for a $\frac{10\mu m}{180nm}$ device, maximum g_m & f_{ugf} occurs for $i_d = 10mA$.

So we take $i_d = 10mA$; assuming $V_{dsat} = 300mV$

& we know $K_n' = 234\,\frac{\mu A}{V^2}$

$\therefore (W/L)_{LNA} = \frac{2 \times I_{LNA}}{K_n' V_{dsat}^2} = \frac{2\times10m}{0.234m \times (0.3)^2} = 949$

We round off this value to 1000

$\therefore (W/L)_{LNA} = 1000$ & $L = 180nm \therefore W = 180\mu m$

For the size of cascode device, we can keep it identical to the input transistor

$\therefore (W/L)_{Cascode} = 180\mu m / 180\,nm.$

At the output port: for resonance at 2.4 GHz, we need $L_d C_d = 1/\omega_0^2 = \left(\frac{1}{2\pi f}\right)^2 = \left(\frac{1}{2\pi \times 2.4\times10^9}\right)^2$

Let's take $C_d = 200fF$; then $L_d = 21.98\,nH \Rightarrow L_g \sim 22nH$ this is a very huge value.

So Let's take $C_d = 10pF$; then $L_d = 0.439\,nH \Rightarrow$

$\boxed{L_d = 0.44nH = 440pH}$

On-chip inductors can have a maximum value of around 1nH.
So we can change value of C_d to get a low value of L_d. (4)

$L_d = 422pH$; $C_d = 10pF$ | seems satisfactory

For biasing circuit, we take bias current = 1mA

I as biasing current needed = 10mA

$\therefore (W/L)_{Bias} = \frac{1}{10}(W/L)_{LNA} = \frac{1}{10} \cdot \frac{180\mu}{180n} = \frac{18\mu m}{180nm}$

$\therefore (W/L)_{Bias} = \frac{18\mu m}{180nm}$.

These values seems rather absurd but provides us a good starting point to start with the simulations.

After simulating with these poor values , the resonant frequency comes to be about 0.3 GHz. This is due to poor input and output matching .

To match the input and output impedances to 50ohms, we will run parametric sweep in cadence to get highly accurate results.

Real part of Zin depends on Ls and Cext, whereas Imaginary part of Zin depends on Ls, Lg and Cext. We dont have much independence to vary Ls as they are very hard to fabricate and generally are limited to less than 1 nH on chips. External inductors can be large. Also, changing Cgs would mean changing transistor sizes which would mess with the bias current and gm value

So, in the input side we first vary Cext to get Real part of Zin to be 50 ohms, and then we vary Lg which is an external inductor to get Imaginary part of Zin to be 0 ohms.

At the output side to get output impedance to be 50 ohms, we keep R to be 50 ohms, and vary Cd so that its impedance gets cancelled with that of Ld at frequency of operation.

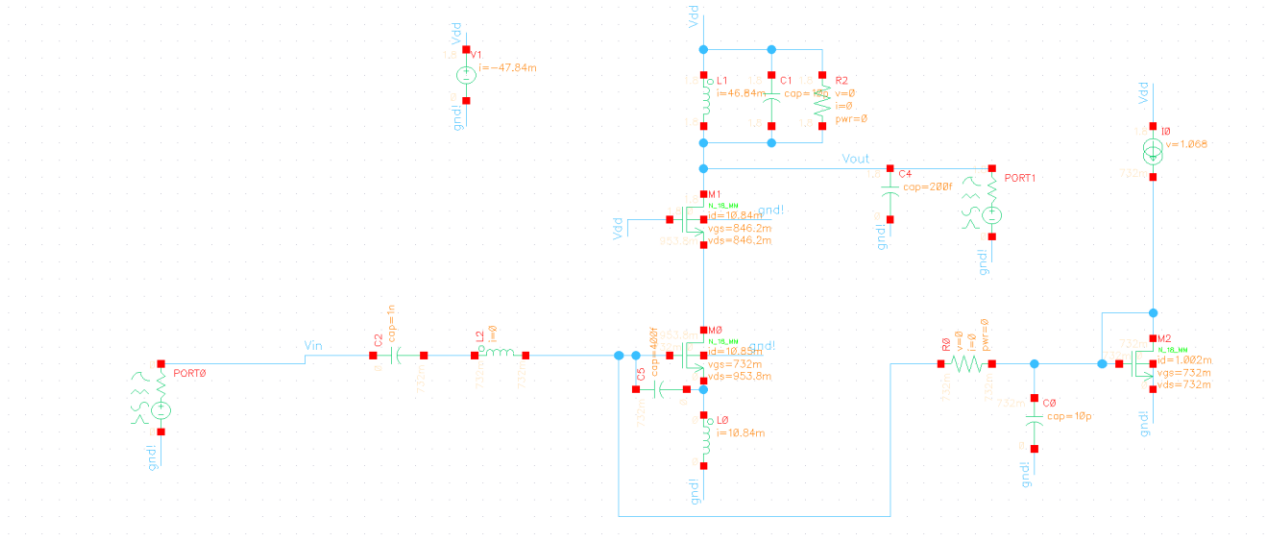
running parametric sweep would provide us the following values,

Lg = 5.72nH, Ls = 1.1 nH, Cext = 400 fF, Ld = 422 pH

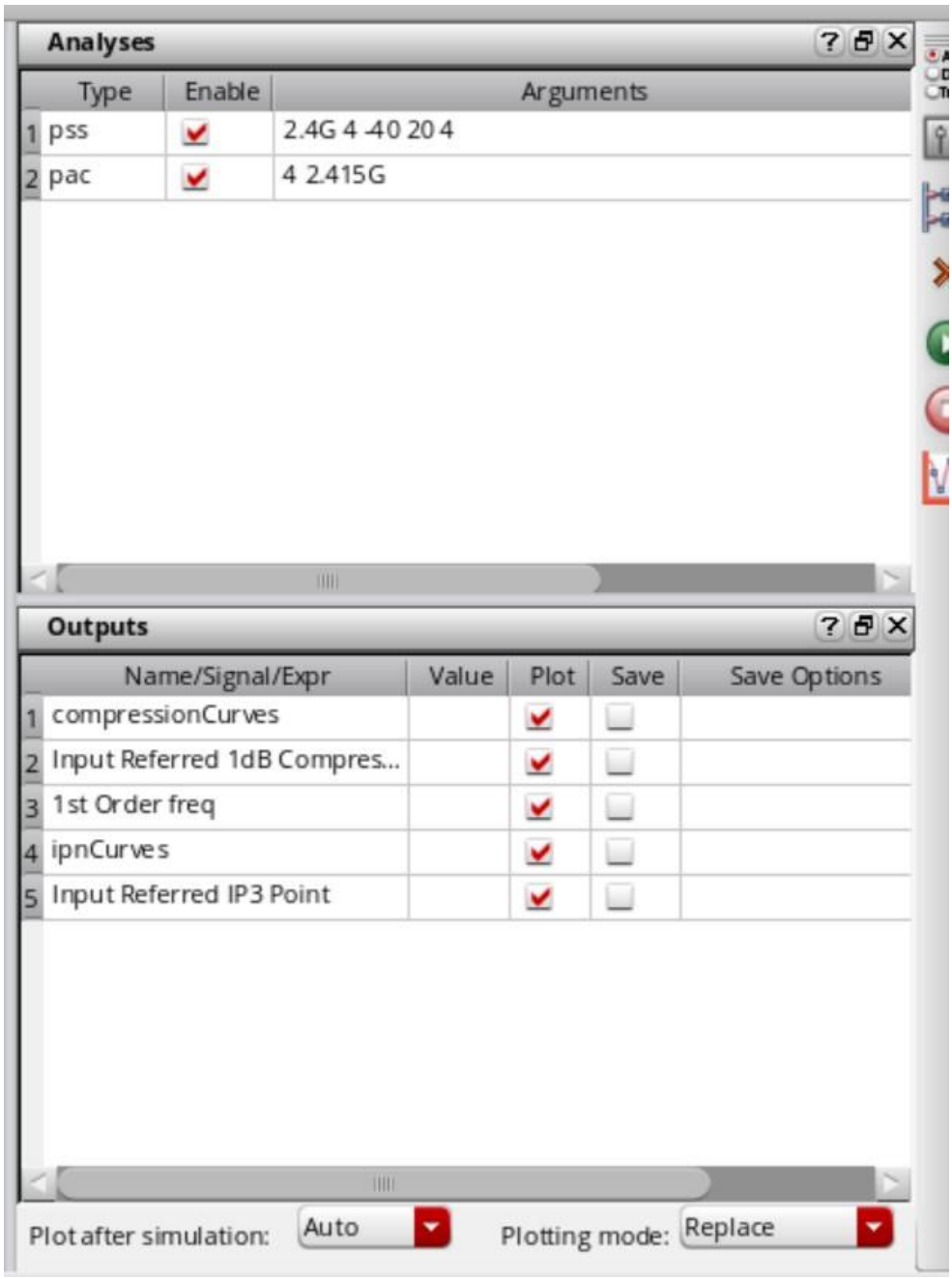
now we perform simulation on these values

Lg	5.72 nH	(W/L)lna	180u/180n
Ls	1.1 nH	(W/L)cascode	180u/180n
Cext	400fF	(W/L)bias	18u/180n
Ld	422 pH		

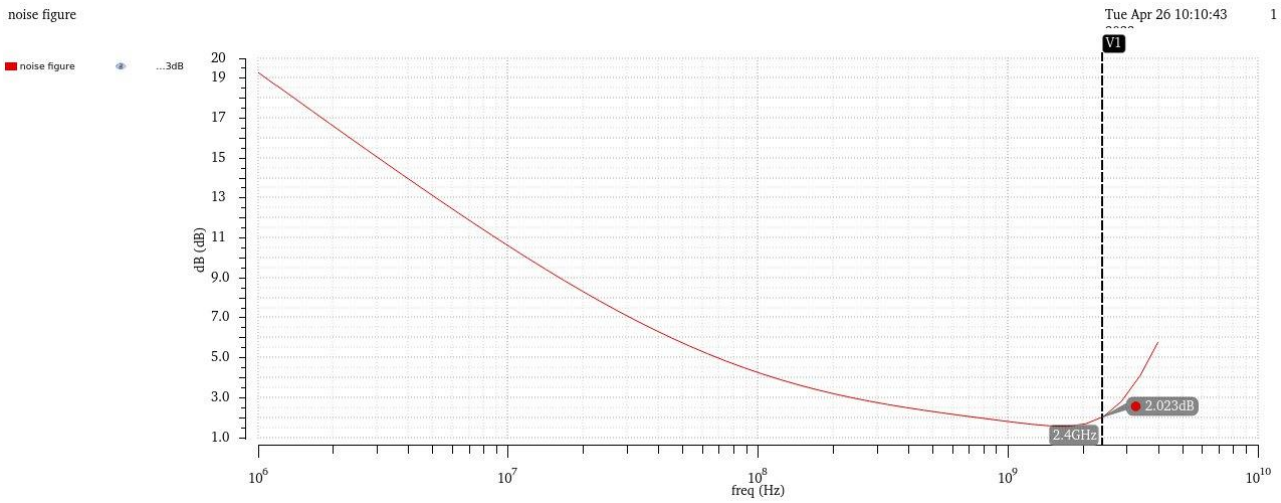
We first perform dc analysis and see the currents and gm values

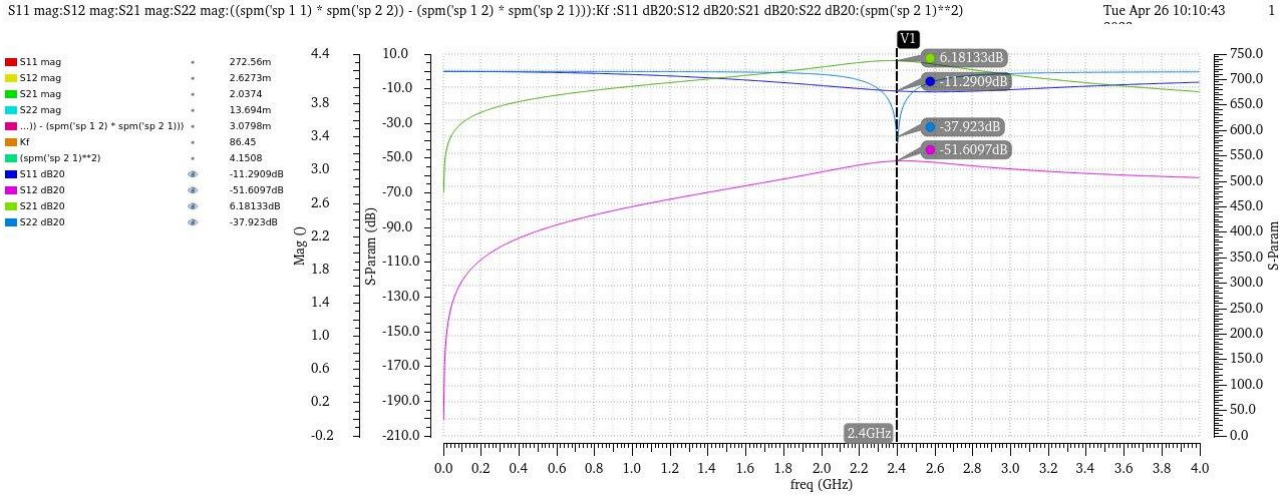


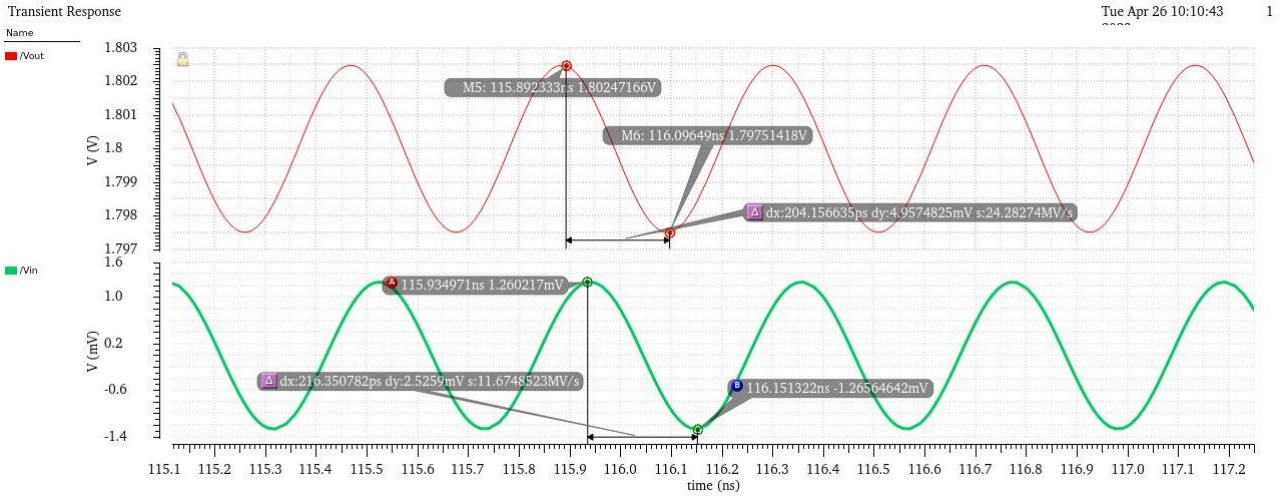
Now we run various analyses to get S parameters, noise figure, voltage gain with the following state

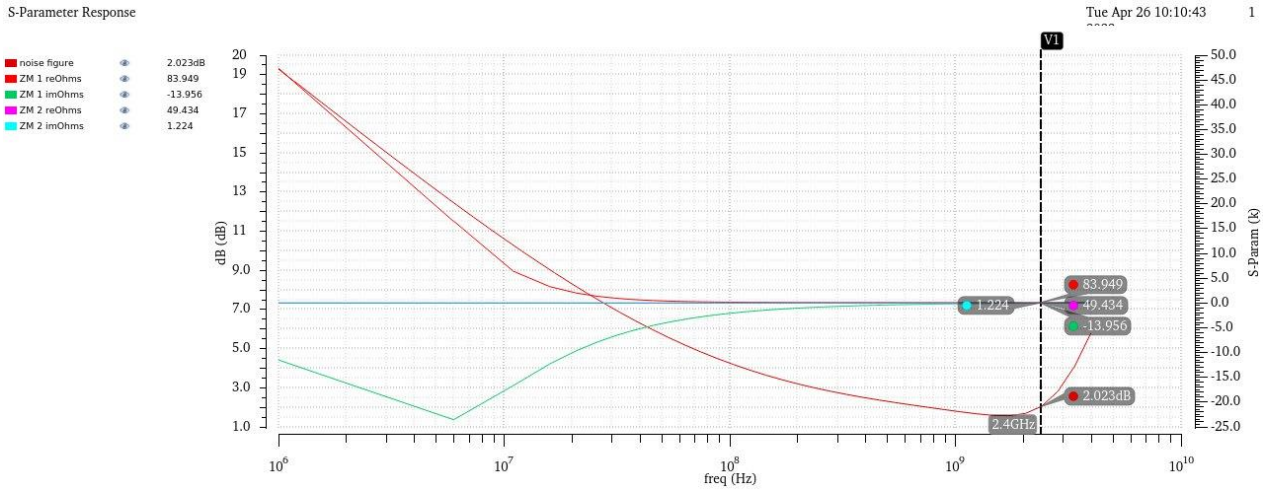


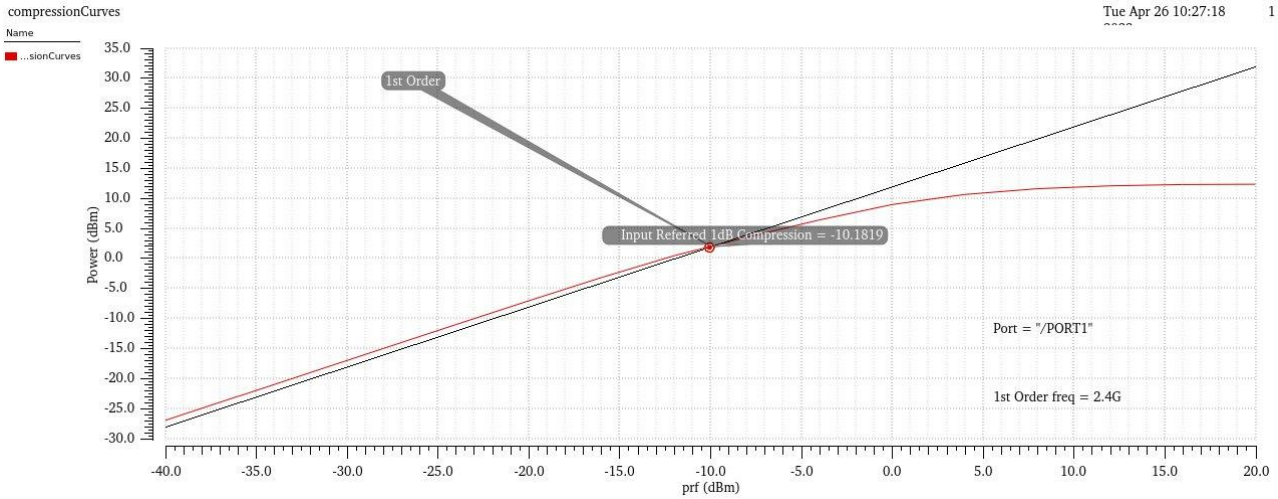
The results are plotted as shown below

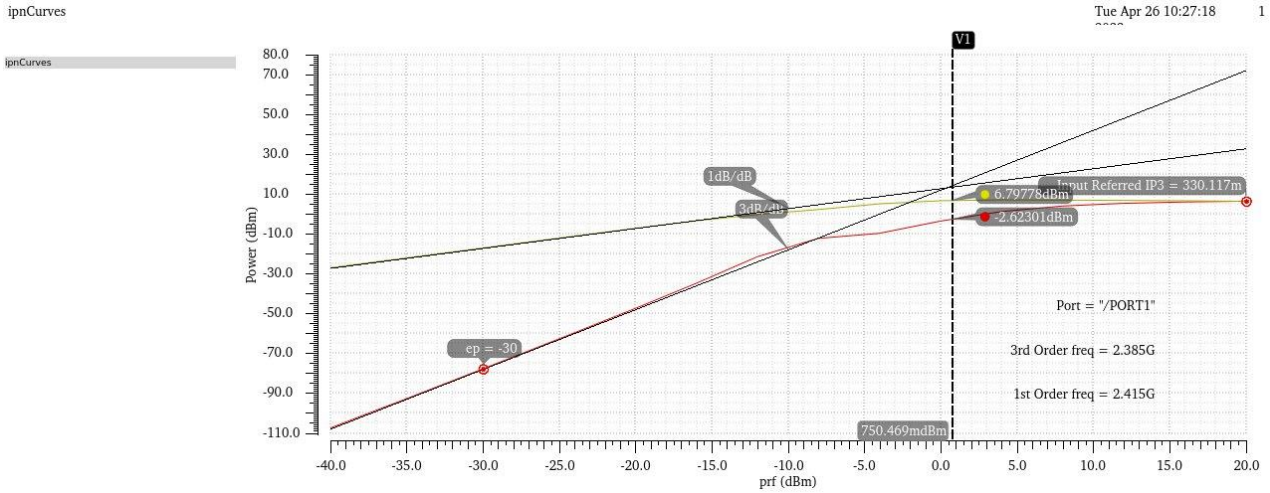

noise figure
Tue Apr 26 10:10:43
1
noise figure
...3dB
V1
dB (dB)
freq (Hz)
2.023dB
2.4GHz


S11 mag:S12 mag:S21 mag:S22 mag:((spm('sp 1 1) * spm('sp 2 2)) - (spm('sp 1 2) * spm('sp 2 1))):Kf :S11 dB20:S12 dB20:S21 dB20:S22 dB20:(spm('sp 2 1)**2)
Tue Apr 26 10:10:43
1
S11 mag 272.56m
S12 mag 2.6273m
S21 mag 2.0374
S22 mag 13.694m
...)) - (spm('sp 1 2) * spm('sp 2 1))) 3.0798m
Kf 86.45
(spm('sp 2 1)**2) 4.1508
S11 dB20 -11.2909dB
S12 dB20 -51.6097dB
S21 dB20 6.18133dB
S22 dB20 -37.923dB
V1
6.18133dB
-11.2909dB
-37.923dB
-51.6097dB
Mag ()
S-Param (dB)
S-Param
freq (GHz)
2.4GHz


Transient Response
Tue Apr 26 10:10:43
1
Name
/Vout
/Vin
M5: 115.892333ns 1.80247166V
M6: 116.09649ns 1.79751418V
dx:204.156635ps dy:4.9574825mV s:24.28274MV/s
115.934971ns 1.260217mV
dx:216.350782ps dy:2.5259mV s:11.6748523MV/s
116.151322ns -1.26564642mV
V (V)
V (mV)
time (ns)







From the above graphs, we get the following specifications

Noise Figure	2.02 dB	Kf	86.45
S11	-11.29 dB	Vpp input swing	2.5mV
S12	-51.6 dB	Vpp output swing	5mV
S21	6.18 dB	IIP3	750 mdB
S22	-37.923 dB	ZM1	84 - j13.956
delta	3m	ZM2	49.434 + j 1.224 ohms

We see that input is not properly matched, and the gain is only 6 dB which is equivalent to 2 V/V. (note that input and output voltage swings peak to peak are 2.5mV and 5 mV).

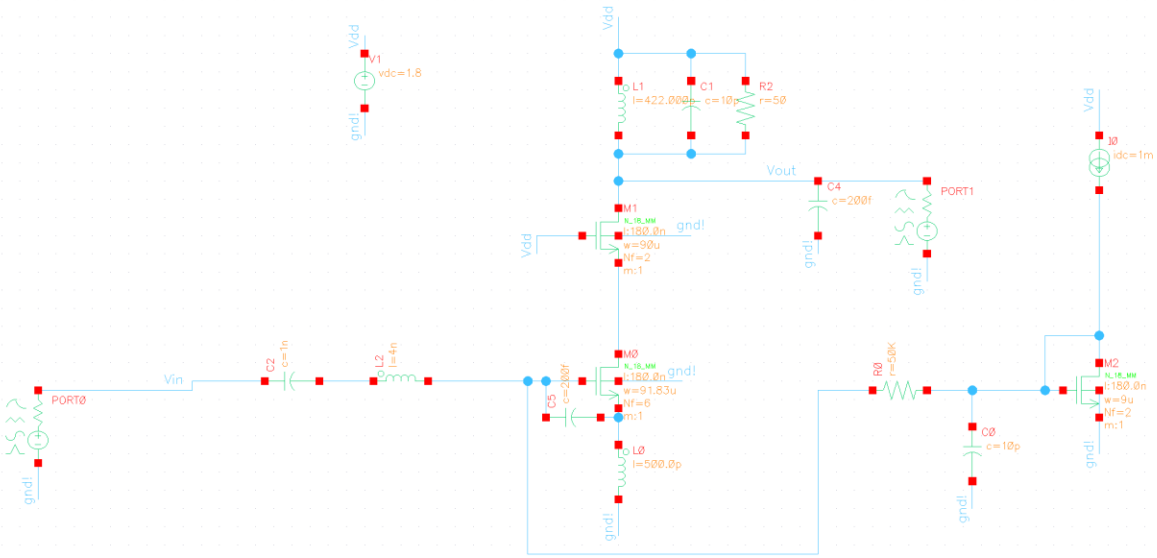
However as Kf > 1 and delta < 1, we say that this LNA if stable at all frequencies, thus it is unconditionally stable.

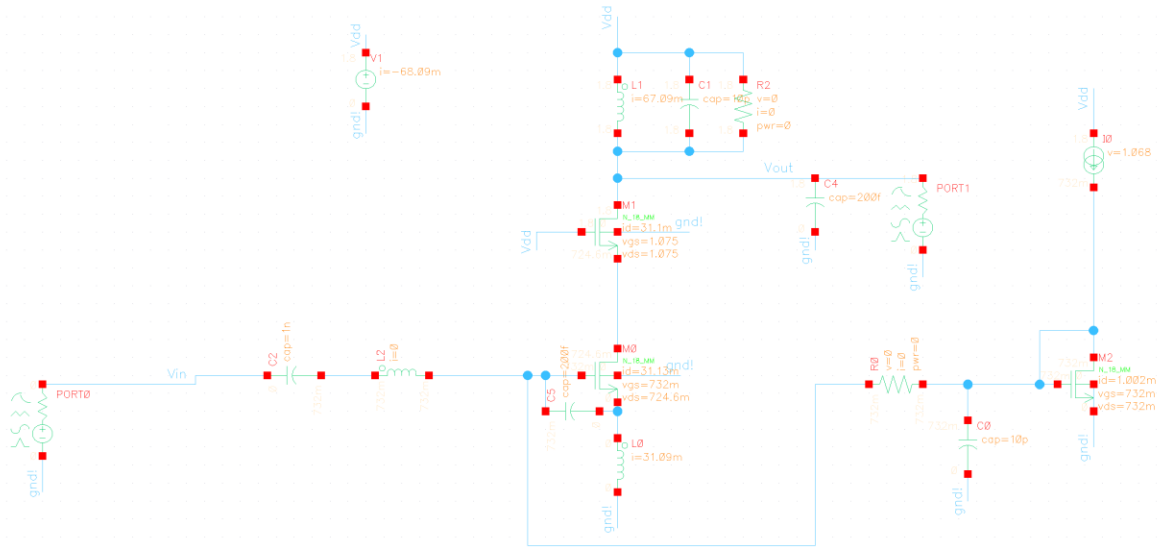
To increase gain we have to increase gm of the input transistor. This can be achieved by increasing W/L and Id of the input transistor. So, we increase W of the transistor to 551 uM. We can use fingers to (=6) to reduce the disproportionate size of the transistors. This would change the Cgs of the transistor and thus would require another parametric sweep to match the topology's input impedance.

after successfull iterations we simulate with the following values

Lg	4 nH	(W/L)lna	551u/180n
Ls	500 pH	(W/L)cascode	180u/180n
Cext	200fF	(W/L)bias	18u/180n
Ld	422 pH		

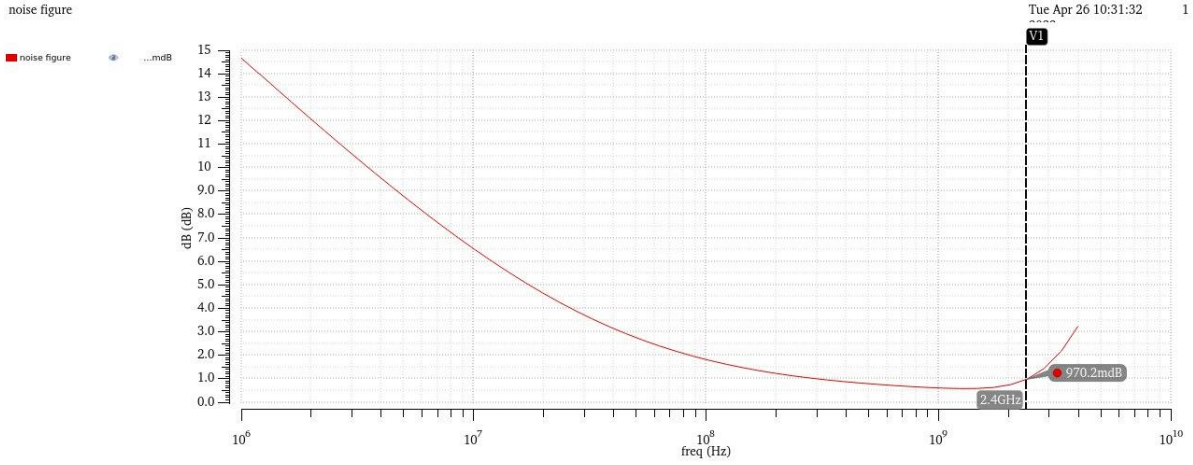
we run dc analysis on this circuit and note that current has now increased to 31 mA

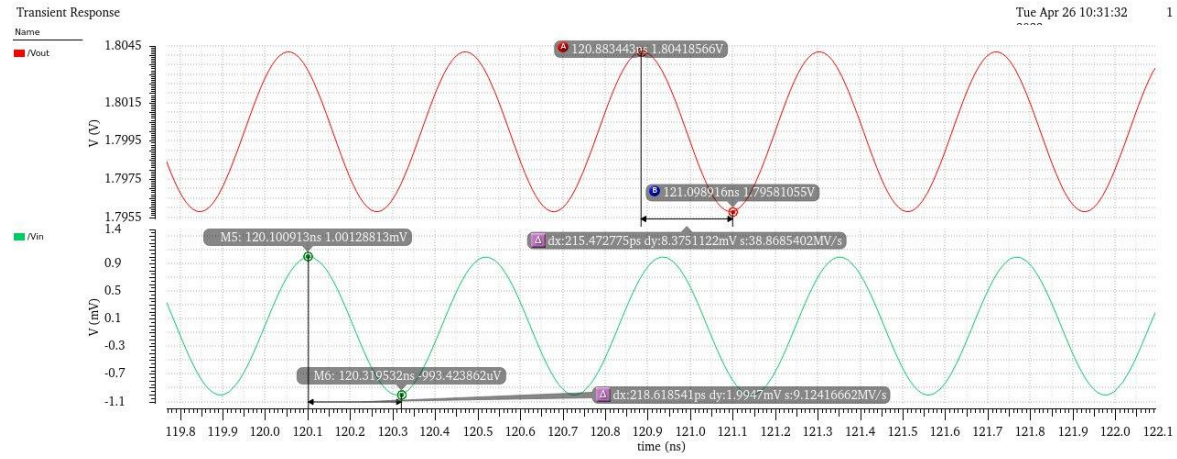

Vdd
V1
vdc=1.8
gnd!
L1
l=422.0Øp
C1
c=1Øp
R2
r=5Ø
Vout
C4
c=2ØØf
PORT1
1Ø
idc=1m
M1
N_18_MM
l=18Ø.Øn
w=9Øu
Nf=2
m:1
Vin
C2
c=1n
L2
l=4n
PORTØ
MØ
w=91.83u
CØ
c=1Øp
RØ
r=58K
M2
w=9u
LØ
l=5ØØ.Øp

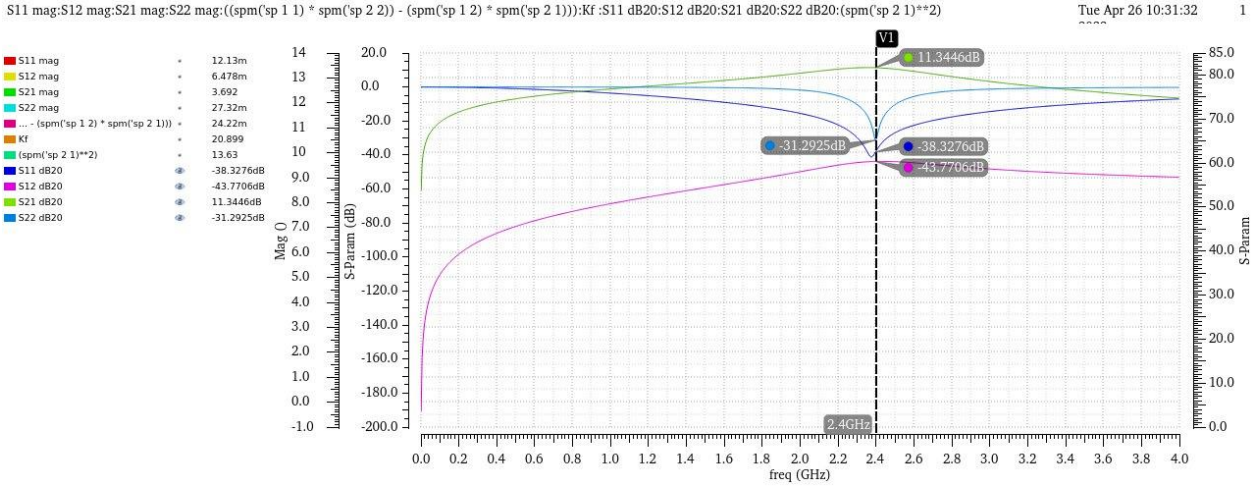

Vdd
V1
i=-68.09m
gnd!
L1
i=67.09m
C1
R2
v=Ø
i=Ø
pwr=Ø
Vout
C4
cap=2ØØf
PORT1
1Ø
v=1.Ø68
M1
id=31.1m
vgs=1.Ø75
vds=1.Ø75
Vin
C2
cap=1n
L2
i=Ø
PORTØ
MØ
id=31.13m
vgs=732m
vds=724.6m
CØ
cap=1Øp
RØ
v=Ø
i=Ø
pwr=Ø
M2
id=1.ØØ2m
vgs=732m
vds=732m
LØ
i=31.09m

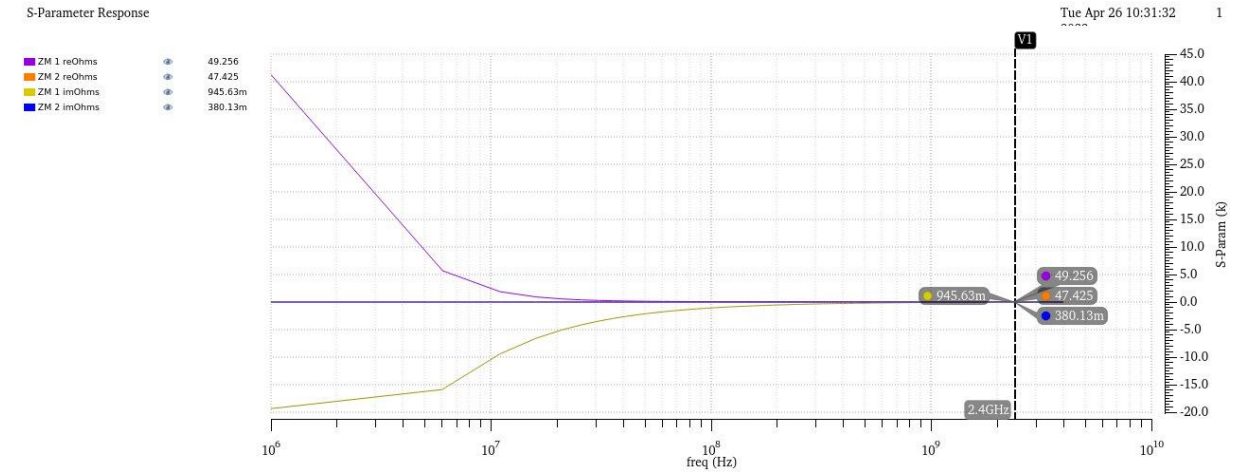
fug	33.01G
gbd	0
gbs	823.3p
gds	9.627m
gm	191.2m

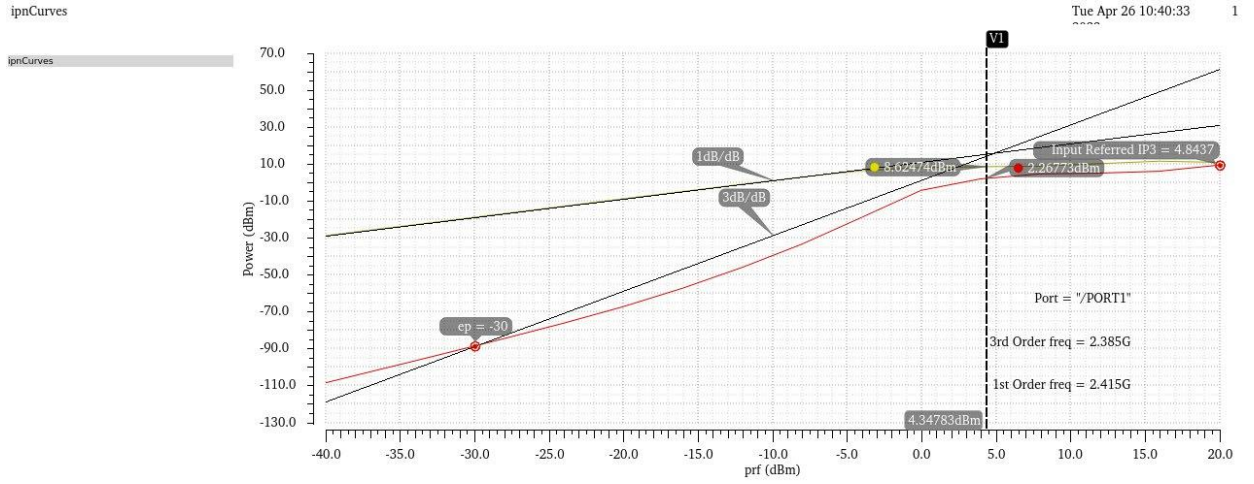
we run different analyses now as shown in the spectre state

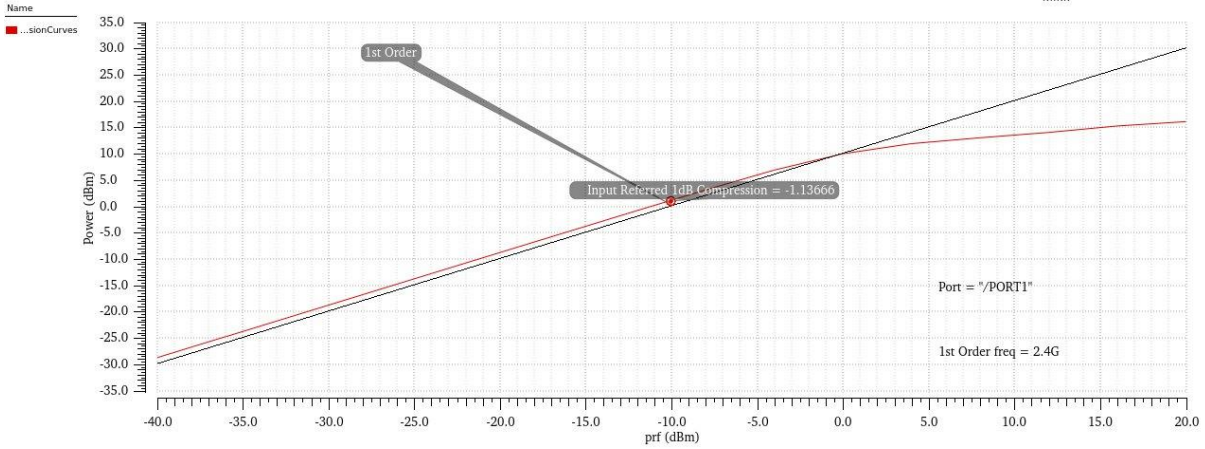





S11 mag:S12 mag:S21 mag:S22 mag:((spm('sp 1 1) * spm('sp 2 2)) - (spm('sp 1 2) * spm('sp 2 1))):Kf :S11 dB20:S12 dB20:S21 dB20:S22 dB20:(spm('sp 2 1)**2)
Tue Apr 26 10:31:32
1
S11 mag 12.13m
S12 mag 6.478m
S21 mag 3.692
S22 mag 27.32m
... - (spm('sp 1 2) * spm('sp 2 1))) 24.22m
Kf 20.899
(spm('sp 2 1)**2) 13.63
S11 dB20 -38.3276dB
S12 dB20 -43.7706dB
S21 dB20 11.3446dB
S22 dB20 -31.2925dB
V1
11.3446dB
-31.2925dB
-38.3276dB
-43.7706dB
2.4GHz
Mag ()
S-Param (dB)
S-Param
freq (GHz)


S-Parameter Response
Tue Apr 26 10:31:32
1
ZM 1 reOhms 49.256
ZM 2 reOhms 47.425
ZM 1 imOhms 945.63m
ZM 2 imOhms 380.13m
V1
49.256
47.425
945.63m
380.13m
2.4GHz
S-Param (k)
freq (Hz)


ipnCurves
Tue Apr 26 10:40:33
1
ipnCurves
V1
1dB/dB
3dB/dB
8.62474dBm
2.26773dBm
Input Referred IP3 = 4.8437
ep = -30
Port = "/PORT1"
3rd Order freq = 2.385G
1st Order freq = 2.415G
4.34783dBm
Power (dBm)
prf (dBm)


Name
...sionCurves
1st Order
Input Referred 1dB Compression = -1.13666
Port = "/PORT1"
1st Order freq = 2.4G
Power (dBm)
prf (dBm)
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
-35.0
-40.0
-35.0
-30.0
-25.0
-20.0
-15.0
-10.0
-5.0
0.0
5.0
10.0
15.0
20.0

We see a lot of improvement in the specifications but at the expense of more power dissipation and larger transistors

The 2nd iteration's component values and resulting specifications are tabulated as below

Noise Figure	970 mdB	Kf	20.899
S11	-38.32 dB	Vpp input swing	2 mV
S12	-43.77 dB	Vpp output swing	58.3 mV
S21	11.34 dB	IIP3	4.34 mdB
S22	-31.3 dB	ZM1	49.256 - j0.95 ohms
delta	3m	ZM2	47.425 + j0.38 ohms

Kf>1 and delta <1 indicates that the LNA is unconditionally stable.

Gain has increased from 6 dB to 11 dB but still falls short by 4 dB for the required gain of 15 dB

All the rest of S parameters meet the specifications.

Input and output impedances are matched to 50 ohms

Noise figure also improved from 2.02 dB to 970 mdB.

IIP3 also improved from 750 mdB to 4.34 mdB