A 255nW Ultra-High Input Impedance Analog Front-End for Non-contact ECG Monitoring

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***Abstract* — This paper presents a high-input impedance analog front-end (AFE) for low-power bio-potential acquisition. In order to boost input impedance, parasitic capacitance from PCB, pad, and amplifier gate input were cancelled using shielding buffer and positive feedback. To maximize the amount of positive feedback while guaranteeing stability, a self-calibration scheme is proposed for the positive feedback. A prototype IC fabricated in 0.18μm CMOS consumes 255nW from 0.8V supply. Measured input impedance with the proposed calibration is 50GΩ at 50Hz which is equivalent to an input capacitance of 60fF. It is also verified that the proposed scheme is resilient to supply and temperature variations and applicable to non-contact ECG monitoring.**

***Keywords* — High input impedance, positive feedback calibration, low-power bio-potential, non-contact ECG.**

I. INTRODUCTION

In wearable bio-potential acquisition systems, dry-electrode is preferred over wet-electrode for long-term comfortable measurement as it does not dry out, and can ultimately be used for non-contact measurement. However, it is difficult to obtain accurate measurement using dry-electrodes since the contact impedance between the skin and the electrode is very large and varies significantly in the presence of motion. In order to overcome this issue, the input impedance seen from the contact must be made as large as possible.

The input impedance of an AFE is determined by two parts; one is the off-chip parasitic capacitance from the PCB trace and the other is the on-chip capacitance from pad, ESD, and gates of the input amplifier. There have been several approaches to increase the input impedance by canceling the on-chip or the off-chip parasitic capacitance. In [1-3], a positive feedback is used to cancel the input capacitance of the amplifier. However, these works use a weak positive feedback that only cancels the input capacitance of the amplifier and does not cancel parasitic capacitance from the pad or ESD. In [4,5], active shielding technique was introduced to reduce the off-chip parasitic capacitance. However, it cannot cancel the on-chip parasitic capacitances. While previous approaches show improved input impedance, none of the previous work cancels both the on-chip and off-chip capacitance and thus their impedance is limited to below 7GΩ at 50Hz.

In this work, we propose an AFE achieving 60fF input capacitance which results in an impedance of 50GΩ at 50Hz by cancelling all parasitic capacitance using a foreground self-calibrated positive feedback and shield buffer amplifier that is robust to temperature and supply variations.

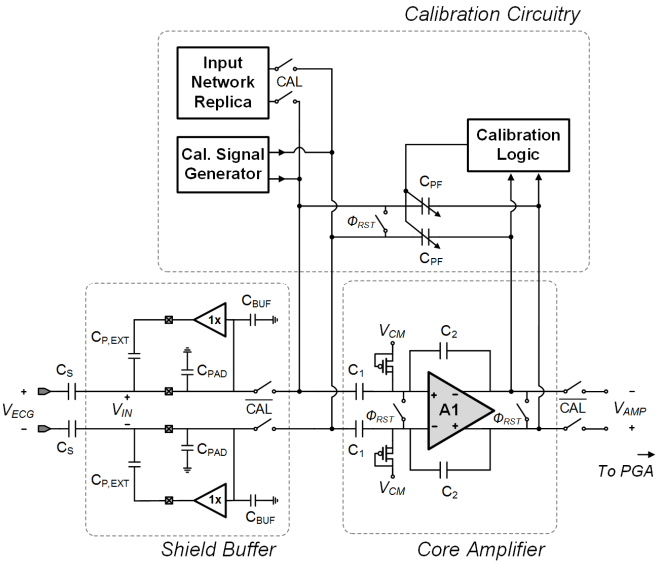

Fig. 1. Overall Architecture of the proposed high input impedance AFE.

II. ANALOG FRONT END DESIGN

Fig. 1 shows the overall architecture of the proposed AFE. It is composed of three parts; shield buffers, input amplifier and calibration circuitry. To reduce the off-chip parasitic capacitance ($C_{P,EXT}$) whose value is tens of pF, differential input signal (V_{IN}) is shielded by two active buffers, which reduce the capacitance by the open-loop gain of the amplifier inside the unity gain buffer [4,5]. The input amplifier is a capacitive feedback amplifier with an embedded shunt feedback DC servo loop (DSL) for offset removal. A diode-connected MOS pseudo-resistor is used at the input of the opamp A1, to provide DC bias without lowering the input impedance. In order to cancel the on-chip capacitance, C_{PAD}, C_{BUF} and C_1, a capacitively coupled positive feedback (C_{PF}) is added. Unlike previous works [1-3] where C_{PF} is set to be equal to C_2, which results in cancellation of only the input capacitance C_1, this work employs a programmable capacitance (C_{PF}) to cancel all on-chip parasitic capacitance while maintaining stability.

In order to determine this desired C_{PF}, an internal self-calibration is performed before bio-potential acquisition. When the calibration signal (CAL) is high, the feedback amplifier is disconnected from the input and connected to an internal calibration network which consists of calibration signal generator, calibration logic and an input network replica that has identical parasitic capacitance as the main amplifier circuit

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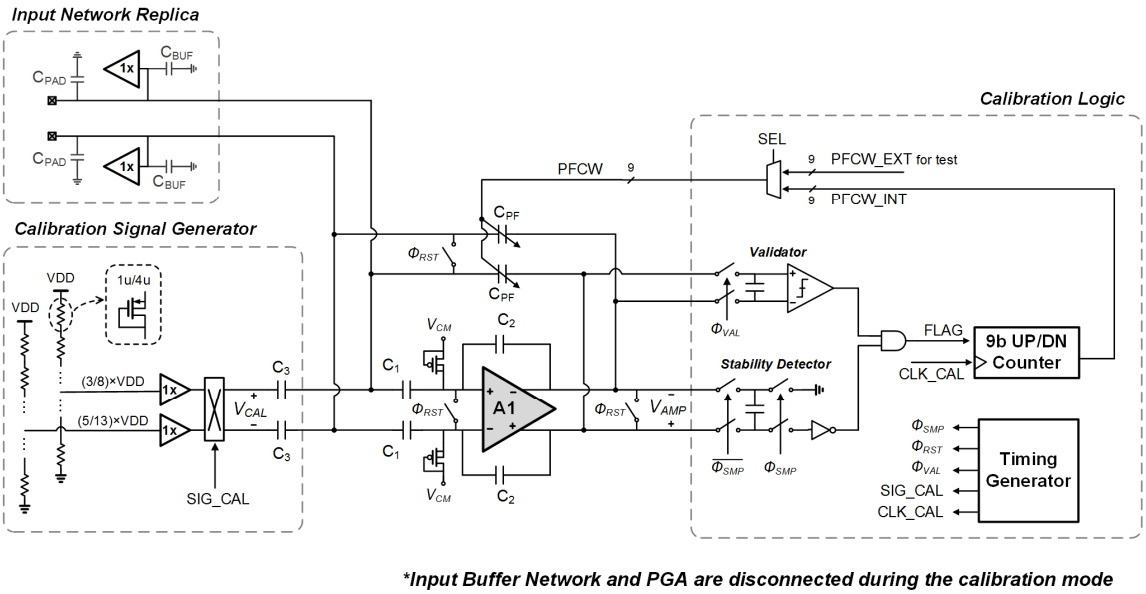

Fig. 2. Schematic during calibration mode for detecting stability limit.

during normal operation. During calibration, C_{PF} is set such that on-chip parasitic capacitance is cancelled while maintaining stability. Note that chopper-stabilized amplifier is avoided to maximize input impedance since chopper reduces the input impedance by chopper frequency [6,7]. The input stage amplifier is followed by an on-chip programmable gain amplifier (PGA).

A. Active Shield

As shown in Fig. 1, the active shield surrounds each input signal both in IC and at PCB level to suppress external parasitics. Measured parasitic capacitance of custom non-contact electrode is 30pF and it is reduced to 30fF by the open loop gain of 60dB. Note that in [4,5], shield buffer is used for not only for the external parasitic reduction but also as the low-noise input amplifier. Thus, each shield buffer consumes large amount of power of about 30μW. In this work, shield buffer was employed just to cancel external parasitic capacitance and consumes 64nW.

B. System Transfer Function Analysis

During the measurement of bio-potential signal (see Fig. 1), internal parasitic capacitances (C_{PAD}, C_{BUF}, C_1, etc.), comparable to body-electrode coupling capacitance (C_S), reduces the voltage gain from the body to the amplifier output. The transfer function can be expressed as

$$\left.\frac{V_{AMP}}{V_{ECG}}\right|_{Measure} \approx \frac{C_1}{C_2}\frac{C_S}{C_S + C_{PAD} + C_{P,INT} + C_1 + (1-C_1/C_2)C_{PF}} \quad (1)$$

where $C_{P,INT}$ is the entire internal parasitic capacitance at input excluding C_{PAD} and C_1. This gain can be equal to the ideal value of C_1/C_2 if all parasitic is cancelled, which is when the following condition is met.

$$C_{PAD} + C_{P,INT} + C_1 + (1-C_1/C_2)C_{PF} = 0 \quad (2)$$

In order to find the C_{PF} that meets this condition, a self-calibration is performed, which is described next.

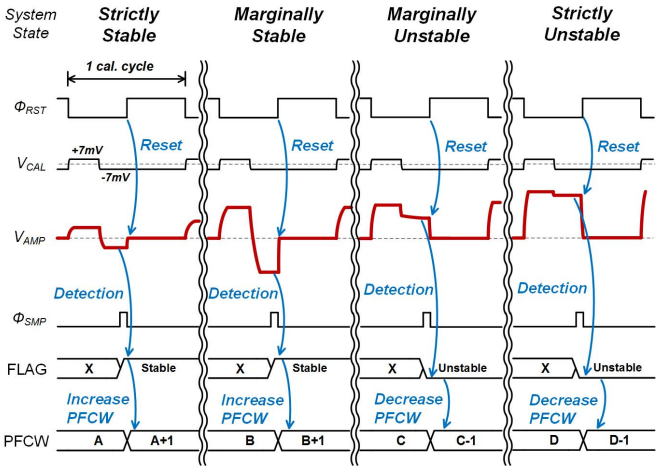

Fig. 3. Timing diagram of calibration mode and its 4 cases: strictly stable, marginally stable, marginally unstable and strictly unstable. Calibration settles at the boundary between marginally stable and marginally unstable.

C. Positive Feedback Calibration

Fig. 2 shows the proposed self-calibration scheme of the positive feedback amplifier. At the start of calibration, input signal and PGA are disconnected from the input amplifier (A1). Instead, input network replica, calibration signal generator and calibration logic are connected. The input network replica consists of pads, ESD and unity gain buffers whose parasitic capacitance match that of the main circuit during normal operation.

The calibration signal is a small-signal ($14mV_{pp}$) differential clock (V_{CAL}) that is generated by using two pseudo-resistor ladders. The system transfer function during calibration mode can be represented as:

$$\left.\frac{V_{AMP}}{V_{CAL}}\right|_{Calibration} \approx \frac{C_1}{C_2}\frac{C_3}{C_{PAD} + C_{P,INT} + C_1 + (1-C_1/C_2)C_{PF}}. \quad (3)$$

Note that AC coupling capacitor (C_3) in the calibration signal generator is included in $C_{P,INT}$.

By comparing (2) and (3), it is apparent that parasitic cancellation condition is satisfied when the denominator of the system transfer function in (3) is zero. Since the capacitance during calibration is same as the capacitance during normal operation, the proposed scheme can cancel not only the capacitance at the input of the amplifier (C_1), but also the parasitics including C_3, C_{PAD} and C_{BUF}.

D. Calibration Operation

A detailed timing diagram during calibration mode is shown in Fig. 3. When Φ_{RST} is low, the calibration signal (V_{CAL}) is applied to the amplifier, which goes up by 7mV and then down by -7mV. Depending on the system stability, the amplifier behaves differently as the calibration signal changes from 7mV to -7mV. That is, when the system is marginally or strictly stable, the system acts as an amplifier whose output is proportional to calibration input signal V_{CAL}. On the other hand, when the system is marginally or strictly unstable, the system acts as a positive feedback latch and thus the output is stuck at a high value and does not respond to the input when it goes down to -7mV. Thus, system stability can be determined by sampling the output when the input is lowered and comparing it to a threshold detector, which is implemented by a differential-to-single ended converter and an inverter.

Based on the detected system state, the 9-bit positive feedback control word (PFCW) is changed so that positive feedback becomes stronger when the system is stable and weaker when the system is unstable. Hence, the system settles at the boundary between stable and unstable state, where the parasitic cancellation condition (2) is satisfied. When calibration is finished, the PFCW is adjusted by 5 LSBs towards a more stable state to have some stability margin, to ensure that the system is stable under supply or temperature variations.

III. Measurement Results

The proposed AFE is implemented in 0.18µm CMOS and occupies 700µm×830µm area. The chip micrograph is shown in Fig. 4. Input amplifier, shield buffers, and the other peripheral circuits draw 194nA, 80nA, and 46nA from 0.8V supply, respectively. The measured differential gain is 34dB and the bandwidth is 400Hz. CMRR and PSRR are measured as 66dB and 69dB, respectively. Fig. 5 shows the input referred noise of the AFE. The integrated noise is 8.26µV_{rms} and the thermal noise density above 100Hz is 140nV/ $Hz^{1/2}$, resulting in a Noise Efficiency Factor (NEF) of 7.

Fig. 6 illustrates the input impedance and capacitance of the proposed AFE. In Fig. 6(a), the measured input capacitance is shown for various PFCW with 5m$V_{pp,diff}$ of 50Hz input signal. The capacitance value decreases as PFCW increases and is measured as +3pF at PFCW of 0 and –2pF at PFCW of 500, resulting in a capacitor resolution of 10fF. Using the proposed self-calibration technique, the PFCW settles to 311 and the AFE achieves 60fF of input capacitance. Fig. 6(b) presents the

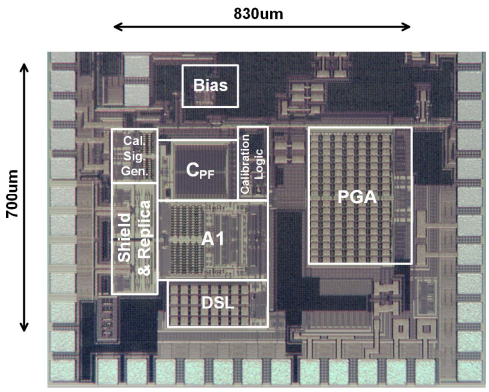

Fig. 4. Chip Micrograph

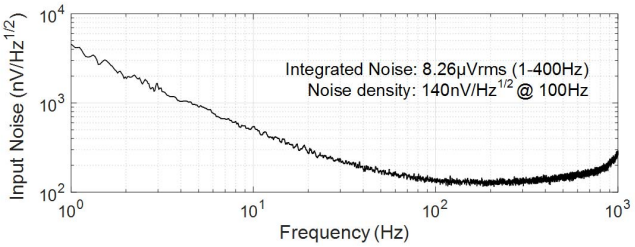

Fig. 5. Measured input-referred noise of the implemented AFE.

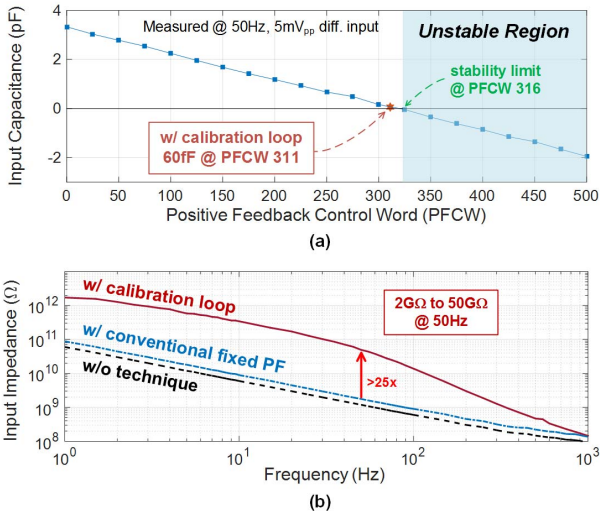

Fig. 6. Measured input impedance characteristic (a) input capacitance according to Positive Feedback Code Word (PFCW) and (b) input impedance over the frequency.

input impedance compared to conventional architectures. The conventional positive feedback technique with fixed capacitance (C_{PF}=C_2) has impedance of 2GΩ at 50Hz. After employing the proposed calibration loop, the AFE has 25 times higher impedance of 50GΩ. The performance of the proposed AFE is summarized and compared with other AFEs with high input impedance in Table I. It can be seen that the proposed work achieves the highest input impedance and lowest input capacitance.

Table I. Performance comparison

	This Work		[1] JSSC 15	[2] ISSCC 15	[3] ISSCC 16		[4] VLSI 16		[5] JETCAS 11
Process	**0.18µm**		65nm	65nm	40nm		0.18µm		0.5µm
VDD (V)	**0.8**		0.6	0.6	1.2		1.8		3.3
Power (µW)	**0.255**		0.064	0.003	4.8[a]		216[a]		31.6[a]
CMRR (dB)	**66**		55	60	-		108		-
PSRR (dB)	**69**		67	63	-		-		-
Input-Referred Noise (μV_{rms})	**8.26 (1-400Hz)**		6.52 (0.5-250Hz)	26 (1.5-370Hz)	2 (0.5-200Hz)		0.67 (0.5-100Hz)		200nV/√Hz @1Hz 45nV/√Hz @1kHz
NEF	**7.01**[b]		2.64[b]	2.1[b]	10.87[c]		28.2[c]		-
Input Impedance (Ω)	**200G @ DC**	**50G @ 50Hz**	>110M	>2G	300M @ DC	200M @ 10Hz	18G @ DC	6.7G @ 50Hz	~50TΩ || 60fF
Input Capacitance (pF)	**0.06**		28.9[d]	1.6[d]	80		0.47		0.06
Capacitance Consideration	**off-chip, PAD, coupling, amplifier**		amplifier input	amplifier input	coupling, amplifier input		off-chip, amplifier input		off-chip

[a] considered 2 channels of active electrode power consumption
[b] considered amplifier power only
[c] calculated from the given data
[d] calculated from $1/(2\pi f_{in} \cdot Z_{in})$, where f_{in} is 50Hz if it is not specified

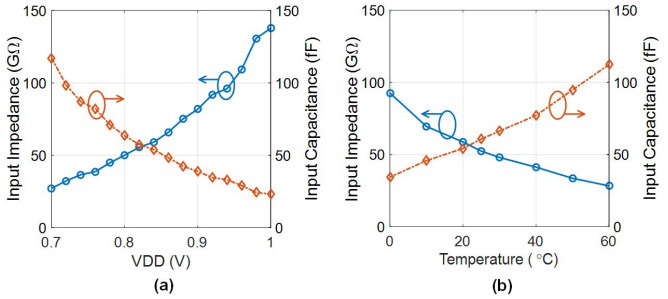

Fig. 7 Robustness of input impedance (solid) and input capacitance (dotted) under (a) supply and (b) temperature variation

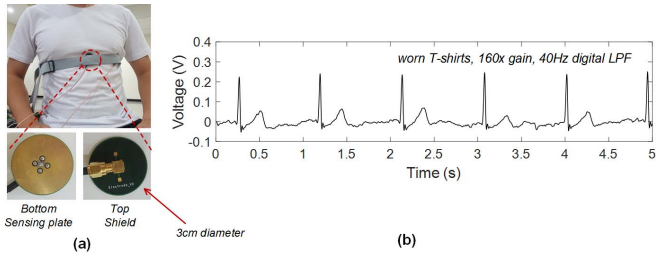

Fig. 8. (a) Measurement setup using shielded non-contact electrodes. (b) Measured ECG using non-contact electrode while worn T-shirt. Output voltage was low-pass filtered by 40Hz.

Since foreground calibration technique is susceptible to variation in the surrounding environment, the robustness of the proposed AFE is checked against supply voltage and temperature variations as shown in Fig. 8. With 0.7-0.9V supply and 0-50°C temperature change, the input impedance and capacitance do not have significant change that may cause system instability.

In order to demonstrate its usage in non-contact bio-potential acquisition, ECG was recorded using the implemented AFE and two custom electrodes as shown in Fig. 8. Two electrodes were put on the T-shirt above the chest. The measured ECG is shown in Fig. 8(b), where the output of the AFE was low-pass filtered with 40Hz cut-off frequency.

IV. Conclusion

A high input impedance AFE with self-calibrated positive feedback and shield buffer has been introduced. It achieves 50GΩ input impedance at 50Hz, which is equivalent to 60fF of input capacitance.

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