A Low-power, Wireless, Real-time, Wearable Healthcare System

Zhihong Lin, Feng Ye, Wenhui Qin, Xiaofei Cao, Yanchao Wang, Rongtao Hu, Ruijie Yan, Yajie Qin, Ting Yi, Zhiliang Hong
State Key Laboratory of ASIC & System, Fudan University, Shanghai, 201203, China
Email: zlhong@fudan.edu.cn

***Abstract*—A low-power, wireless, real-time, wearable healthcare system for monitoring bio-potential signals including ECG, EEG and EMG signal is proposed. The system consists of Analog Front End (AFE), Incremental ΣΔADC and Short Range Device (SRD) Transceiver. All the ICs are implemented in 0.35µm CMOS technology and integrated on the printed circuit board (PCB). The AFE and the Incremental ΣΔADC consume less than 100µW and can be configured to various gains, bandwidths and sampling rates for best energy efficiency when capturing different ExG signals. Lithium-battery provides power for the system. Integrating with Huahong MCU, the system is capable of restoring the ExG signals at real time on TFTLCD after wireless communication, storing the ExG information in SD card, and transferring the ExG data to PC for analyzing it in MATLAB.**

***Keywords*—Healthcare system; Low-power; Real-time; Wearable; Analog Front End; Incremental ΣΔADC; SRD Transceiver;**

I. INTRODUCTION

With the world aging, chronic diseases like heart disease and cerebrovascular disease are becoming the major causes of death around the world. Long-term continuous health monitoring is essential in detecting and treating with these diseases [1]. Compared with the big, heavy and cable-connected medical equipment in hospital, wireless wearable healthcare system has several superiorities such as compact dimensions, low weight, comfortable using and so on. It is portable for monitoring people's health.

Wearable devices are usually powered by battery. In order to extend the cell lifetime, wearable healthcare system needs to meet the strict power consumption constraint. Moreover, as ExG signals shown in Fig. 1 [1] cover wide frequency and amplitude ranges, the system should be able to detect various ExG signals under the extremely low energy budget.

Wearable healthcare system research has become a popular area now. A wireless senor node SoC for continuous real-time health monitoring was presented in [2], consuming only 700uW at 0.7V supply voltage and able to work for more than 200 hours without changing the battery. Illustrated in [3], an ultra-low power battery-less energy harvesting body sensor node (BSN) SoC is capable of acquiring, processing and transmitting ExG signals, only consuming 19uW and running solely on harvested energy. Integrating a three channels ΣΔADC, the wireless portable ECG monitoring SoC in [3] only consumes 850uW at 1V supply voltage.

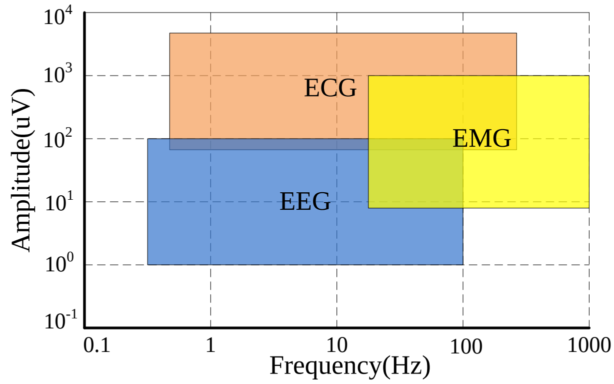

Fig. 1 Characteristics of ExG signals [1]

In this paper, an ExG signals monitoring healthcare system with several features is proposed as below:

a. Low power consumption: Power consumption of the AFE and the Incremental ΣΔADC is less than 100uW.

b. Flexible configuration: In order to achieve best trade-off between performance and power consumption when detecting different ExG signals, the AFE can be configured to different gains and bandwidths, and the Incremental ΣΔADC can be adjusted to various sampling rates. Data rate and output power of the SRD Transceiver are also programmable under different conditions.

c. Real-time and wireless monitoring: The system realizes the real-time ExG signals monitoring on TFTLCD after wireless communication. It also has the function of storing the ExG information in SD card and transferring the ExG data to PC for analyzing it in MATLAB.

The system description, core chips design and software design are presented in Section II. Section III illustrates the experimental results of monitoring human body's ECG signal at real time. Finally, a conclusion is drawn in Section IV.

II. SYSTEM DESCRIPTION

The proposed healthcare system diagram is shown in Fig. 2, composing of power management part (PM), transmitting part

(TX) and receiving part (RX). In PM part, the lithium-battery provides power for the whole system. The DC-DC Converter adjusts the supply voltage for different ICs. In TX part, the ExG signals are amplified by AFE and digitalized by ADC. Then the digital data are transmitted by the SRD Transceiver to the space. While in the RX part, the data are received by the SRD Transceiver and then restored on the TFTCLD, saved in the SD Card, or transferred to PC. As the central processor, MCU controls and configures all the ICs properly.

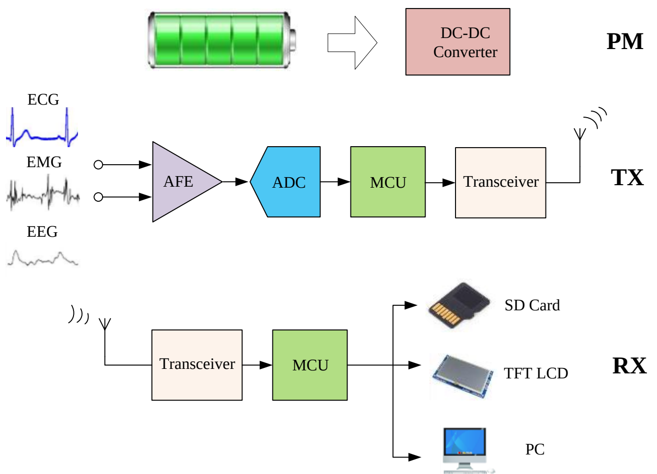

Fig. 2 Proposed healthcare system diagram

A. AFE

ExG signals are extremely weak and cover a wide frequency range, bringing a lot of challenges to AFE design. AFE needs to be ultra-low noise and have sufficient gain to amplify the ExG signals. For various signal amplitudes and frequencies, programmable AFE gain and bandwidth will be better to filter high frequency noise and interference. Besides, the CMRR of the AFE should be high enough to suppress power line interference. Achieving high impedance is also vital to avoid attenuating input signals due to the high impedance of skin-electrode.

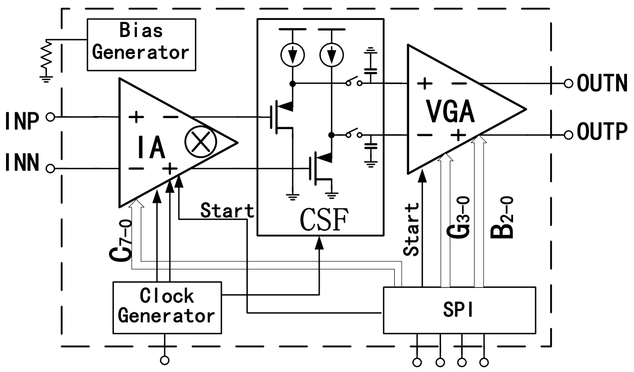

Fig. 3 Architecture of the AFE [5]

In this paper, the architecture of the AFE shown in Fig. 3 [5] has three blocks: Instrumental Amplifier (IA), Chopping Spike Filter (CSF) and Variable Gain Amplifier (VGA). IA is designed for blocking electrode DC differential offset and achieving high CMRR, high input impedance, low input referred noise and high linearity. VGA realizes programmable gain (41-79dB) and bandwidth (63Hz-1.2kHz) for three kinds of ExG signals. The AFE consumes only 3.96μA under a supply voltage of 3.3V.

B. Incremental ΣΔADC

In healthcare system, the Successive Approximation Register (SAR) ADC is usually adopted due to the low power consumption. However, when capturing some ultra-weak signals like EEG signal, AFE has to provide large gain due to the low resolution of SAR ADC. As Incremental ΣΔADC can achieve very high resolution, it will relax the AFE gain budget. Moreover, Incremental ΣΔADC can be easily multiplexed between different channels for multi-channel application.

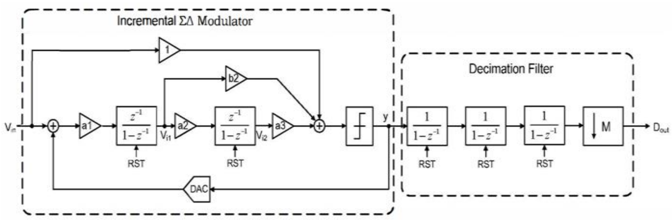

Fig. 4 Incremental ΣΔADC architecture [6]

The architecture of the proposed Incremental ΣΔADC is shown in Fig.4 [6], consisting of a second-order incremental ΣΔ modulator and a third-order cascade-of-integrators (CoI) decimation filter. The ADC consumes only 24μA current from 3.3V supply voltage. The oversampling ratio (OSR) of the ADC can be configured to 64, 128, 256 or 512 for different application. The ADC read-out data are 16 bits and the effective data are 10 bits.

C. SRD Transceiver

The transceiver proposed in this paper is a time division duplexing RF transceiver, working on the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency band typically at 434MHz and 868MHz.

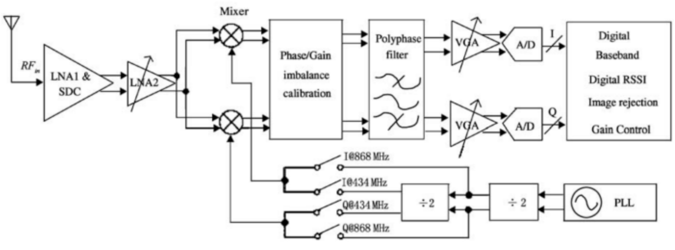

Fig. 5 SRD Receiver block diagram [7]

The SRD Receiver block diagram is shown in Fig. 5 [7]. It adopts the low-IF receiver architecture. The received RF signal is amplified by the two-stage low noise amplifier (LNA) and then down-converted to the intermediate frequency (IF) by quadrature mixer. The IF I/Q signals are filtered by poly-phase filter with phase and gain imbalance calibration and then digitized by ADCs. Automatic gain control, demodulation and bit synchronization are performed in digital baseband. OOK, FSK and GFSK modulations are optional and date rate can be configured to different value up to 153.6kBs.

The SRD Transmitter adopts the indirect VCO modulation architecture shown in Fig. 6. The synthesized RF signal is fed directly to the power amplifier (PA). The frequency synthesizer design details are given in [8]. Programmable output power is performed by power control logic. The maximal output power is 2dBm and the transmitting distance is more than 10m.

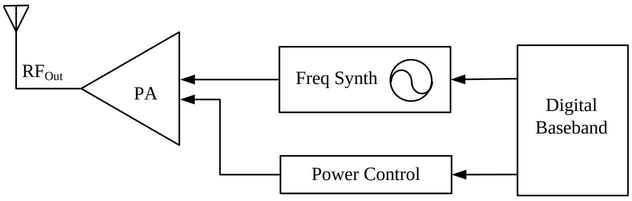

Fig. 6 SRD Transmitter architecture

D. Software

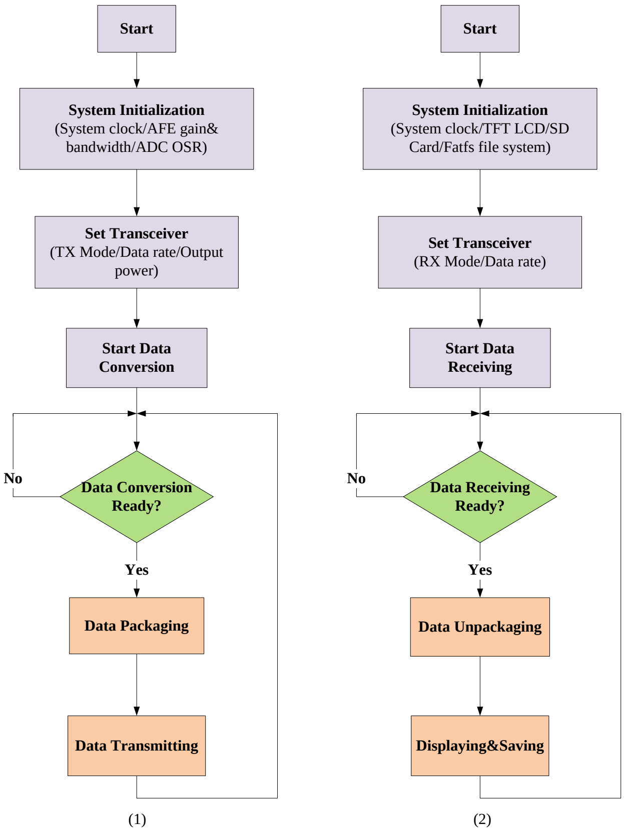

Fig. 7 Software flow diagram (1) TX part (2) RX part

The healthcare system TX part software flow diagram is shown in Fig. 7 (1). After TX system powers on, the system initialization including system clock, AFE gain, AFE bandwidth and ADC OSR is performed. Then the SRD transceiver is configured to TX mode, proper data rate and output power. Next, start data conversion to get the 16 bits ADC raw data (10 effective bits) shown in Fig. 8 and wait for data conversion ready. Then add 4 bits Head and 4 bits End to raw data to do the packaging. After packaged, the data is transmitted to space. Shown in Fig. 7 (2), the RX part software is doing the opposite operation. System initialization including system clock, TFTLCD, SD Card and Fatfs file system is performed after RX system powers on. After configured to RX mode with proper data rate, the SRD Transceiver starts to receive the data. When data receiving is ready, MCU will unpack the data shown in Fig. 8, restore the data on TFTLCD and save the data in SD Card.

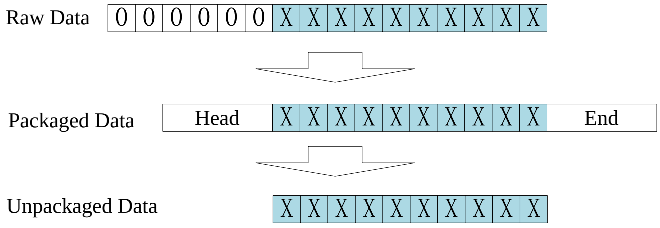

Fig. 8 Data format

III. EXPERIMENTAL RESULTS

The chip micrographs of the AFE, the Incremental ΣΔADC, and the SRD Transceiver are shown in Fig.9 (1)-(3) [5]-[7] respectively. All the ICs are implemented in 0.35um CMOS technology.

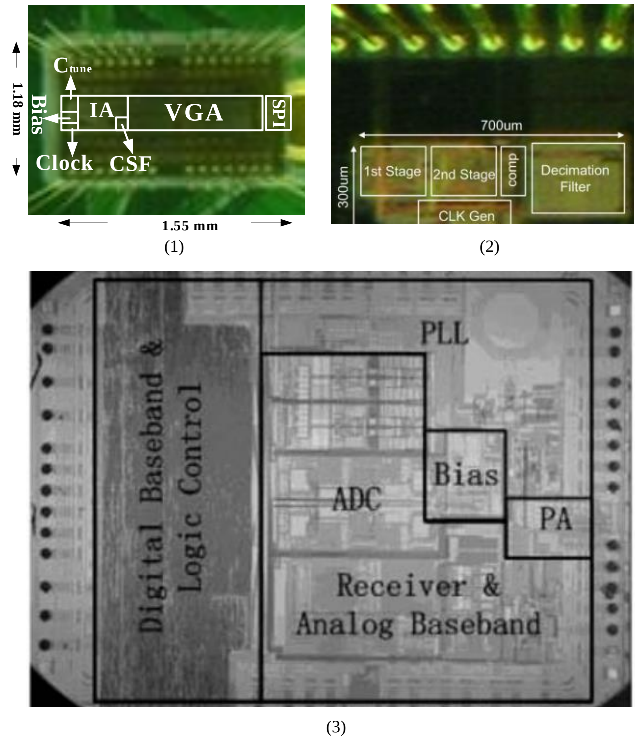

Fig. 9 Chip micrographs [5]-[7]
(1) AFE (2) Incremental ΣΔADC (3) SRD Transceiver

The low-power, wireless, real-time and wearable healthcare system proposed in this paper is realized on the printed circuit board, shown in Fig. 10 (3). The transmitting part is on the left while on the right is the receiving part. Using three wet electrodes (Ag/AgCl), the experiment of monitoring human's ECG signal is performed. Shown in Fig.10 (1), the red and green electrodes are the ECG signal input while the black one is the right leg drive (RLD) output, suppressing the human body common mode interference.

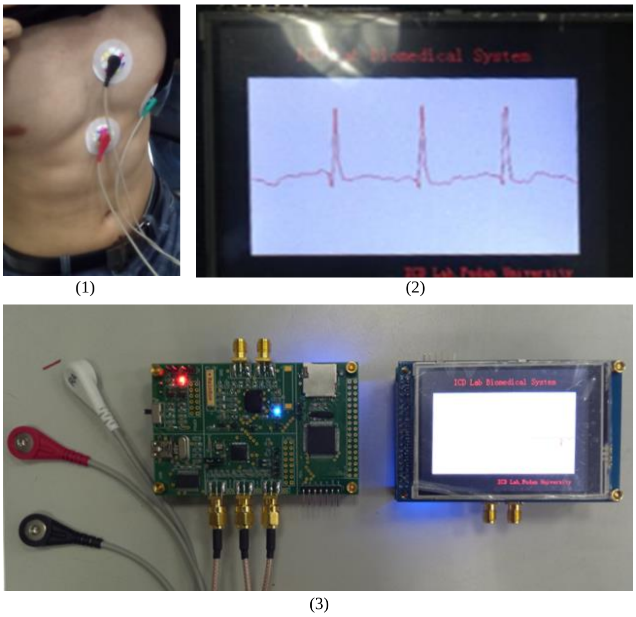

Fig. 10 ECG signal monitoring experiment (1) Electrode placing (2) Restored ECG signal on TFTCLD (3) Proposed healthcare system on PCB

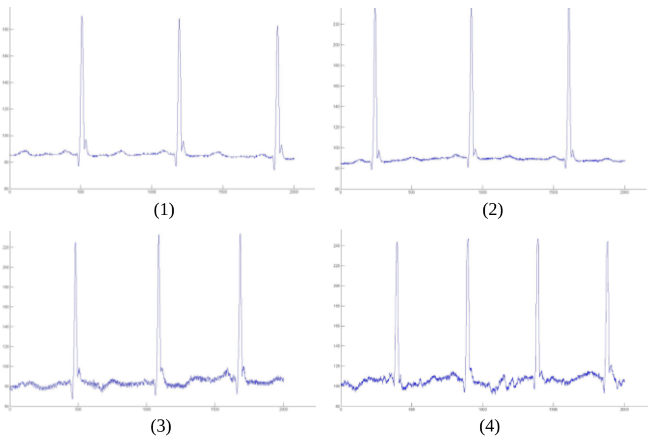

Fig. 11 ECG waves under different conditions (1) Sitting (2) Standing (3) walking (4) running

For ECG signal, the amplitude range is about 100uV-5mV and the frequency range is 0.5-150Hz. The ADC clock is set to 64k Hz and the oversampling ratio 128. Then the ADC sampling rate will be 0.5k Hz. With 10 bits effective data, 4 bits Head and 4 bits End, the transmitting data rate is 9kBs after calculation. So 9.6kBs data rate of the SRD Transceiver is sufficient for communication. The AFE gain and bandwidth setting are 50dB and 500Hz, respectively. Fig.10 (2) shows the restored ECG signal at real time on TFTLCD after wireless communication.

The ECG signal information is also saved in SD card and transferred to PC. The human ECG signal under different conditions is plotted in MATLAB. Fig.11 (1)-(4) shows the ECG waves of sitting, standing, walking and running respectively. One can see that heart rate is rising when doing intense sports.

IV. CONCULSION

In this paper, a bio-potential signals monitoring healthcare system composing of Analog Front End, Incremental ΣΔADC and SRD Transceiver is introduced. The system is designed with low power consumption and flexible configuration, capable of monitoring ExG signals wirelessly at real-time. Experimental results show that the proposed system is portable for people to monitor health.

ACKNOWLEDGMENT

This work is funded by Science and Technology Commission of Shanghai Municipality under Grant 13511501100 and the State Key Laboratory Project of China (No.11MS002).

REFERENCES

[1] H. J. Yoo, et al., “Bio-Medical CMOS ICs [M],” Boston: Springer, 2011

[2] Tee Hui Teo et al., “A 700-uW Wireless Sensor Node SoC for Continuous Real-Time Health Monitoring”, IEEE J. Solid-State Circuits, vol. 45, no. 11, pp. 2292–2299, Nov. 2010

[3] Yanqing Zhang et al., “A Batteryless 19 W MICS ISM-Band Energy Harvesting Body Sensor Node SoC for ExG Applications”, IEEE J. Solid-State Circuits, vol. 48, no. 1, pp. 199–213, Jan. 2013

[4] F. Giroud et al., “ECG Sensor Interface in a Low Power SoC for Wireless Portable ECG Monitoring”, IEEE Biomedical Circuits and Systems Conference (BioCAS). pp. 149-152, 2014

[5] Wenhui Qin et al., “A low power analog front-end for portable biopotential acquisition systems”, IEEE Solid-State and Integrated Circuit Technology (ICSICT), pp. 1-3, 2014

[6] Xiaofei Cao et al., “A 95-dB DR Second Order Incremental ΣΔADC for Multi-channel Healthcare Application”, IEEE Solid-State and Integrated Circuit Technology (ICSICT), pp. 1-3, 2014

[7] Juan Li et al., “A 434/868 MHz CMOS low-IF receiver with I/Q imbalance calibration for SRDs application”, Journal of Semiconductors, vol. 30, no. 3, pp. 97-103, Mar. 2009

[8] Zhang Huajiang et al., “A ΣΔ Fractional-N PLL Frequency Synthesizer with AFC for SRD Applications”, Journal of Semiconductors, vol. 29, no. 7, pp. 47-53, Jul. 2008