Digital Logic Circuit
(SE273 – Fall 2020)
Lecture 3: Boolean Algebra

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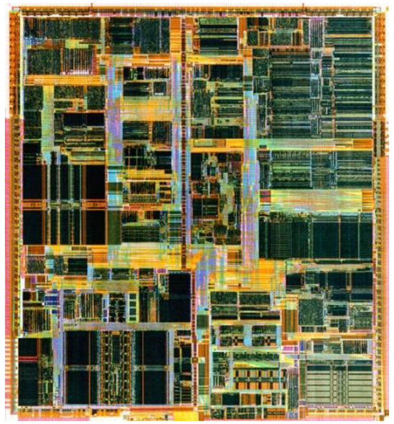
Goal

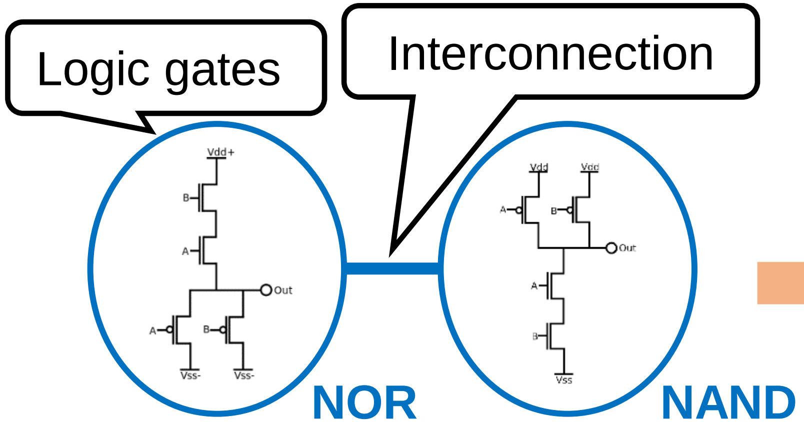
- Learn Boolean algebra and logic gates
  - Basic theory and properties of Boolean algebra
  - Digital logic gates
- Apply simplification of Boolean functions
  - Karnaugh map (K-map)
  - Sum-of-products/product-of-sums simplification

Binary Logic

- Digital circuits manipulates binary information
  - Composed of transistors and interconnections
- Basic circuit is referred to as "**logic gate**"
  - Each gate performs a specific logical operation

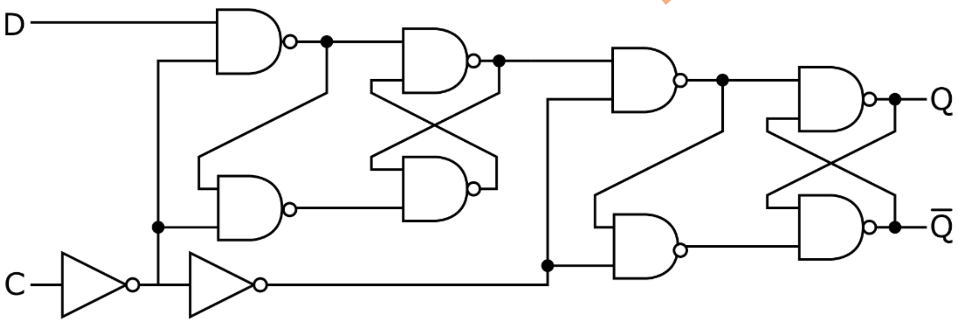
Digital circuits





Part of digital circuit

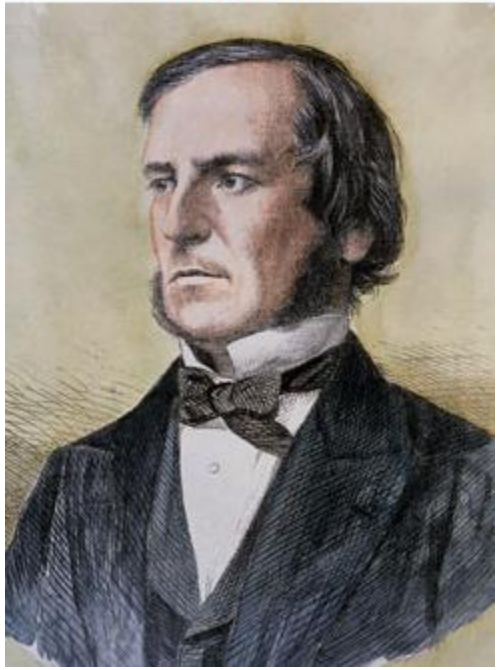
D Flip-flop circuit



Logic Gates and Boolean Algebra

- Why do we need an abstraction of a logic gate?
  - A designer need not be concerned with the internal electronics
  - Only their external logic properties are important
- To describe operational properties of digital circuits,
  - We introduce a mathematical notation to analyze/design circuits
  - The binary logic system is called **Boolean algebras**

George Boole

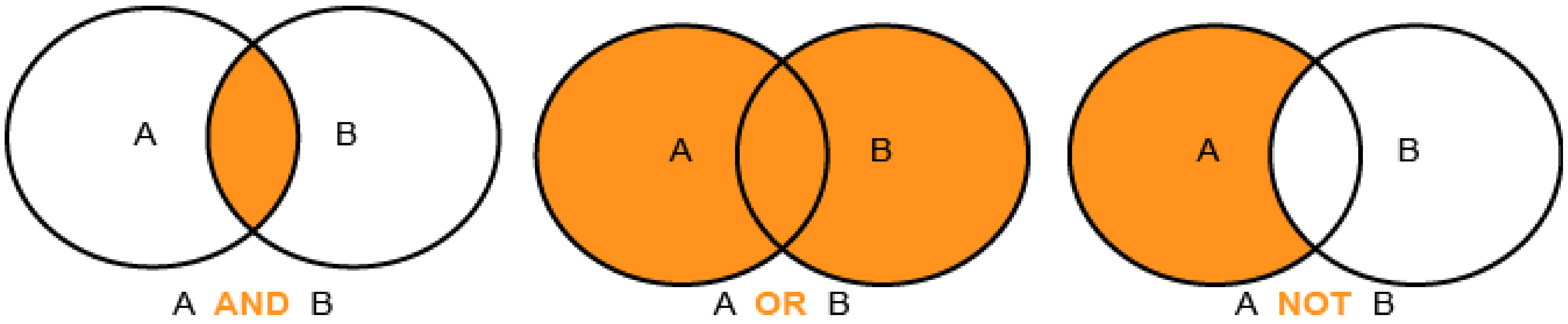


Published a book in 1854
on mathematical theory of logics

Binary Logic

- It deals with binary variables (A,…,X,Y,Z) that take on two discrete values (0 or 1)
- Three basic logical operations

Boolean AND, OR, and NOT



Truth Table

- The definition of the logic operation may be listed in compact form (truth table)
  - A table of combinations of the binary variables showing the relation btw the values that the variables take on and its result

Truth Tables for the Three Basic Logical Operations

AND

X	Y	$Z = X \cdot Y$
0	0	0
0	1	0
1	0	0
1	1	1

OR

X	Y	$Z = X + Y$
0	0	0
0	1	1
1	0	1
1	1	1

NOT

X	$Z = \overline{X}$
0	1
1	0

Boolean Algebra - Binary Logic

- Three basic logical operations

Operation:	AND (product) of two inputs	OR (sum) of two inputs	NOT (complement) on one input
Expression:	$X \cdot Y$, $X \,\&\, Y$	$X + Y$, $X \mid Y$	X', $\bar{X}$, $\sim X$

Truth table:

AND

X	Y	Z = X · Y
0	0	0
0	1	0
1	0	0
1	1	1

OR

X	Y	Z = X + Y
0	0	0
0	1	1
1	0	1
1	1	1

NOT

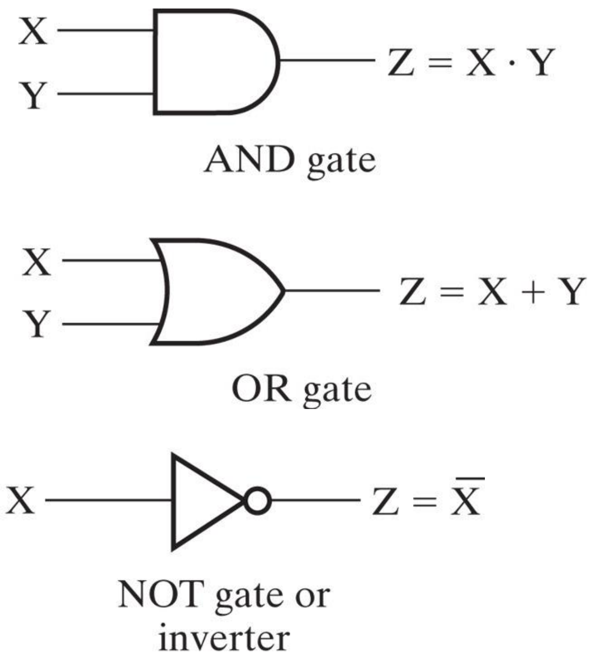
X	$Z = \bar{X}$
0	1
1	0

Do not confuse with
binary arithmetic: ($1_2 + 1_2 = 10_2$)

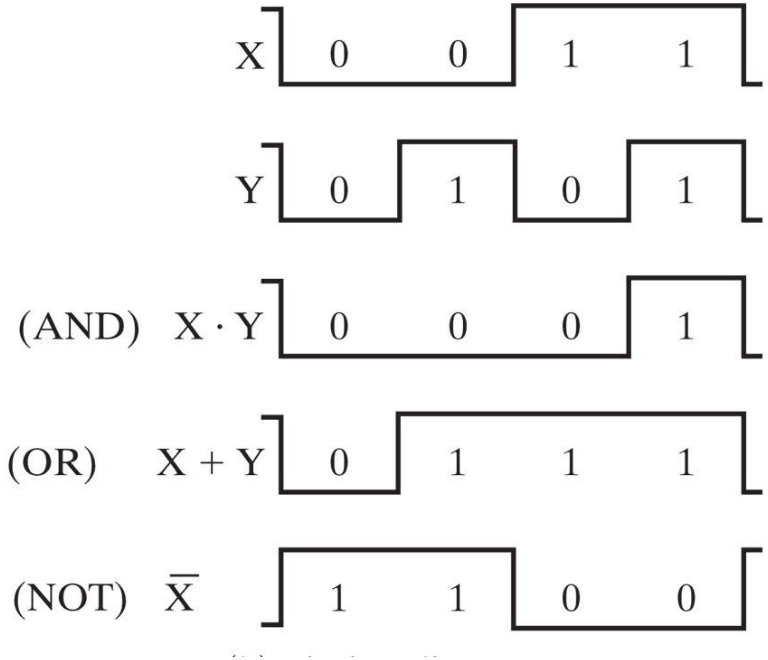
Logic Gates

- They are electronic circuits that operate on one or more input signals to produce an output signal

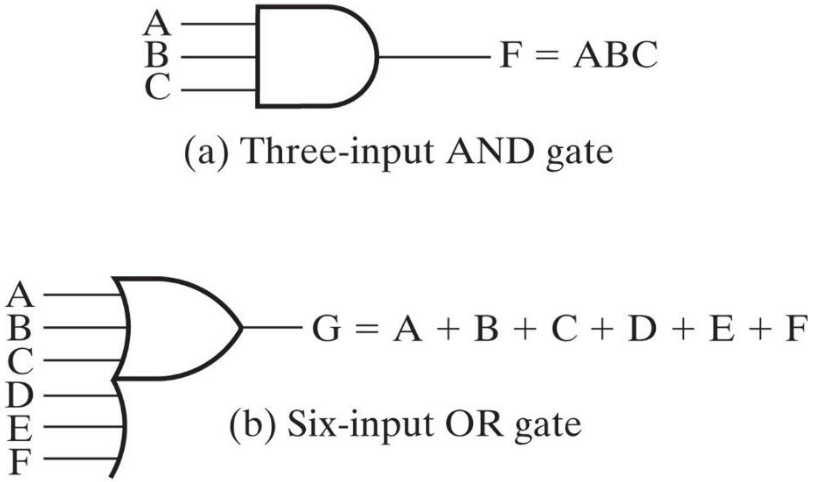
Graphic symbols



Timing diagram

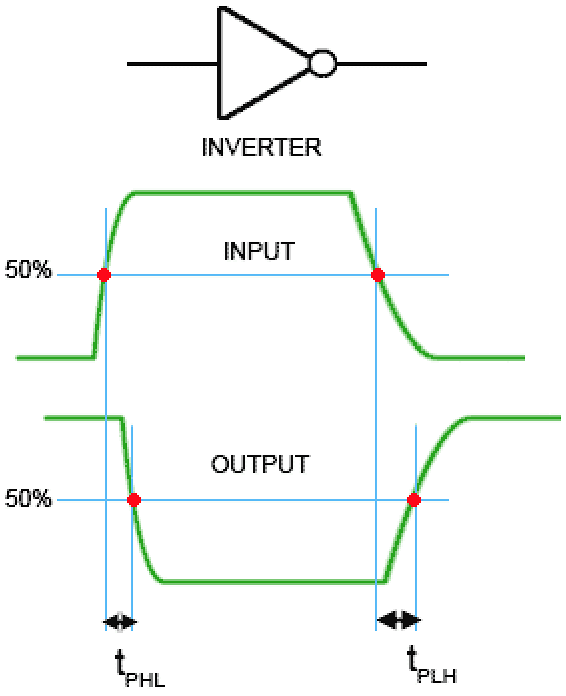


Multi-input gate



Gate Delay

- Each gate has a very important property called gate delay
  - The length of time it takes for an input change to result in the corresponding output change
  - It depends on the technology node (ex: 7nm vs. 65nm), # of inputs, or a gate type



t_{PHL} = Propagation delay high-low
t_{PLH} = Propagation delay low-high

Example – Reading the datasheet

- SN74LVC1G04 – Single Inverter Gate

TEXAS INSTRUMENTS

SN74LVC1G04

SCES214AD–APRIL 1999–REVISED OCTOBER 2014

SN74LVC1G04 Single Inverter Gate

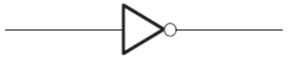
1 Features

- Available in the Ultra-Small 0.64-mm² Package (DPW) with 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages up to 5.5 V Allowing Down Translation to V_{CC}
- Max t_{pd} of 3.3 ns at 3.3-V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3-V
- I_{off} Supports Live-Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

4 Simplified Schematic



3 Description

This single inverter gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G04 device performs the Boolean function $Y = \overline{A}$.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The SN74LVC1G04 device is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

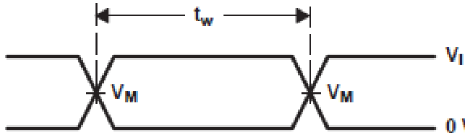
Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
SN74LVC1G04	SOT-23 (5)	2.9mm × 1.6mm
	SC70 (5)	2.0mm × 1.25mm
	SON (6)	1.45mm × 1.0mm
	SON (6)	1.0mm × 1.0mm
	X2SON (4)	0.8mm × 0.8mm

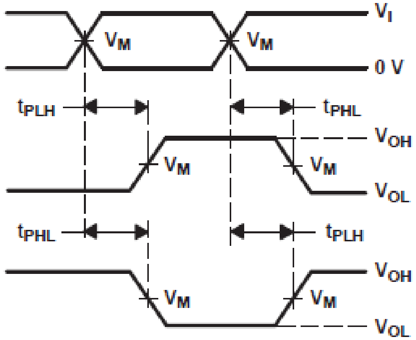
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Function Table

INPUT A	OUTPUT Y
H	L
L	H



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

7.6 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2	6.4	1	4.2	0.7	3.3	0.7	3.1	ns

7.7 Switching Characteristics, C_L = 30 pF or 50 pF, –40°C to 85°C

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3	7.5	1.4	5.2	1	4.2	1	3.7	ns

7.8 Switching Characteristics, C_L = 15 pF, –40°C to 125°C

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2	6.4	1	4.2	0.7	3.3	0.7	3.1	ns

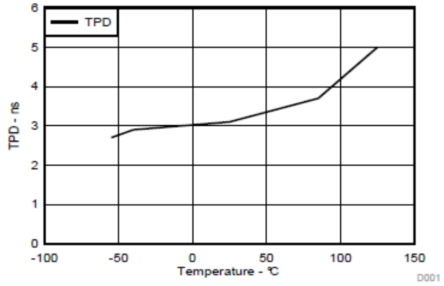


Figure 1. TPD Across Temperature at 3.3-V V_{CC}

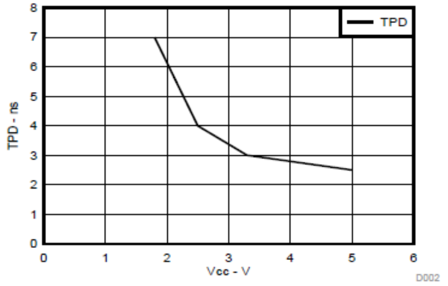


Figure 2. TPD Across V_{CC} at 25°C

Boolean Function

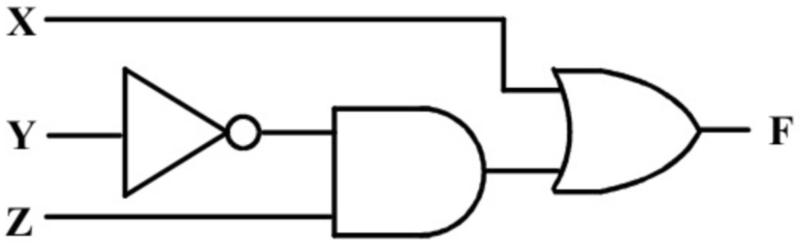
- Boolean algebra: an algebra dealing with binary variables
- Boolean function *F* (or Boolean expression)
  - X and $\bar{Y}Z$ are called '*terms*'

$$F = X + \bar{Y}Z$$

Denotes the Boolean function

Algebraic expression formed by binary variables

Logic circuit diagram



NOT UNIQUE!!
Can be simplified in some cases
(The end justifies the means)

Truth table

X Y Z	$F = X + \bar{Y} \cdot Z$
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

UNIQUE!!

Boolean Function Example

- We can design a logic for lowering the driver's power window

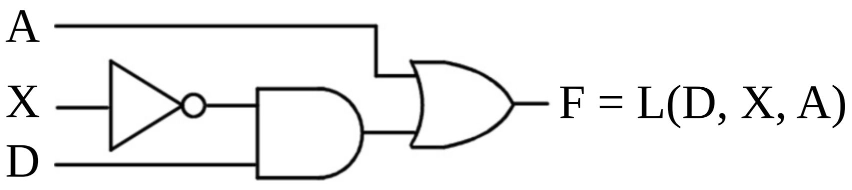
$$L(D, X, A) = D\overline{X} + A$$

- *L*: "lower the window" command
- *D*: output produced by pushing the ↓ button
- *X*: output of a mechanical limit
- *A*: onset of automated lowering operation (ex: when *D*=1 for more than 0.5s)

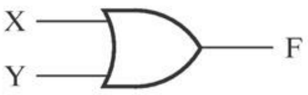
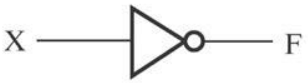
Truth Table??

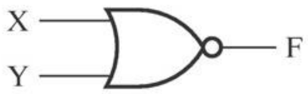
A X D	$F = A + \overline{X} \cdot D$
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

Circuit Diagram

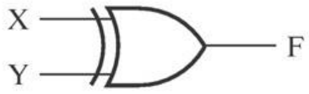


Logic Gates & Boolean Function

Name	Distinctive-Shape Graphics Symbol	Algebraic Equation	Truth Table
AND		$F = XY$	X Y | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = X + Y$	X Y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
NOT (inverter)		$F = \overline{X}$	X | F 0 | 1 1 | 0

Name	Distinctive-Shape Graphics Symbol	Algebraic Equation	Truth Table
NAND		$F = \overline{X \cdot Y}$	X Y | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR		$F = \overline{X + Y}$	X Y | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0

Universal Gates

Name	Distinctive-Shape Graphics Symbol	Algebraic Equation	Truth Table
Exclusive-OR (XOR)		$F = X\overline{Y} + \overline{X}Y = X \oplus Y$	X Y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0
Exclusive-NOR (XNOR)		$F = XY + \overline{X}\,\overline{Y} = \overline{X \oplus Y}$	X Y | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 1

Boolean Algebra

- Basic identities of Boolean algebra

Duality

1.	$X + 0 = X$	2.	$X \cdot 1 = X$	Identity element
3.	$X + 1 = 1$	4.	$X \cdot 0 = 0$	
5.	$X + X = X$	6.	$X \cdot X = X$	Idempotence
7.	$X + \overline{X} = 1$	8.	$X \cdot \overline{X} = 0$	Complement
9.	$\overline{\overline{X}} = X$			Involution
10.	$X + Y = Y + X$	11.	$XY = YX$	Commutative
12.	$(X + Y) + Z = X + (Y + Z)$	13.	$(XY)Z = X(YZ)$	Associative
14.	$X(Y + Z) = XY + XZ$	15.	$X + YZ = (X + Y)(X + Z)$	Distributive
16.	$\overline{X + Y} = \overline{X} \cdot \overline{Y}$	17.	$\overline{X \cdot Y} = \overline{X} + \overline{Y}$	DeMorgan's

Extension of DeMorgan's Theorem

- Very important in Boolean algebra
  - Used to obtain the complement of an expression
  - Manipulate it to reduce # of terms/literals in a function
- Can extend to multiple variables

$$\overline{X_1 + X_2 + \cdots + X_n} = \overline{X_1} \cdot \overline{X_2} \cdot \ldots \cdot \overline{X_n}$$

$$\overline{X_1 X_2 \ldots X_n} = \overline{X_1} + \overline{X_2} + \ldots + \overline{X_n}$$

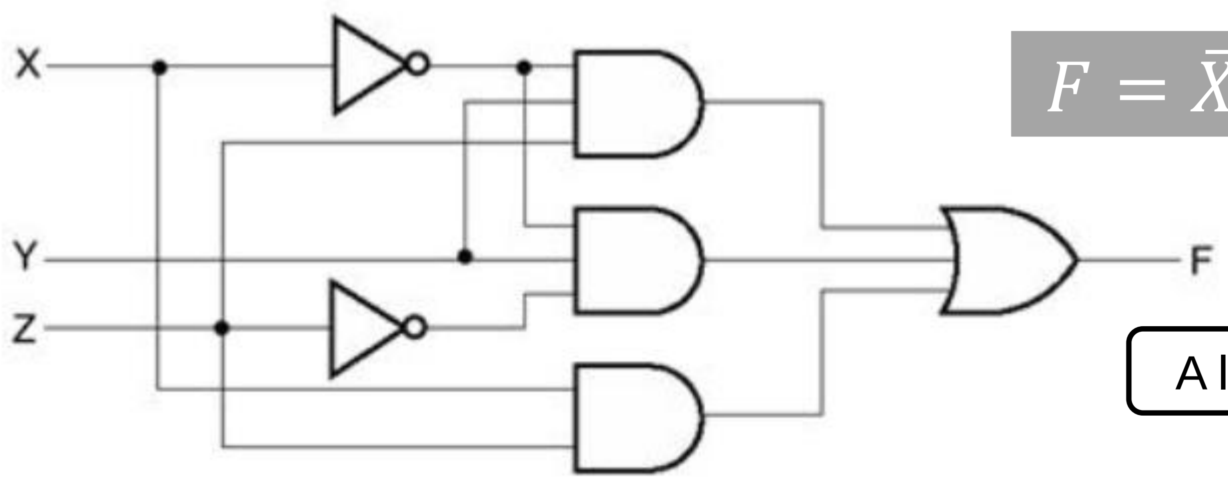
Algebraic Manipulation

- Can **simplify digital circuits** at early design stage
- Let's consider

$$
\begin{aligned}
F &= \bar{X}YZ + \bar{X}Y\bar{Z} + XZ \\
&= \bar{X}Y(Z + \bar{Z}) + XZ && \text{Identity 14: distributive} \\
&= \bar{X}Y \cdot 1 + XZ && \text{Identity 7: Complment} \\
&= \bar{X}Y + XZ && \text{Identity 2: Identity Element}
\end{aligned}
$$

Reduced to two terms from three

What is the Benefit of Algebraic Manipulation?



$$F = \bar{X}YZ + \bar{X}Y\bar{Z} + XZ$$

Three terms, eight literals

A logic gate

An input to a gate

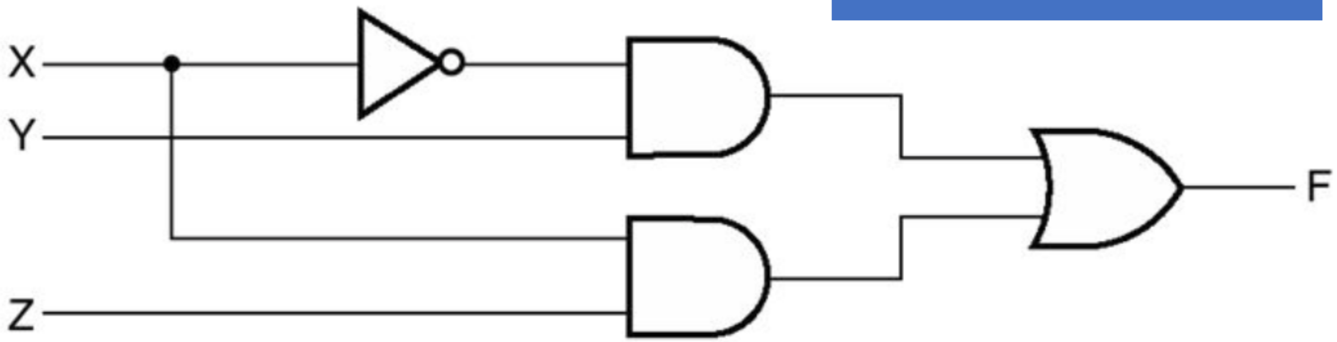
Two terms, four literals

$$F = \bar{X}Y + XZ$$

Reduce an expression!!

1. Fewer gates

2. Fewer inputs per gate



But, Same Truth Table!

$$F = \bar{X}YZ + \bar{X}Y\bar{Z} + XZ$$

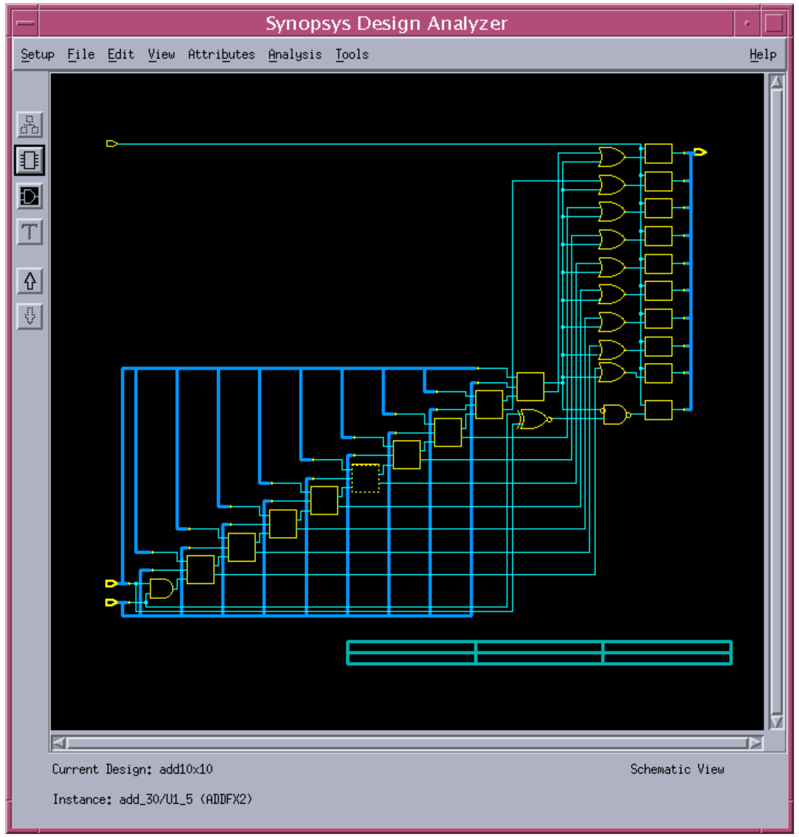
$$F = \bar{X}Y + XZ$$

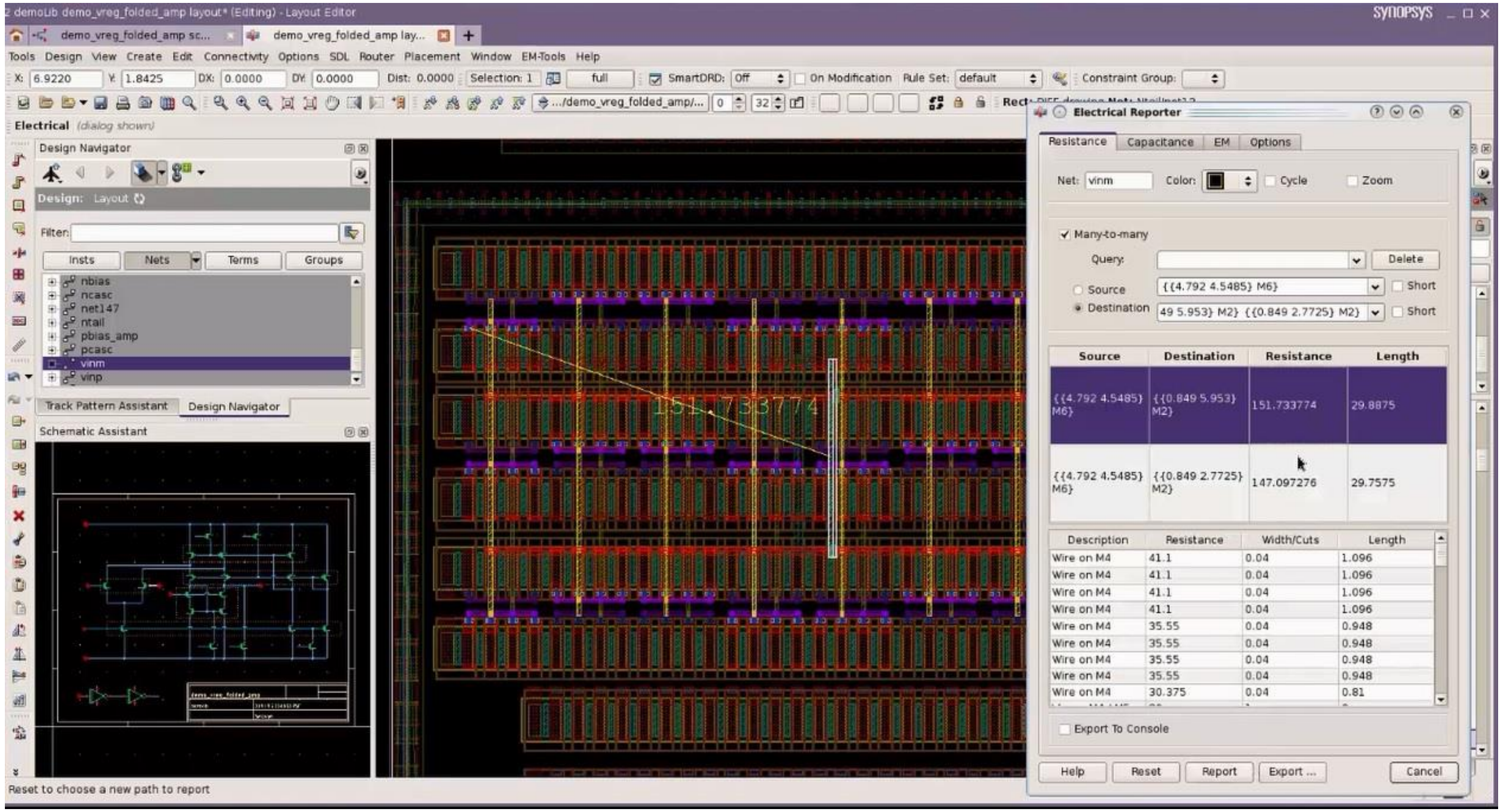
Truth Table for Boolean Function

X	Y	Z	(a) F	(b) F
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

Logic Synthesis: Synopsys Design Compiler

- Logic synthesis tools help designers reduce complex expressions





Logic Gate Reduction

- Again, use Boolean algebra to reduce complexity of digital circuits

1.	$X + 0 = X$	2.	$X \cdot 1 = X$	Identity element
3.	$X + 1 = 1$	4.	$X \cdot 0 = 0$	
5.	$X + X = X$	6.	$X \cdot X = X$	Idempotence
7.	$X + \overline{X} = 1$	8.	$X \cdot \overline{X} = 0$	Complement
9.	$\overline{\overline{X}} = X$			Involution
10.	$X + Y = Y + X$	11.	$XY = YX$	Commutative
12.	$(X + Y) + Z = X + (Y + Z)$	13.	$(XY)Z = X(YZ)$	Associative
14.	$X(Y + Z) = XY + XZ$	15.	$X + YZ = (X + Y)(X + Z)$	Distributive
16.	$\overline{X + Y} = \overline{X} \cdot \overline{Y}$	17.	$\overline{X \cdot Y} = \overline{X} + \overline{Y}$	DeMorgan's

$$X + XY = X(\mathbf{1} + \boldsymbol{Y}) = X$$

$$XY + X\bar{Y} = X(\boldsymbol{Y} + \bar{\boldsymbol{Y}}) = X$$

$$X + \bar{X}Y = (\boldsymbol{X} + \bar{\boldsymbol{X}})(X + Y) = X + Y$$

Logic Gate Reduction

1.	$X + 0 = X$	2.	$X \cdot 1 = X$	Identity element
3.	$X + 1 = 1$	4.	$X \cdot 0 = 0$	
5.	$X + X = X$	6.	$X \cdot X = X$	Idempotence
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16.	$\overline{X + Y} = \overline{X} \cdot \overline{Y}$	17.	$\overline{X \cdot Y} = \overline{X} + \overline{Y}$	DeMorgan's

$$X + XY = X(1 + Y) = X$$

$$XY + X\bar{Y} = X(Y + \bar{Y}) = X$$

$$X + \bar{X}Y = (X + \bar{X})(X + Y) = X + Y$$

$$X(X + Y) = X + XY = X$$

$$(X + Y)(X + \bar{Y}) = X + Y\bar{Y} = X$$

$$X(\bar{X} + Y) = X\bar{X} + XY = XY$$

Duals of previous examples

Consensus Theorem

- Allows us to remove a redundant term

$$XY + \bar{X}Z + YZ = XY + \bar{X}Z$$

Proof:

$$\begin{aligned} XY + \bar{X}Z + YZ &= XY + \bar{X}Z + YZ(X + \bar{X}) \\ &= XY + \bar{X}Z + XYZ + \bar{X}YZ \\ &= XY(1 + Z) + \bar{X}(Z + YZ) \\ &= XY + \bar{X}Z \end{aligned}$$

Sum of Product form

Dual of consensus theorem

$$(X + Y)(\bar{X} + Z)(Y + Z) = (X + Y)(\bar{X} + Z)$$

Product of Sum form

Consensus Theorem: Example

- Example of minimizing Boolean expression with consensus theorem

$$
\begin{aligned}
(A+B)(\bar{A}+C) &= A\bar{A} + AC + \bar{A}B + BC \\
&= AC + \bar{A}B + BC \\
&= AC + \bar{A}B
\end{aligned}
$$

Consensus theorem applied

Complement of a Function

- Obtain by interchanging 1's to 0's and vice versa in the truth table
- Also, it can be derived by using DeMorgan's theorem

$$\overline{F_1} = \overline{\bar{X}Y\bar{Z} + \bar{X}\bar{Y}Z} = \overline{(\bar{X}Y\bar{Z})} \cdot \overline{(\bar{X}\bar{Y}Z)}$$
$$= (X + \bar{Y} + Z) \cdot (\mathrm{X} + \mathrm{Y} + \bar{Z})$$

$$\overline{F_2} = \overline{X(\bar{Y}\bar{Z} + YZ)} = \bar{X} + \overline{(\bar{Y}\bar{Z} + YZ)}$$
$$= \bar{X} + (\overline{\bar{Y}\bar{Z}} \cdot \overline{YZ}) = \bar{X} + (Y + Z)(\bar{Y} + \bar{Z})$$

Standard Forms - Minterms

- **Minterm**: a product term in which all the variables appear only once
  - It represents exactly one combination of the binary variables in a truth table
  - For ‘n’ variables, there are ‘2^n’ distinct minterms

1 for a specific binary combination

Minterms for Three Variables

X	Y	Z	Product Term	Symbol	m_0	m_1	m_2	m_3	m_4	m_5	m_6	m_7
0	0	0	$\bar{X}\bar{Y}\bar{Z}$	m_0	1	0	0	0	0	0	0	0
0	0	1	$\bar{X}\bar{Y}Z$	m_1	0	1	0	0	0	0	0	0
0	1	0	$\bar{X}Y\bar{Z}$	m_2	[illegible]	[illegible]	1	0	0	0	0	0
0	1	1	$\bar{X}YZ$	m_3	[illegible]	[illegible]	0	1	0	0	0	0
1	0	0	$X\bar{Y}\bar{Z}$	m_4	0	0	0	0	1	0	0	0
1	0	1	$X\bar{Y}Z$	m_5	0	0	0	0	0	1	0	0
1	1	0	$XY\bar{Z}$	m_6	0	0	0	0	0	0	1	0
1	1	1	XYZ	m_7	0	0	0	0	0	0	0	1

Two discrete signals

Standard Forms - Maxterms

- **Maxterm**: a sum term that contains all the variables
  - Each maxterm is a logical sum with each variable
  - Complemented if it is 1 and uncomplemented if it is 0

0 for a specific binary combination

Maxterms for Three Variables

X	Y	Z	Sum Term	Symbol	M_0	M_1	M_2	M_3	M_4	M_5	M_6	M_7
0	0	0	$X+Y+Z$	M_0	0	1	1	1	1	1	1	1
0	0	1	$X+Y+\overline{Z}$	M_1	1	0	1	1	1	1	1	1
0	1	0	$X+\overline{Y}+Z$	M_2	1	1	0	1	1	1	1	1
0	1	1	$X+\overline{Y}+\overline{Z}$	M_3	1	1	1	0	1	1	1	1
1	0	0	$\overline{X}+Y+Z$	M_4	1	1	1	1	0	1	1	1
1	0	1	$\overline{X}+Y+\overline{Z}$	M_5	1	1	1	1	1	0	1	1
1	1	0	$\overline{X}+\overline{Y}+Z$	M_6	1	1	1	1	1	1	0	1
1	1	1	$\overline{X}+\overline{Y}+\overline{Z}$	M_7	1	1	1	1	1	1	1	0

$$M_j = \overline{m_j}$$

Representing a Boolean Function w/ Minterms

- A Boolean function can be expressed by forming logical sum of all the minterms that produce a 1 in the truth table

Boolean function F

X	Y	Z	F	$\bar{F}$
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

Sum of minterms

$$F = (\bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} + X\bar{Y}Z + XYZ)$$
$$= m_0 + m_2 + m_5 + m_7$$

Can be abbreviated by listing only decimal subscripts of minterms

$$F(X,Y,Z) = \sum m(0,2,5,7)$$

Logical sum (Boolean OR)

Representing a Boolean Function w/ Maxterms

- Consider the complement of a Boolean function F

X	Y	Z	F	$\bar{F}$
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

$$\bar{F} = (\bar{X}\bar{Y}Z + \bar{X}YZ + X\bar{Y}\bar{Z} + XY\bar{Z})$$
$$= m_1 + m_3 + m_4 + m_6 = \sum m(1,3,4,6)$$

Take complement again

$$F = \overline{m_1 + m_3 + m_4 + m_6}$$
$$= \overline{m_1} \cdot \overline{m_3} \cdot \overline{m_4} \cdot \overline{m_6} = M_1 \cdot M_3 \cdot M_4 \cdot M_6$$
$$= (X + Y + \bar{Z})(X + \bar{Y} + \bar{Z})(\bar{X} + Y + Z)(\bar{X} + \bar{Y} + Z)$$

Logical product (Boolean AND)

Product of maxterms

$$F(X,Y,Z) = \prod M(1,3,4,6)$$

Summary on Minterms

- Important properties of minterms
  1. There are 2^n minterms for n Boolean variables
  2. Any Boolean function can be expressed as a logical sum of minterms
  3. The complement of a function contains those minterms not included in the original function
  4. A function that includes all the 2^n minterms is equal to logic 1