Digital Logic Circuit (SE273 – Fall 2020)

Lecture 1: Admin

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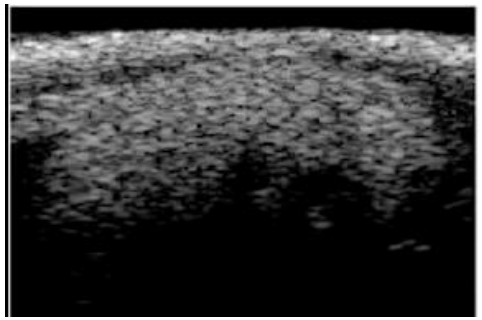
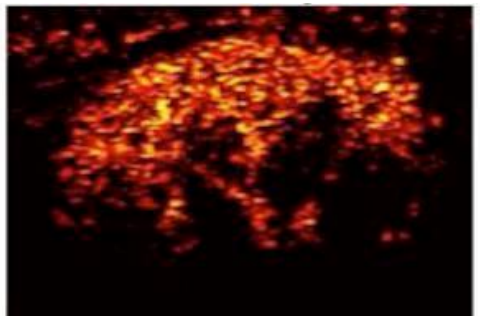
Research Area: Medical Ultrasound Imaging and Therapeutics

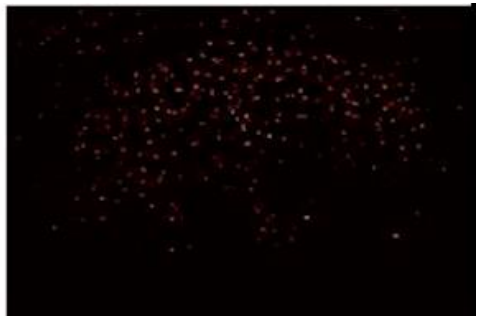
- Ultrasound-based Multi-modal Imaging Technologies
- Novel Ultrasound Imaging and Therapeutic Technologies
- Deep-learning based Ultrasound Image Processing and Diagnosis



B-mode



Ultrafast Doppler



Super-resolution

Instructor – Research

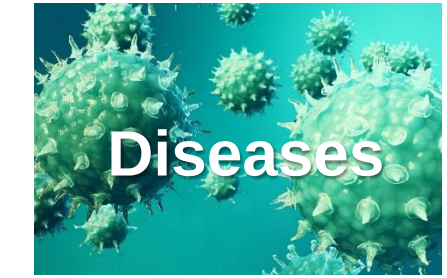
Morphology

Hemo-dynamics

Mechanical property

Composition

Optical property

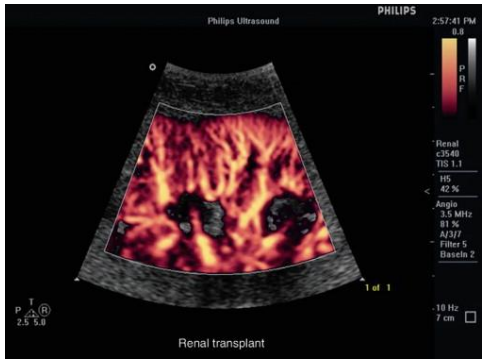


Morphological imaging

3D Real-time non-invasive anatomical information

Doppler imaging

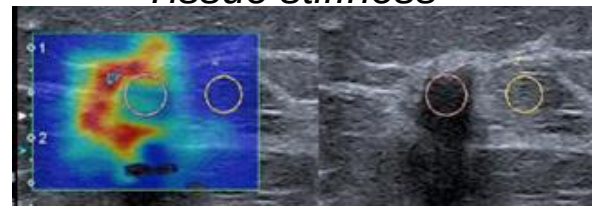
Real-time blood-flow



Hemodynamics

Shear-wave / Strain elasticity imaging

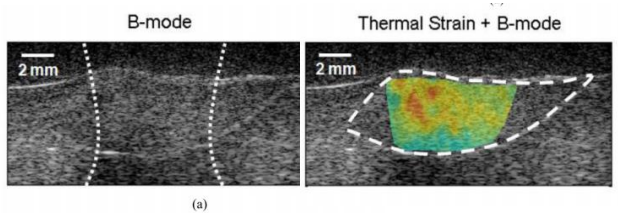
Tissue stiffness



Breast imaging: Malignant invasive ductal carcinoma (Score 5)

Thermal strain imaging

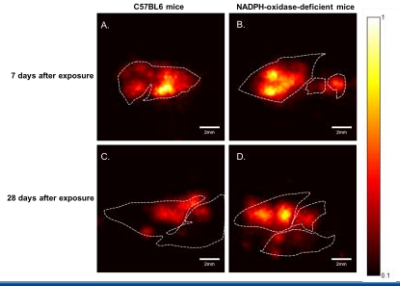
Fat vs Water-based tissue



Fat identification in NAFLD

Photoacoustic imaging

Optical absorption



Course objectives

- Understanding the digital system
  (Midterm / Final)
  - ~ Midterm: Combinational logic design
  - ~ Final: Sequential logic and System design

- Learning skills to design the basic digital system
  (Term project)
  - Design a simple calculator (processor) by using HDL

Term project

- When: Will be assigned after Midterm (~3 wks)
- What: You will design a simple processor based on HDL
- How: 2 Students/team - Random mating
- To be determined further detail due to Covid-19 situation

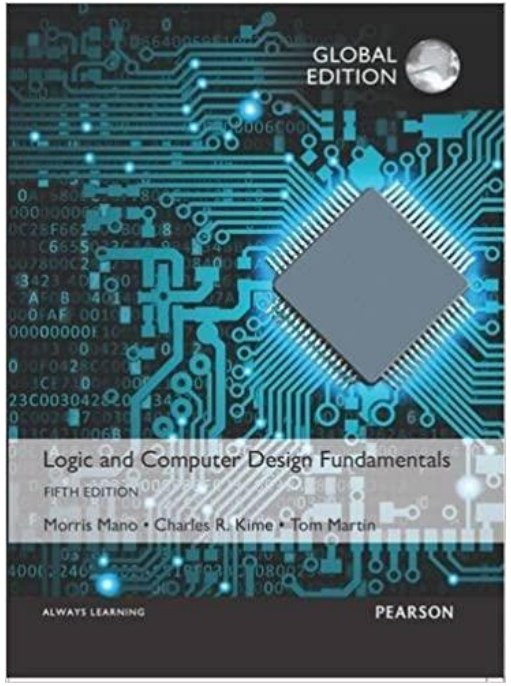
Logistics

- Weekly lectures: Mon & Wed 2:30 - 4:00 PM, Online lecture
- Grading (TBD): Midterm (30%), Final (30%), Term projects (30%), Attendance (10%) + Engagement (bonus 5%)
- Term projects: A simple processor design using VHDL
- Office hours: Mon/Wed after class or by appointment
- Holidays: 9/7 (Anniversary), 9/30 (Thanksgiving)

Logistics

- Handout:
  - Some materials courtesy of Jaeha Kung (DGIST)

- Textbook:
  - **“Logic and Computer Design Fundamentals”, Mano, Kime, Martin, Pearson**
  - “Digital Design”, Mano, Ciletti, Pearson
  - “Fundamentals of Digital Logic with VHDL design”, Brown, McGraw-Hill



Academic Integrity

- Don’t cheat. (Zero Tolerance)

- All work is to be done individually unless stated otherwise by the professor

- Talking things over is generally OK and even encouraged, exchanging or copying files or written work is NEVER ALLOWED.

- If you are having trouble with the assignments, come to us for help (and we mean it).

- Regardless of reasons, cheating will significantly affect your grade.

Note for disability

If you have a disability for which you are or may be requesting an accommodation, you are encouraged to contact me via e-mail jaesok.yu@dgist.ac.kr, as early as possible in the term. We will determine reasonable accommodations for this course.

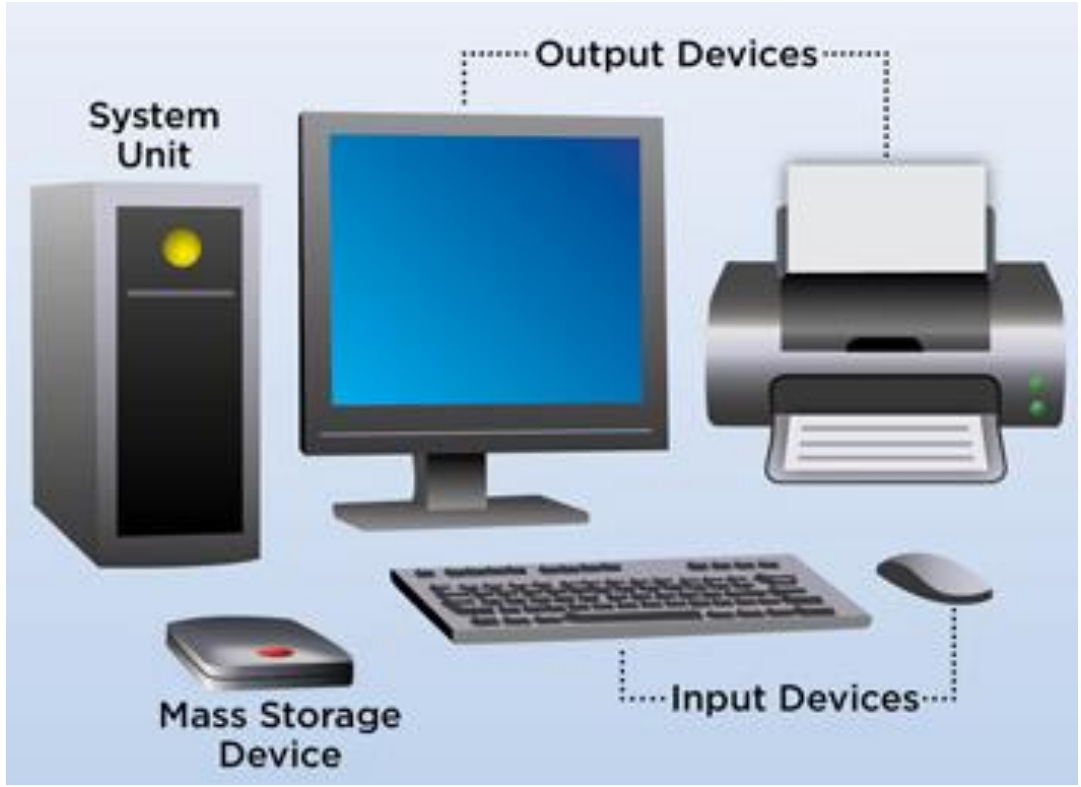
Questions?

Comments? and

Any suggestion?

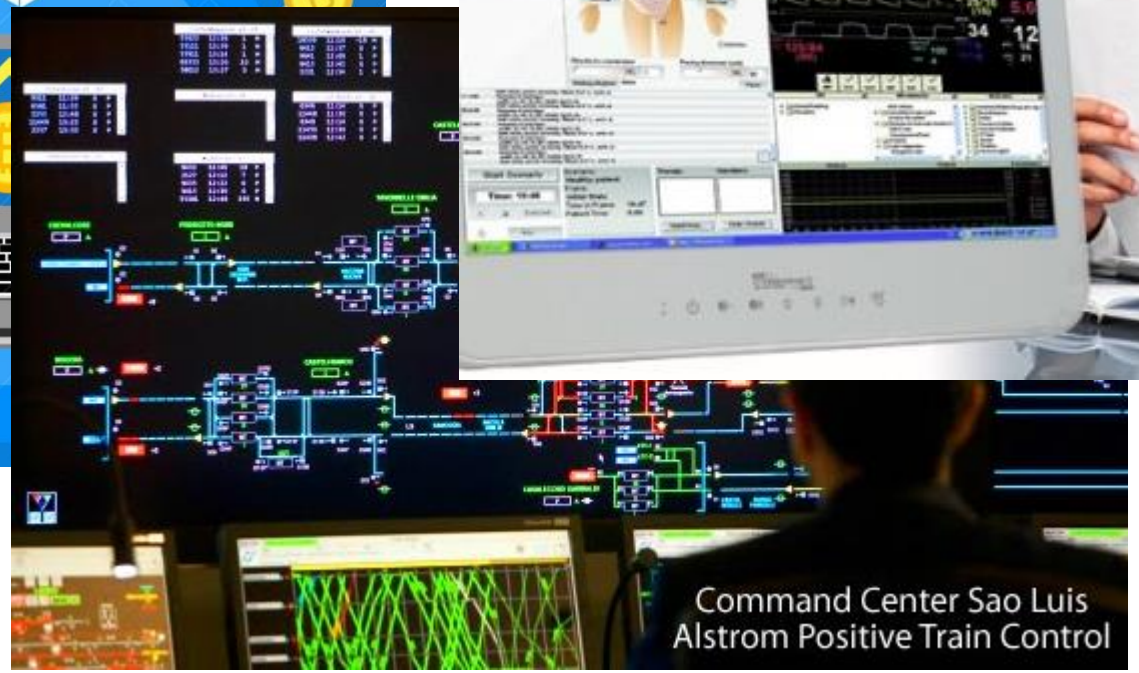
What Are Digital Computers?

We are living in the “information age” with a number of computing devices



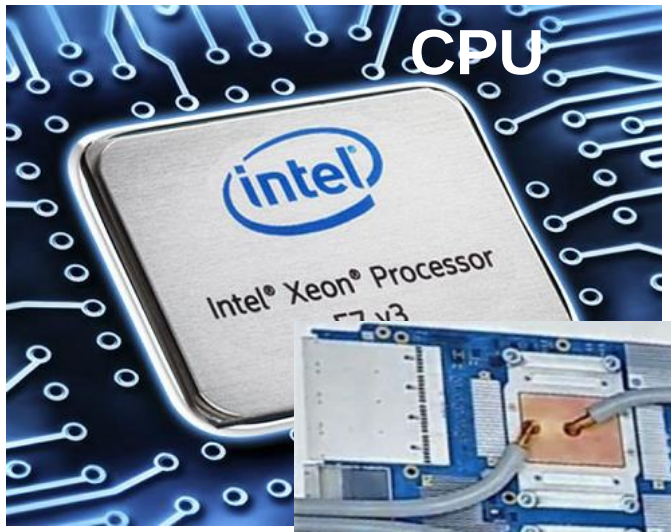
Computers Are Everywhere

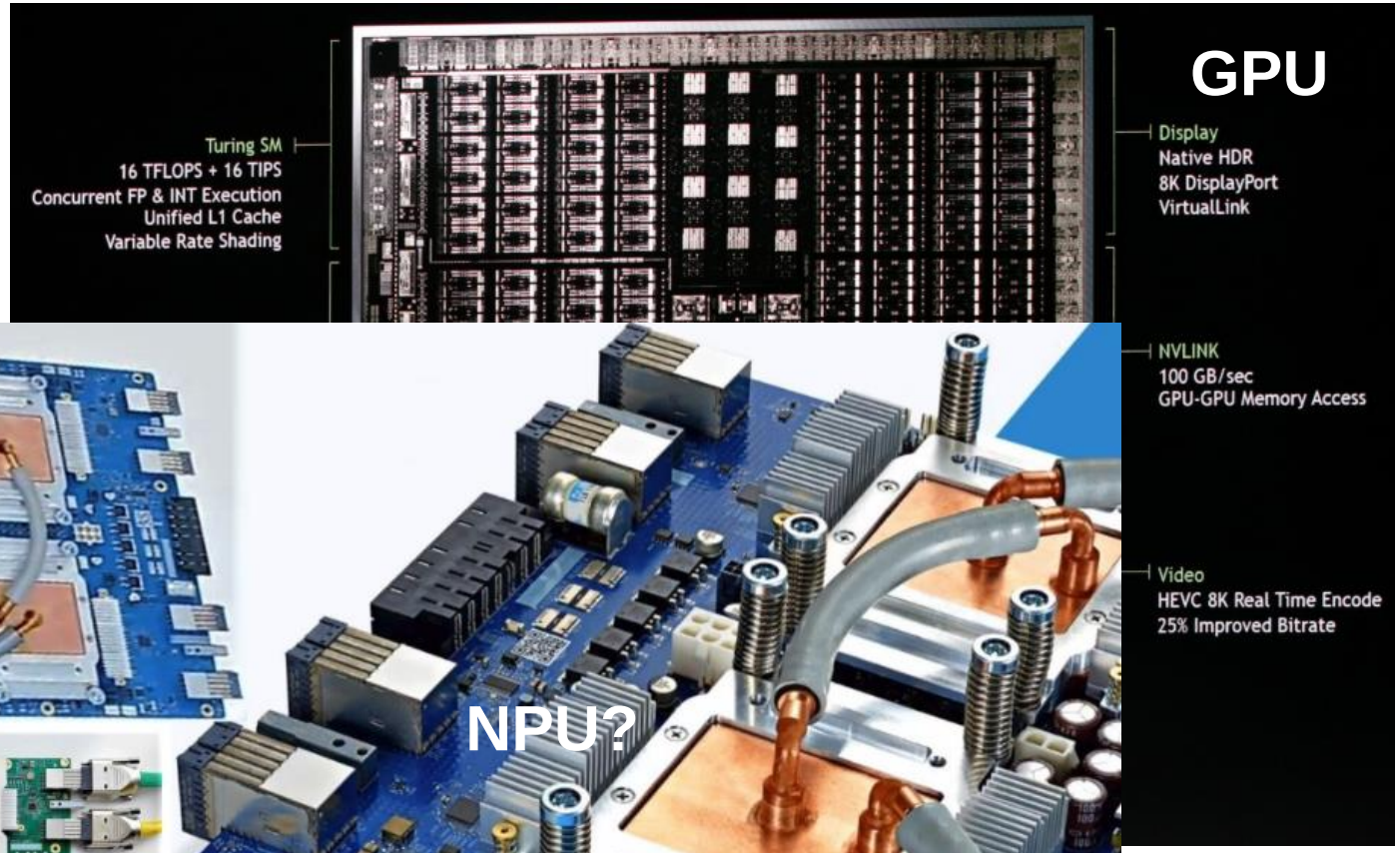
Computers are involved in business transactions, transportation, medical treatment, communications, etc.

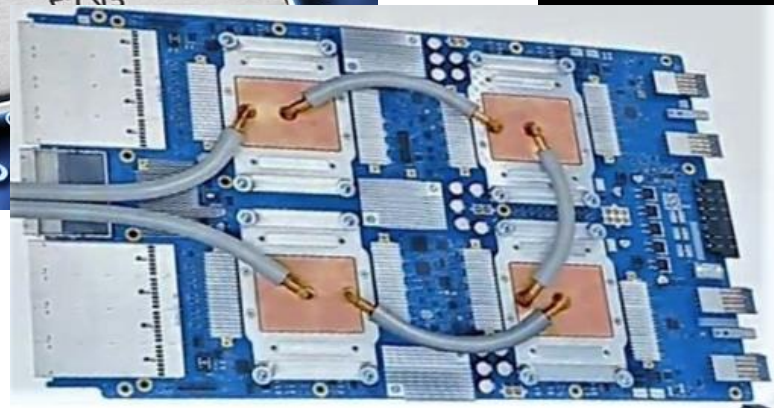


Types of Digital Computers

- General Purpose Processors (CPU, GPU, NPU?)

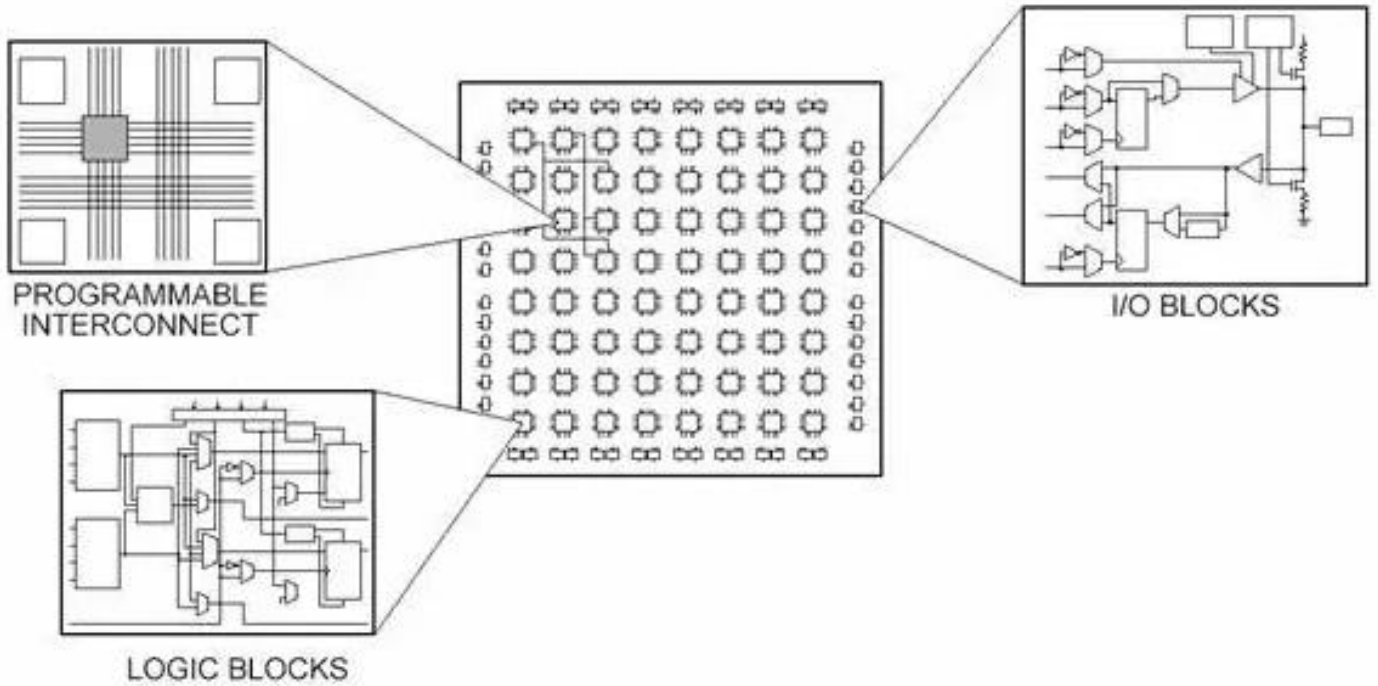






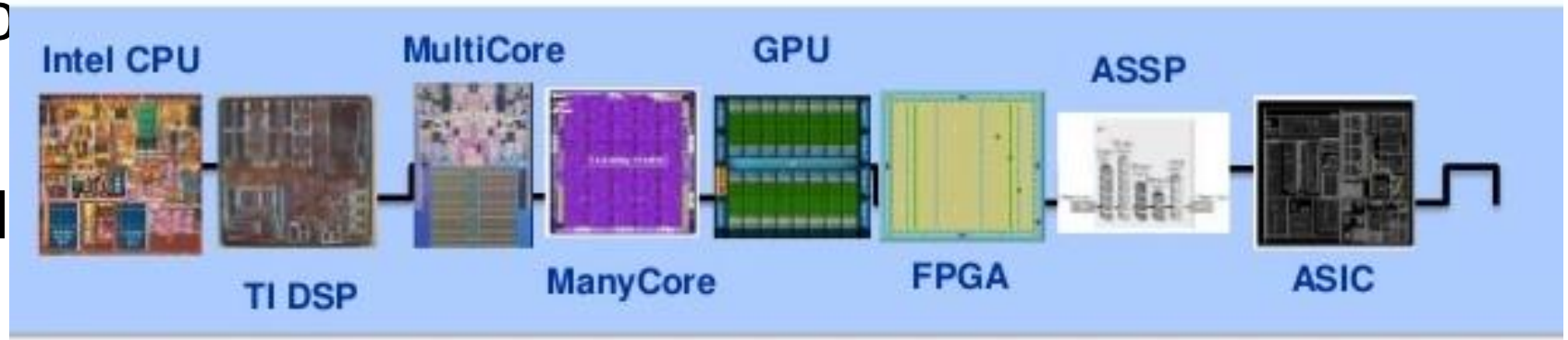
Types of Digital Computers

- General Purpose Processors (CPU, GPU, NPU?)
- Field Programmable Gate Array (FPGA)



Types of Digital Computers

- General Purpose Pro
- Field Programmable
- Application-Specific I

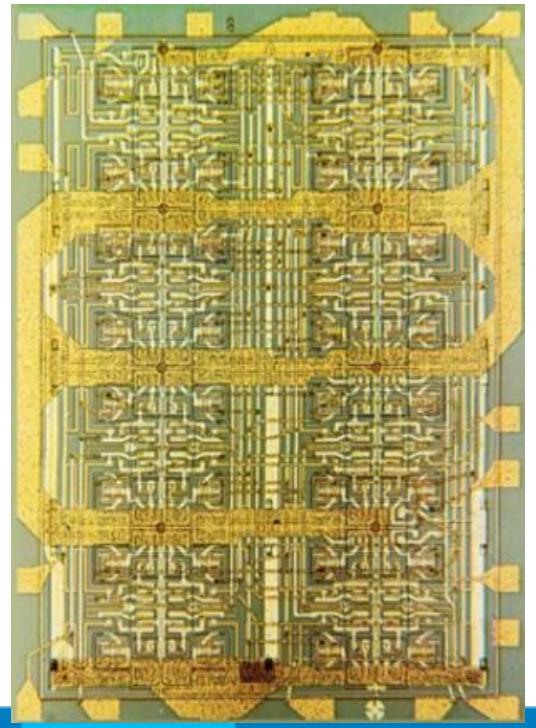


CPU:
- Market-agnostic
- Accessible to many programmers (C++)
- Flexible, portable

FPGA:
- Somewhat Restricted Market
- Harder to Program (Verilog)
- More efficient than SW
- More expensive than ASIC

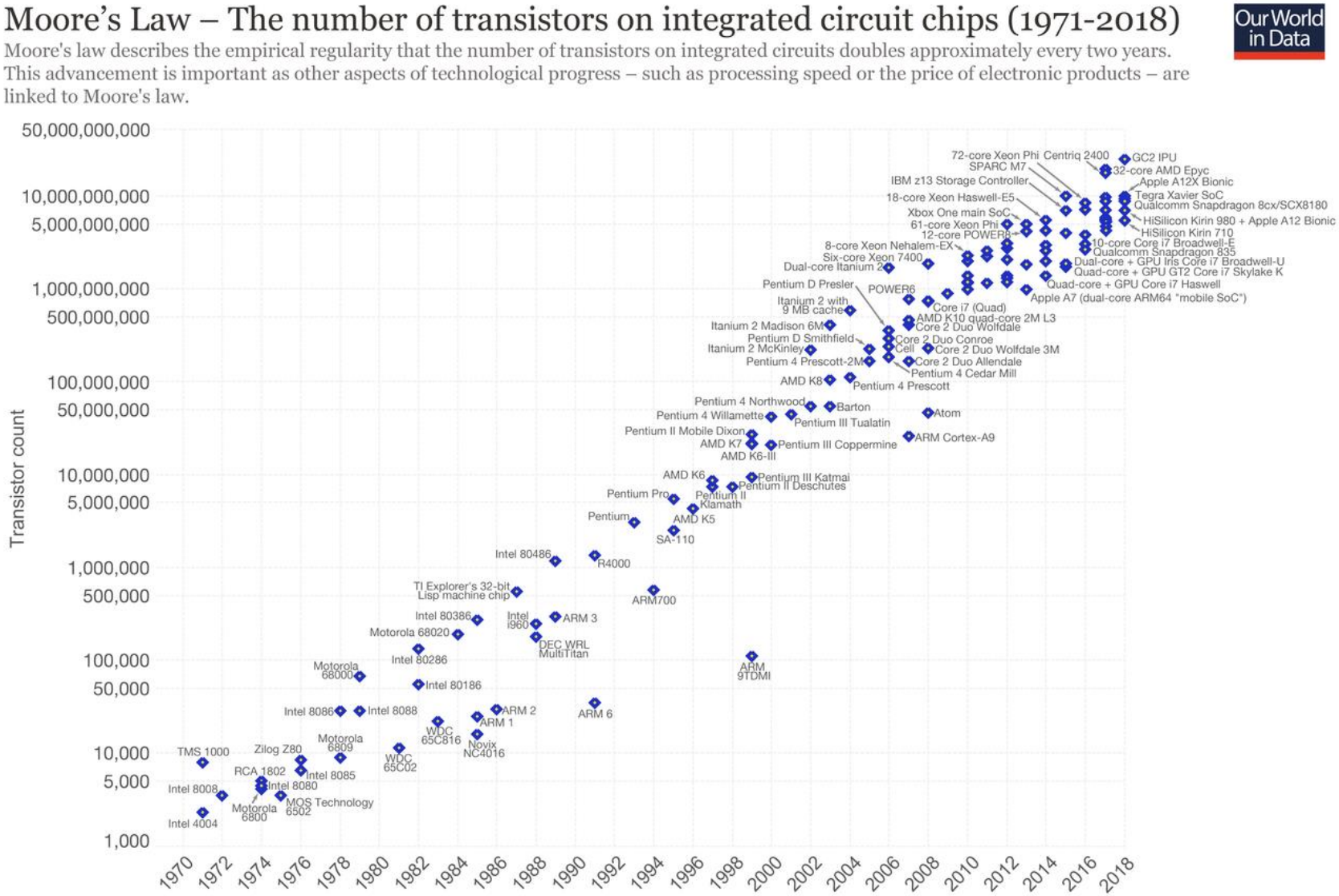
ASIC
- Market-specific
- Fewer programmers
- Rigid, less programmable
- Hard to build (physical)

Source: Altera

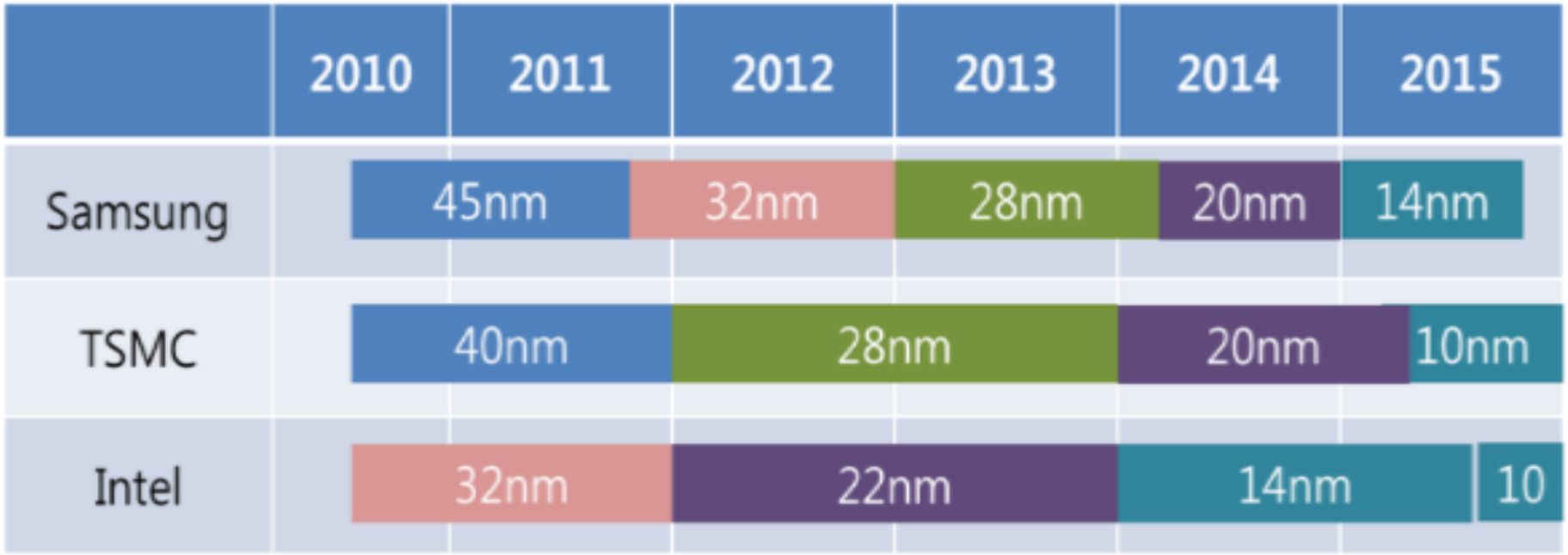


Fairchild 4500 (IBM & Texas Instruments)
ASIC prototype using computer-aided design
for mass production of ICs

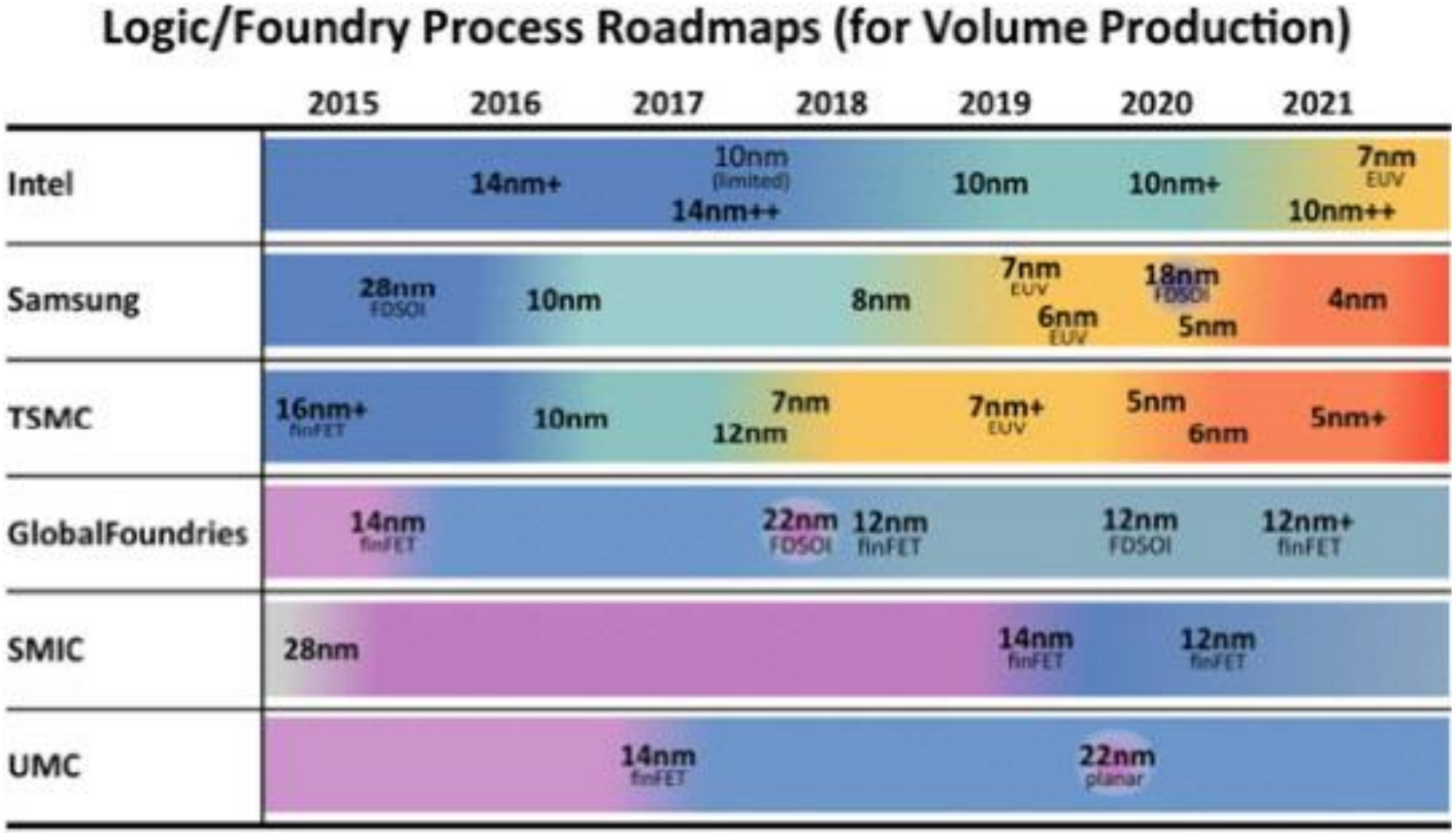
Moore’s Law


Moore’s Law – The number of transistors on integrated circuit chips (1971-2018)
Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.
Our World in Data
Transistor count
50,000,000,000
10,000,000,000
5,000,000,000
1,000,000,000
500,000,000
100,000,000
50,000,000
10,000,000
5,000,000
1,000,000
500,000
100,000
50,000
10,000
5,000
1,000
1970 1972 1974 1976 1978 1980 1982 1984 1986 1988 1990 1992 1994 1996 1998 2000 2002 2004 2006 2008 2010 2012 2014 2016 2018
72-core Xeon Phi Centriq 2400
GC2 IPU
SPARC M7
32-core AMD Epyc
IBM z13 Storage Controller
Apple A12X Bionic
18-core Xeon Haswell-E5
Tegra Xavier SoC
Xbox One main SoC
Qualcomm Snapdragon 8cx/SCX8180
61-core Xeon Phi
HiSilicon Kirin 980 + Apple A12 Bionic
12-core POWER8
HiSilicon Kirin 710
8-core Xeon Nehalem-EX
10-core Core i7 Broadwell-E
Six-core Xeon 7400
Qualcomm Snapdragon 835
Dual-core Itanium 2
Dual-core + GPU Iris Core i7 Broadwell-U
Quad-core + GPU GT2 Core i7 Skylake K
Pentium D Presler
POWER6
Quad-core + GPU Core i7 Haswell
Itanium 2 with 9 MB cache
Apple A7 (dual-core ARM64 "mobile SoC")
Core i7 (Quad)
AMD K10 quad-core 2M L3
Itanium 2 Madison 6M
Core 2 Duo Wolfdale
Pentium D Smithfield
Core 2 Duo Conroe
Itanium 2 McKinley
Cell
Core 2 Duo Wolfdale 3M
Pentium 4 Prescott-2M
Core 2 Duo Allendale
Pentium 4 Cedar Mill
AMD K8
Pentium 4 Prescott
Pentium 4 Northwood
Barton
Atom
Pentium 4 Willamette
Pentium III Tualatin
Pentium II Mobile Dixon
ARM Cortex-A9
AMD K7
Pentium III Coppermine
AMD K6-III
AMD K6
Pentium III Katmai
Pentium II Deschutes
Pentium Pro
Pentium II Klamath
Pentium
AMD K5
SA-110
Intel 80486
R4000
TI Explorer's 32-bit Lisp machine chip
ARM700
Intel 80386
Intel i960
ARM 3
Motorola 68020
DEC WRL MultiTitan
Intel 80286
ARM 9TDMI
Motorola 68000
Intel 80186
Intel 8086
Intel 8088
ARM 2
ARM 1
ARM 6
WDC 65C816
Motorola 6809
Novix NC4016
TMS 1000
Zilog Z80
WDC 65C02
RCA 1802
Intel 8085
Intel 8008
Intel 8080
MOS Technology 6502
Motorola 6800
Intel 4004

Semiconductor Foundry Process Roadmap (~2015)



Semiconductor Foundry Process Roadmap (2015~)



Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embelishments, so these points of transition should only be seen as very general guidelines.

Sources: Companies, conference reports, IC Insights

Now what?

Computing / Quantum computing

We're not prepared for the end of Moore's Law

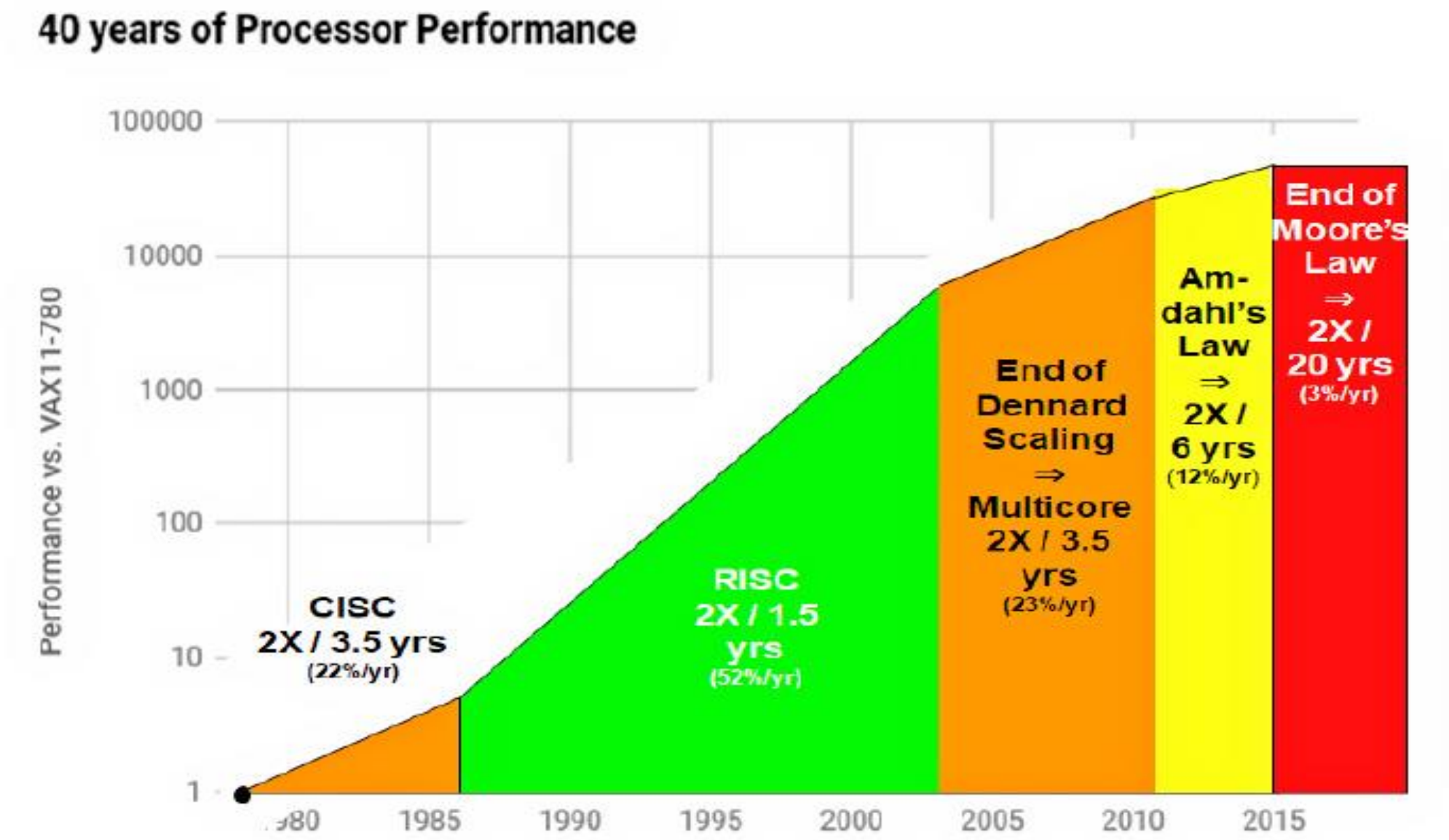
It has fueled prosperity of the last 50 years. But the end is now in sight.

by **David Rotman** February 24, 2020

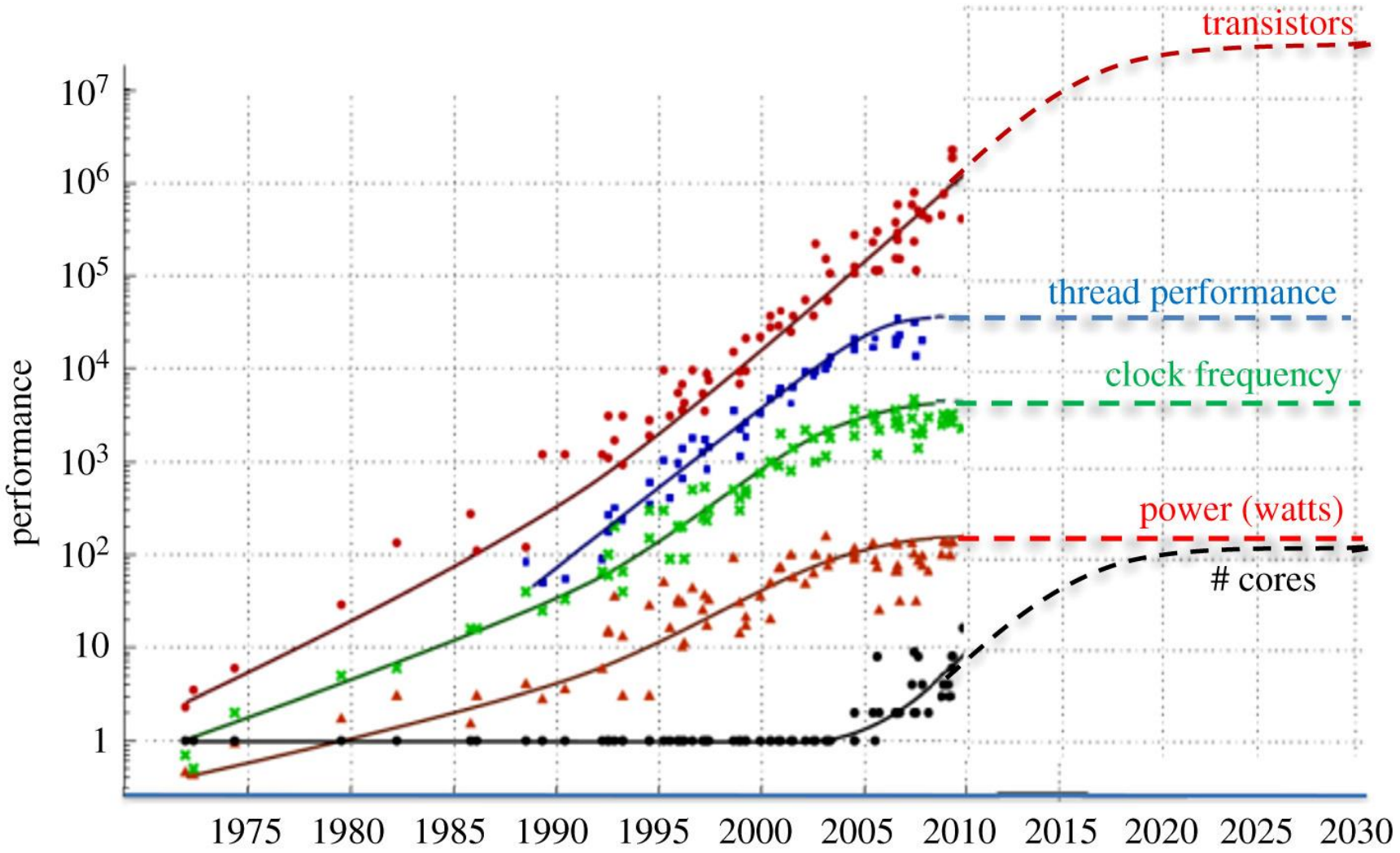
Gordon Moore's 1965 forecast that the number of components on an integrated circuit would double every year until it reached an astonishing 65,000 by 1975 is the greatest technological prediction of the last half-century. When it proved correct in 1975, he revised what has become known as Moore's Law to a doubling of transistors on a chip every two years.

Since then, his prediction has defined the trajectory of technology and, in many ways, of progress itself.

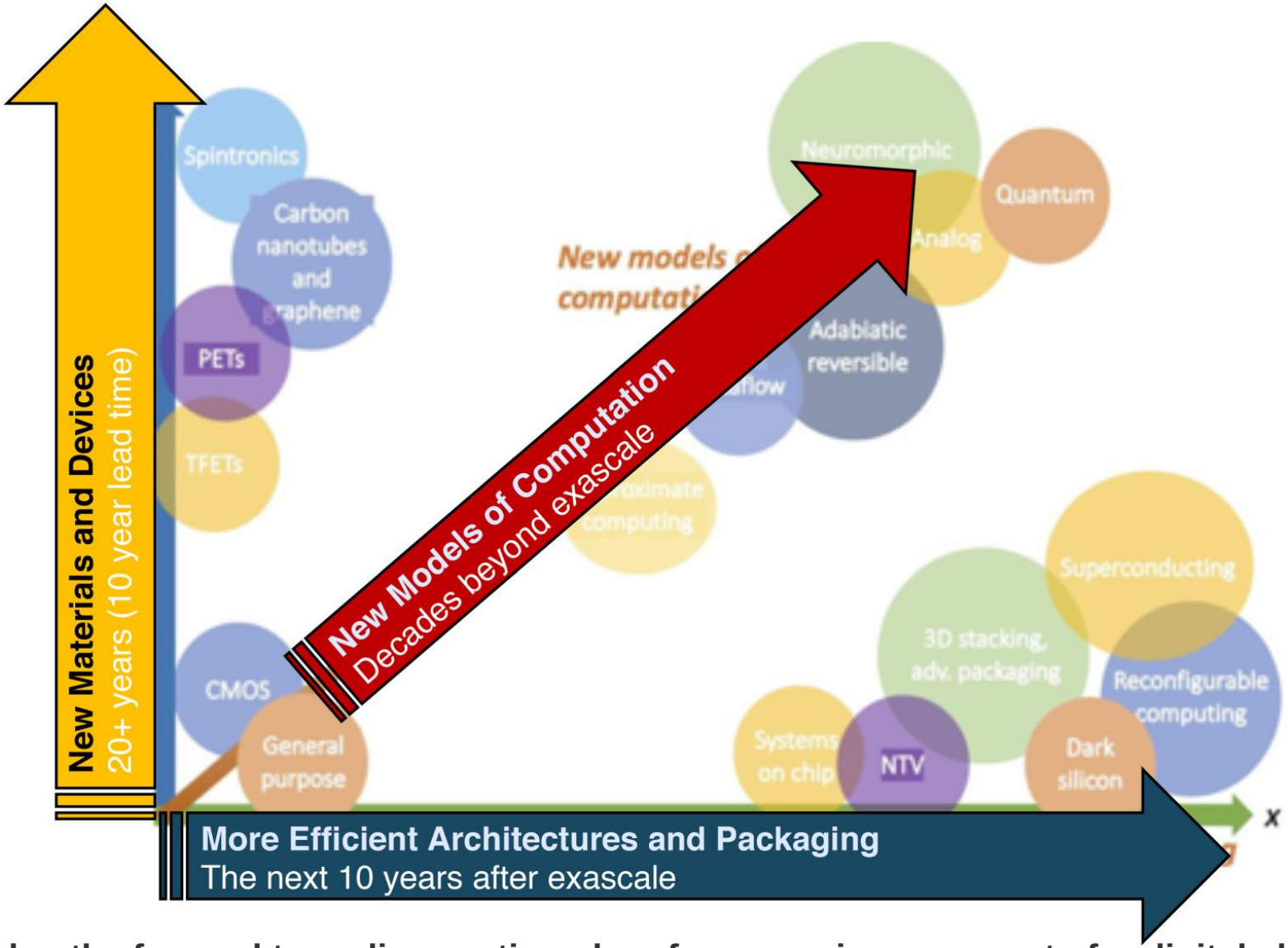
Beyond Moore's Law



Beyond Moore's Law



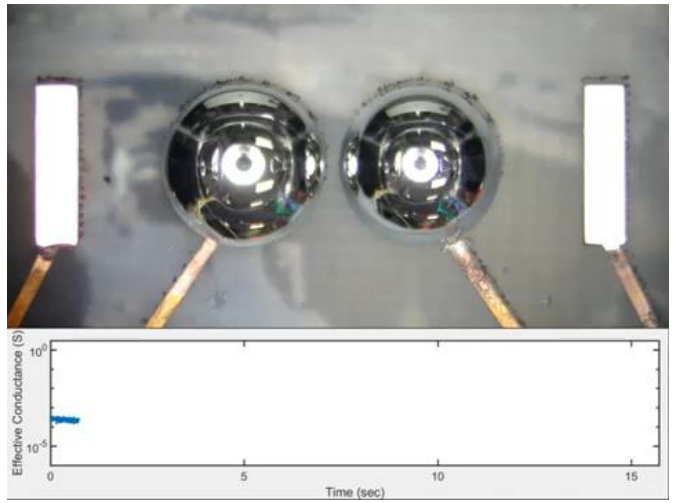
Beyond Moore's Law



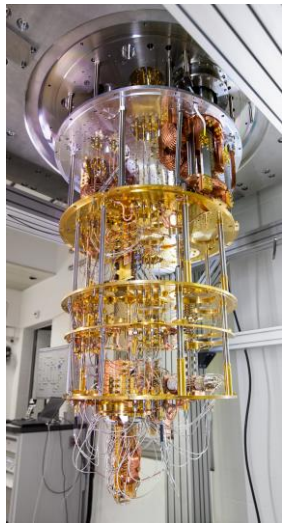
Three potential paths forward to realize continued performance improvements for digital electronics technology

What's the future? - Technologies

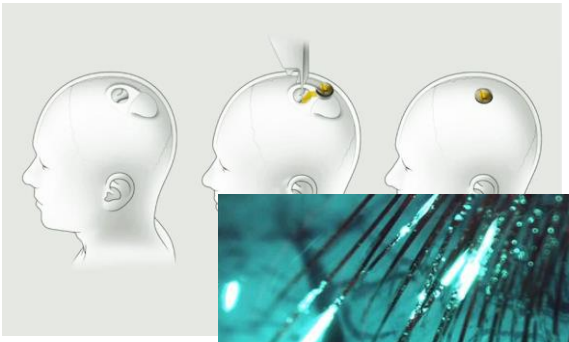
- Alternative Materials
  - Galium Nitride
- Alternative Methodology
  - Liquid Metal Transistor – Robot, Fabrics.. Etc.
  - Nanomagnetics – Ultra-low energy
- New models of Computing
  - Light Computing
  - Quantum Computing
  - Neuro copmuting

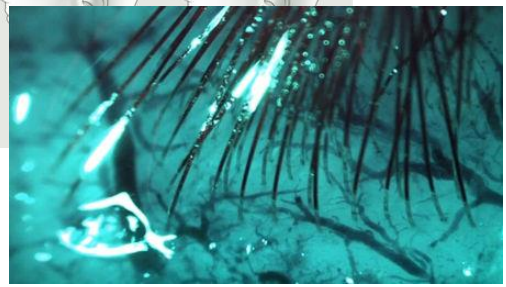


Liquid Metal Transistor (@ CMU)



Quantum computer

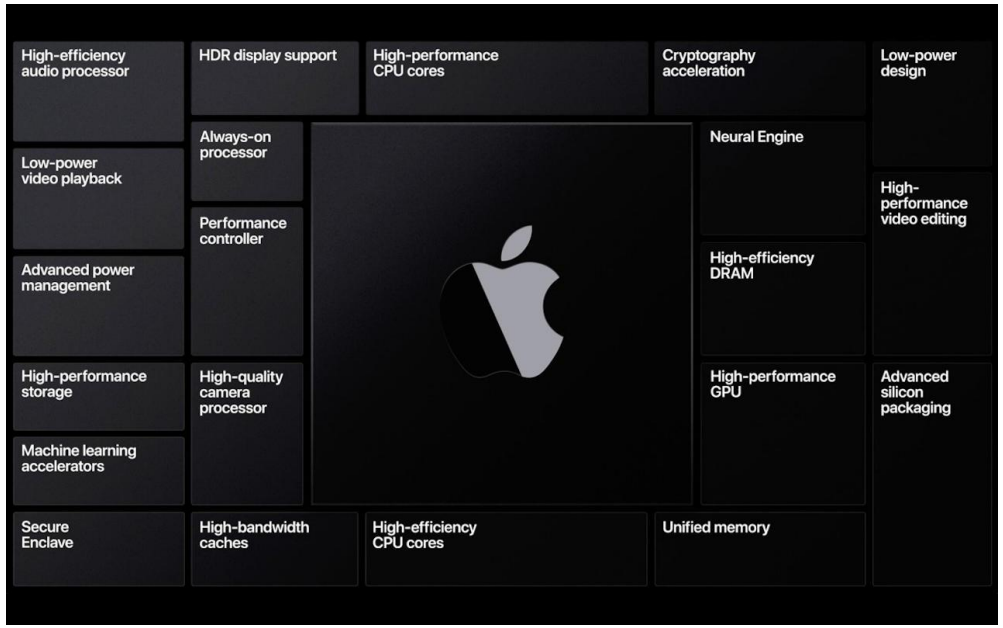




Neuro Computing (Neuralink, 2020)

What's the future? - Architecture

- *Complex Instruction Set Computer(CISC)* vs *Reduced Instruction Set Computer (RISC)*
- Fixed Instruction length in RISC
  - Pros: Fast pipelining, Low power consumption
  - Cons: Complicated compiler optimization
- No TRUE CISC processor
  - The current x86 works as RISC Internally.
  - Emulate CISC for compatibility.



Apple Silicon,
Apple announces Mac transition to Apple Silicon from CISC to RISC

What's the future? - Architecture

- Deep pipelining can solve all problems?
  - Heat problem!

Year	Microarchitecture	Pipeline stages
1993	P5 (Pentium)	5
1995	P6 (Pentium Pro/2)	14
2000	NetBurst - Willamette	20
2002	NetBurst - Northwood	20
2004	NetBurst – Prescott	31
2006	Core	14
2008	Bonnell	16
2011	Sandy Bridge	14
2013	Haswell	14
2015	Skylake	14
2016	Kabylake	14

so-called "PresHOT"

What's the future? - Hybrid

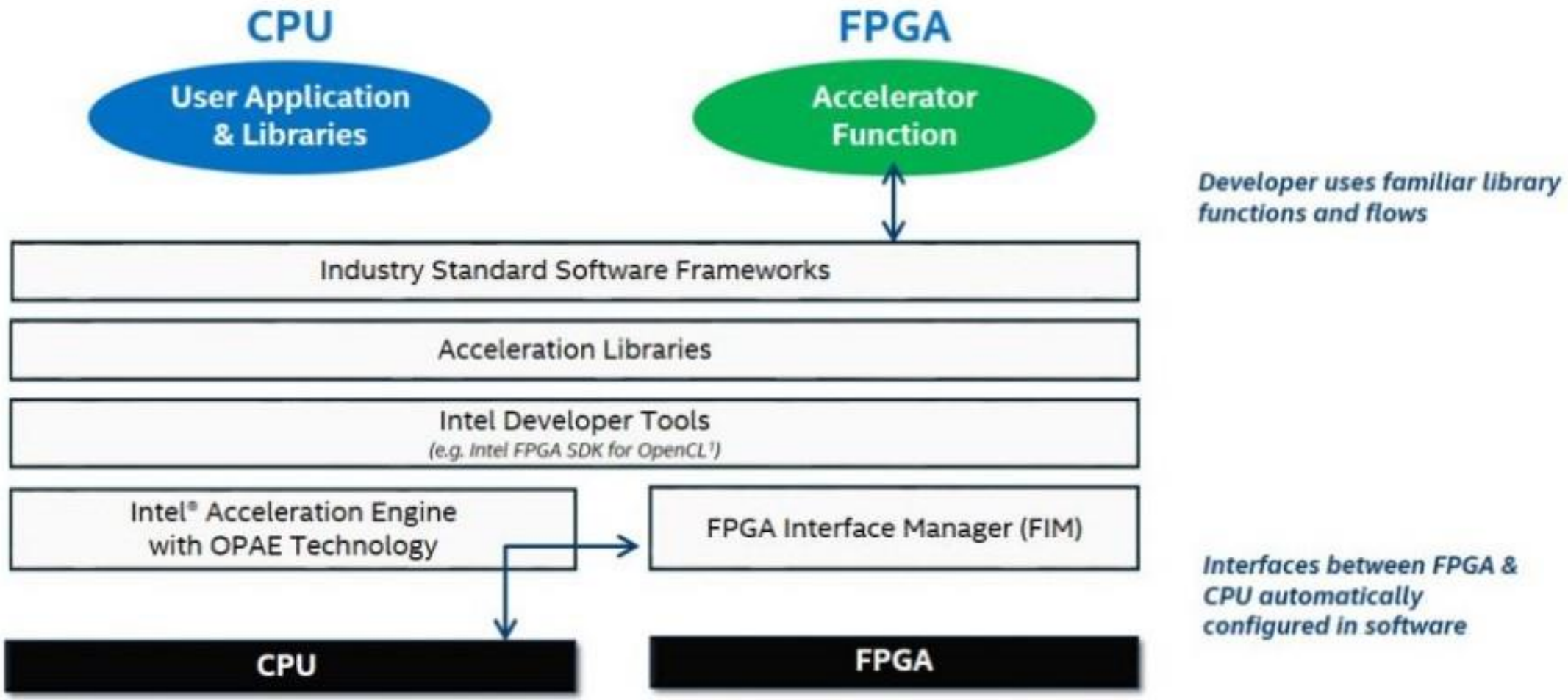
Intel acquires Altera

In June this year, Intel announced that it was acquiring FPGA maker Altera. Among the many op-eds trying to explain the rationale behind this deal, the one that resonated the most was the one by Kurt Marko (Link).

"The only way the Altera deal makes sense is if we are on the precipice of a secular shift in system design, not unlike the transition from proprietary RISC CPUs to x86, in which rapid hardware customization is the best path to faster performance. If true, the Altera deal is Intel's acknowledgement that the benefits of brute force, Moore's Law scaling have shrunk and that continuing an upward performance trajectory is more dependent on system design than semiconductor physics."

What's the future? - Hybrid

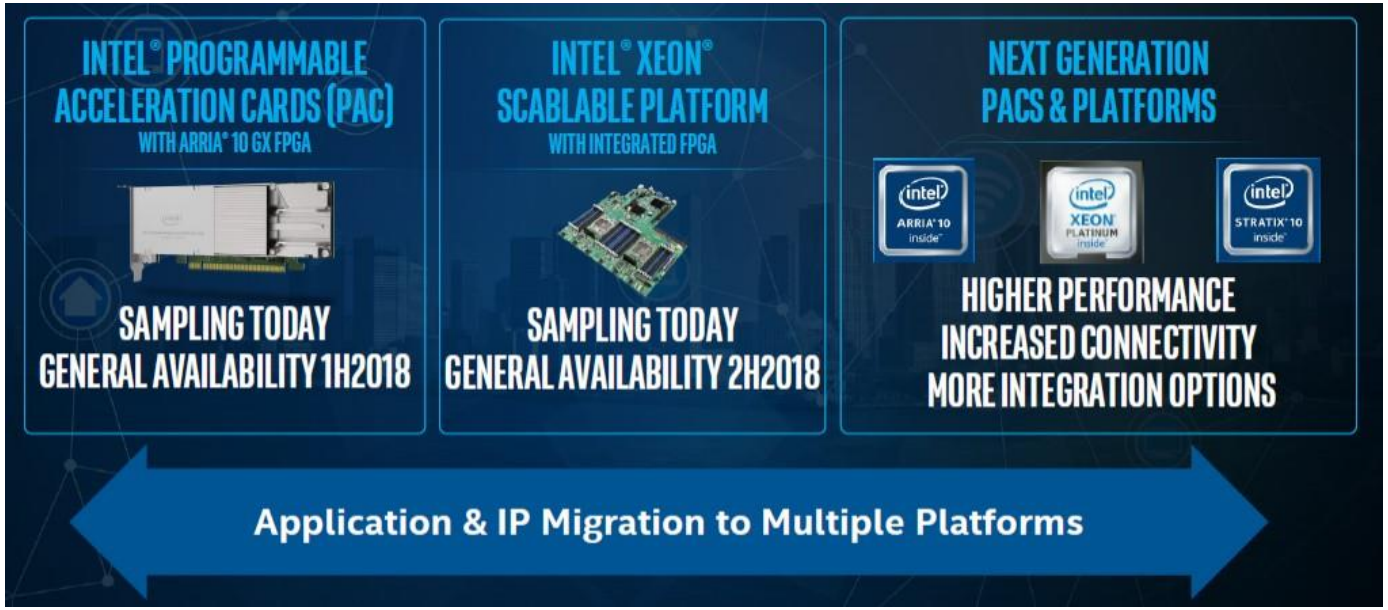
One way to extend the performance gains: Hardware Accelerator by pairing with FPGA/GP-GPU



What's the future? - Hybrid

ALTERA®

now part of Intel



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What's the future? - Hybrid