Sigma-Delta Neural Network Conversion on Loihi 2

Matthew Brehove*, Sadia Anjum Tumpa[†], Espoir Kyubwa*, Naresh Menon* Vijaykrishnan Narayanan[†]
**ChromoLogic LLC, Monrovia, CA, USA

[†]School of Electrical Engineering and Computer Science, Pennsylvania State University, University Park, PA, USA *mbrehove@chromologic.com, [†]sbt5360@psu.edu, *ekyubwa@chromologic.com, *nmenon@chromologic.com, [†]vxn9@psu.edu

Abstract—Neuromorphic computing aims to improve the efficiency of artificial neural networks by taking inspiration from biological neurons and leveraging temporal sparsity, spatial sparsity, and compute near/in memory. Although these approaches have shown efficiency gains, training these spiking neural networks (SNN) remains difficult. The original attempts at converting trained conventional analog neural networks (ANN) to SNNs used the rate of binary spikes to represent neuron activations. This required many simulation time steps per inference, which degraded efficiency. Intel's Loihi 2 is a neuromorphic platform that supports graded spikes which can be used to represent changes in neuron activation. In this work, we use Loihi 2's graded spikes to develop a method for converting ANN networks to spiking networks, which take advantage of temporal and spatial sparsity. We evaluated the performance of this network on Loihi 2 and compared it to NVIDIA's Jetson Xavier edge AI platform.

Index Terms—Neuromorphic computing, Sigma Delta Neuron, Loihi, Sparsity, Conversion

I. Introduction

The increasing demand for more energy-efficient artificial intelligence systems has spurred the development of neuromorphic computing, an approach inspired by the structure and function of biological neurons. This field aims to enhance computational efficiency by leveraging principles such as temporal sparsity, spatial sparsity, and integrating compute capabilities near or within memory units. Unlike conventional AI computing architectures, which use globally accessible memory to perform dense matrix operations, neuromorphic systems keep compute near memory and process inputs as a stream of sparse, discrete spikes routed between neurons. These spiking neural networks (SNN) can reduce unnecessary computations by only transmitting spikes when there are significant changes to their input. SNNs also minimize energy use by only communicating between neurons selectively and by keeping memory close to computation units, reducing data movement and latency.

One notable implementation of these principles in hardware is Loihi [1], Intel's neuromorphic chip designed for low-power, event-driven computations. The Loihi 2 [2] chip used in this work comprises 120 neuromorphic cores with each core supporting approximately 8k neurons. Each neuromorphic core holds its associated neuron's weights and internal state in local SRAM, enabling low-latency data storage. Loihi chips can be networked on a board to pass spikes between them and execute larger networks. Loihi 2's neurons can execute custom microcode, allowing researchers to implement

specialized neuron types tailored to specific applications. Each Loihi 2 chip is 31 mm² and is deployed on either the single-chip "Oheo Gulch" board, the 8-chip "Kapoho Point" board or the 16-chip VPX board which is used in these experiments. Built on the Intel 4 process, Loihi 2 use much less than 1 Watt per chip.

Training SNNs with binary spikes to accuracies comparable to conventional deep analog neural networks (ANN) has proven challenging, in part because the loss must be back-propagated over time [3]. In our experiments, training a spiking network takes $\sim 10\times$ the time as an ANN with the same architecture (Table I). Attempts to convert trained ANNs to SNNs have largely used the rate of spikes to represent activation values [4]. This approach requires many simulation timesteps to be executed for each input so that the spike rates of the outputs can be accurately measured. Loihi 2's ability to use quantized graded spikes opens an opportunity to convert an ANN to a quantized graded-spike SNN that takes advantage of both temporal and spatial sparsity while being easy to train. Loihi's graded spikes can hold up to 16 bit signed integer payloads which can represent quantized activations. This approach was inspired by the sigma-delta neural network (SDNN) [5]. SDNNs accept incoming spikes representing changes in the activation of the previous layer, apply learned weights, update their internal state, and then pass the change in their state to the next layer if it is larger than a given threshold. Their operation closely mirrors that of a conventional ANN neuron (Figure 1). By updating their state only when the input changes, SDNNs naturally exhibit temporal sparsity. Additionally, their selective activation of a limited subset of neurons ensures spatial sparsity, reducing power consumption, and improving resource efficiency.

Our contributions are summarized as follows:

- We propose a novel method to convert trained artificial neural networks (ANNs) into Sigma-Delta Neuron Networks (SDNNs).
- We deploy the converted network on Loihi 2, demonstrating the feasibility of running converted SDNNs on neuromorphic hardware.
- We benchmark the converted network running on Loihi 2 against the original ANN network running on a Jetson Xavier edge AI accelerator.

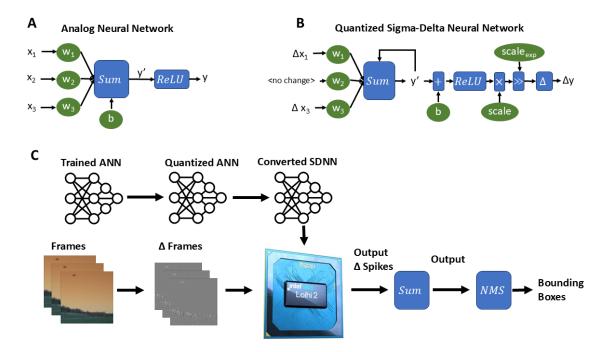


Fig. 1: In an ANN neuron (A) all of the activations from the previous layer are multiplied by their respective weights to calculate the preactivation (y'). The ReLU operation is applied to calculate the activation (y) which is sent to the next layer. For a quantized sigma-delta neuron running on Loihi (B), the changes in the previous layer activations are multiplied by quantized weights to calculate $\Delta y'$. This is then added to a running sum and passed through a ReLU operation to find y. y is then rescaled by multiplication and right-shift. If this rescaled value has changed by more than a set threshold, a spike is generated with the value of that change. This approach allows for the neuron to only perform calculation when the input of the neuron has changed, but otherwise behaves exactly like a conventional ANN neuron. (C) Overall workflow for our experiments. The quantized and converted network runs as an SDNN on Loihi. Frames are converted into sparse delta spikes, passed to Loihi, and the output spikes added to a running sum and interpreted as bounding boxes.

II. RELATED WORKS

O'Connor and Welling introduced SDNNs to reduce redundant computations by transmitting only changes in activation [5]. This temporal difference encoding allows for computational savings while maintaining network performance. Shrestha et al. [6] implemented an SDNN on Intel's Loihi 2 and benchmarked its performance against an NVIDIA Jetson platform. Their work demonstrated the potential advantages of neuromorphic hardware for SDNNs by taking advantage of Loihi 2's event-driven processing. However, their approach relied on SLAYER [7], a training framework designed for binary spiking networks. SLAYER requires the entire time series to be stored in memory during training. We found that this makes SDNN training more difficult and slower than conventional ANN training. Yousefzadeh et al. developed a method for converting ANNs to SDNNs [8], but this method still relied on binary spikes and was not compatible with modern model quantization approaches. In contrast, our approach can convert ANN networks trained and quantized with conventional pytorch tools to SDNNs capable of being deployed on Intel's Loihi 2 neuromorphic hardware.

III. METHODOLOGY

A. Conversion and Loihi Implementation

Loihi 2's neurocores are only capable of integer arithmetic. so the network needs to be quantized. Instead of developing our own quantization approach, we aimed to make our ANN-SDNN conversion method compatible with standard quantization schemes. We started with PyTorch's post-training static quantization [9] which converts the weights (w) and activations (x) from floating-point (FP32) to 8-bit integer (w_a , x_a), while biases (b) were maintained in FP32. The quantization used an affine mapping defined by a floating-point scale (s) and an integer zero-point (z) for each tensor $x_{float} = s \times (x_q - z)$ for activations and similarly for weights $w_{float} = w \times (w_q - z)$. In PyTorch, the matrix multiplication is performed in integer arithmetic and the resulting integer accumulator is rescaled and combined with the FP32 bias before being re-quantized for processing by the next layer. The effective floating-point computation performed is: $y_{floati,k} = k \sum (x_{q,ik} - z_x) \times$ $(w_{q,jk}-z_w)\times(s_x\times s_w)+b_{float,j}$.

For deployment on Loihi 2, direct application of the floating-point scales is not possible. The version of the sigmadelta neuron microcode developed by Intel only allows rescal-

ing by powers of two (bit-shifts). To maintain compatibility with the PyTorch quantization scales, we needed to modify the sigma-delta neuron microcode. We extracted the per-layer input scale (s_x) , weight scale (s_w) , and output scale (s_y) from the quantized PyTorch model using custom python code. The necessary rescaling factor for a layer, $R = s_y \times s_x \times s_w$, was then implemented in the Loihi microcode using fixed-point arithmetic. Specifically, the 24-bit accumulated pre-activation value within the neuron was multiplied by a pre-computed 24bit integer scaling factor (scale) derived from R, and subsequently right-shifted by a pre-computed exponent (scale_exp) to approximate the division by s_y . The loihi microcode then implemented $y = (accumulator \times scale) >> scale_exp$ to ensure the result remained within an 8-bit range for the next layer's input, preventing overflow in the next layer's 24-bit accumulator. The bias was similarly rescaled during conversion and added to the accumulator before scaling. This method was inspired by Jacob et all [10]. The full redesigned microcode is shown in pseudocode in Algorithm 1.

Our method deploys the converted model on Loihi using an initial delta layer executing on the CPU to produce graded delta spikes from a sequence of RBG frames [0, 255] where $spike_i = frame_i - frame_{i-1}$. The spikes are passed to Lava processes running on Loihi 2 which implement the convolution operation and the sigma-delta neurons. The resulting spikes are received from Loihi and added to a running sum to calculate output activations. These output activation frames were then dequantized using the final layer scaling factor from the quantized PyTorch model. These floating point outputs are interpreted as a YOLOv3-style grid of 14 × 14 cells each with associated x-y locations and probability scores for each of the 3 bounding boxes (Figure 1C). We used the Lava extension for Loihi to deploy the model. Intel has recently released a new lower-level interface for Loihi called nxkernel that may provide additional latency improvements, but our implementation was not complete at the time of publication.

Algorithm 1: New Microcode Logic

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\begin{array}{l} y' \leftarrow y' + \Delta x \cdot w_q \; ; \qquad // \; \text{Accumulate input} \\ \text{delta} \\ y \leftarrow \text{ReLU}(y' + bias) \\ y \leftarrow (y \times scale) \gg scale_{exp} \\ \Delta y \leftarrow y - y_{ref} \\ \text{if } |\Delta y| > v_{th} \; \text{then} \\ | \; \text{Emit Spike}(\Delta y) \\ | \; y_{ref} \leftarrow y \end{array}
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B. Dataset

We chose drone-detection in video as the test application for our SDNN networks because these videos contain few moving objects and therefore have high temporal sparsity. We used the multi-sensor drone detection dataset [11] which includes 285 RGB videos, which have a resolution of 640×512 . We resized all input frames to fit the network input size of 448×448 . The dataset features four manually labeled classes of flying objects:

drones, airplanes, helicopters, and birds. The sensor-to-target distance for drones ranged from 20 to 200 meters, and all video acquisitions were performed under daylight conditions. The videos were divided into training and test sets with 20% reserved for testing.

C. Model and Training

The model architecture (YOLO-KP) was developed by Intel and based on the YOLO v3-Tiny architecture [12]. It was adapted to accommodate Loihi's memory and architectural constraints. The most important consideration for Loihi is minimizing the number of neurons. Each Loihi core can hold only a fixed number of neurons as each requires designated dendrite and axon resources. Therefore, higher resolution and deeper networks require more Loihi chips which in turn consume more power. For this reason, max-pooling layers were replaced by strided convolutions for spatial down-sampling. Residual layers were similarly removed to reduce memory requirements and eliminate the need to synchronize spikes arriving from different layers. These removals greatly simplified the implementation. The model is defined in the lavanc/lava-dl repository on github. [13] and served as the basis for other works benchmarking video object detection tasks on Loihi [14].

To work around Loihi's size and connectivity limitations, we first trained a teacher model based on MobileNetV2 [15] on the same dataset. For knowledge distillation, we employed a masked L2 feature matching loss to align the penultimate layer representations between the teacher (MobileNetV2) and student (YOLO-KP) models. This feature distillation loss was combined with the standard detection loss using a weighting coefficient $\alpha = 0.069$, allowing the student network to simultaneously optimize for detection performance while mimicking the richer feature representations learned by the teacher model. The model hyper-parameters were tuned using the optuna package over 20 training runs. We used the albumentations package for data augmentation and trained for 30 epochs. We used the Adam optimizer and a Reduce-on-plateau learning rate schedule. This model was quantized with the PyTorch quantization libraries using 8-bit per-tensor quantization and the HistogramObserver and MinMaxObserver for the activations and weights respectively.

D. Accuracy-Sparsity Tradeoff Exploration

SDNNs have the inherent advantage of being able to adjust the level of sparsity by setting the threshold level for changes to be passed to the next layer. When the thresholds are set to zero, the cumulative output exactly matches the quantized network. When thresholds are raised above zero for some layers, only larger changes are passed through the network. This decreases the number of spikes and the number of synaptic operations needed to execute the network while sacrificing accuracy that exists in the original quantized ANN. In order to explore this tradeoff, we raised the threshold from 0 to 1 in the first *N* layers of the 10-layer network starting from the initial delta layer. This gave us a spectrum from the minimum

sparsity and highest accuracy to higher sparsity and lower accuracy (Fig 2).

E. Benchmarking Loihi

Our experiments were run on an in-house Loihi VPX development board containing 16 Loihi chips and associated IO electronics and connected by 1 and 10 Gigabit Ethernet for control and data respectively. In order to measure the power and latency of the Loihi board, we used Lava Loihi's (v0.7) built in profiling probes that report the power usage, timing, and core-level activity measurements. These probes have limited memory capacity and only 300 frames were used to measure power and the duration of each SDNN simulation time step. The probes measured static and total power. Following the format of Shrestha et al. [6], we report static, dynamic, and total power. Static power is calculated only from the chips that were used by the network. Since 5 chips out of 16 were used for this network we reported static power measurement as 5/16 of the measured static power. The dynamic power was calculated as the measured total power minus measured static power. The reported total power is the sum of the adjusted static power and the dynamic power.

Since spikes are passed from one layer to the next during each simulation time step and our network has 10 layers, the latency of the network was reported as $10\times$ the average measured simulation time step. The frames per second (FPS) is reported as the inverse of this simulation time step since one frame is passed to the network and received from it each time step.

Since integrated circuit design can generally trade speed for energy-efficiency, the energy-delay product (EDP) is used as a measure of overall efficiency of an integrated circuit [16]. The EDP reported here is calculated as $power \times timestep \times latency$. Measurements of the accuracy of Loihi were performed separately by running the entire test set through the Loihi board, saving the output spikes, and then evaluating the accuracy after the run. In order to better understand how IO impacts the execution speed of Loihi in our applications, we loaded 15 frames into on-chip memory and replayed these 10,000 times in order to measure power and latency in the absence of any IO bottlenecks (Figure 3). This approach for reporting power, latency, and EDP is consistent with Intel's recommended reporting structure for Loihi benchmarks [6].

F. Benchmarking NVIDIA Jetson

To compare our results on Loihi with conventional approaches, we ran the same network as an 16-bit floating point ANN on an NVIDIA Jetson Xavier edge AI board using the TensorRT library. The tegrastats tool provided by NVIDIA was used for power measurement and the VDD_CPU_GPU_CV and VDD_SOC power channels were combined to estimate the total power used for network execution. It should be noted that tegrastats on Xavier was not capable of measuring the power used solely by the GPU. Therefore, the comparison between the Xavier and Loihi is not an identical comparison since we report only the power used by the Loihi chip but

TABLE I: Performance comparison of our ANN training approach to Intel's SLAYER training approach [7] in terms of training time and accuracy (mean average precision). See details in section IV(B).

Model	Time per Epoch (min)	Completion Time (hrs)	Memory	mAP
SLAYER	55	45.80	9.4G	0.37
ANN Training	5	3.40	8.6G	0.62

must report the power used by the whole system-on-chip (SOC) in the case of the Xavier. This choice was made to be consistent with Intel's comparisons to a similar Jetson device [6]. In order to temporally separate execution on the GPU from preprocessing steps performed on the CPUs, the initialization and preprocessing was performed first and then execution was paused then restarted before network using TensorRT. The network was run with a batch size of 1 inside a python for-loop without the system GUI running.

IV. RESULTS

A. Model Accuracy

The MobileNetV2 teacher model achieved a mean-average precision (mAP) of 0.72, while our knowledge-distilled student model (YOLO-KP) reached a higher mAP of 0.74. This performance improvement is notable considering that YOLO-KP without knowledge distillation never exceeded 0.6 mAP in our experiments. The comparable parameter count between YOLO-KP and MobileNetV2 likely contributed to the student model's ability to effectively leverage the teacher's representations. After quantization, the accuracy decreased modestly to 0.62 mAP. These results were calculated across our complete test set of 58 videos containing 18,214 frames. For context, the authors of the multi-sensor drone dataset reported mAP values ranging from 0.58 to 0.84 depending on target distance when using a larger, full-precision model [11].

B. SLAYER Training Comparisons

In order to compare the our ANN-SDNN conversion approach with Intel's SLAYER training algorithm, we trained a SDNN network with the same architecture on the same Multi-Sensor Drone Detection Dataset. Training was conducted for 50 epochs with a batch size of 16, a starting learning rate of 2×10^{-5} was used with a learning rate scheduler of factor 0.1. The results (Table I) highlight significant improvements in both training efficiency and performance of our conversion approach. Our quantized model achieves higher mAP (0.69 vs 0.37) demonstrating better detection accuracy than SLAYER. Additionally, ANN training only took 5 minutes per epoch compared to 55 minutes for SLAYER on our NVIDIA GTX 4090. The conversion process only added 30 seconds for post-training quantization.

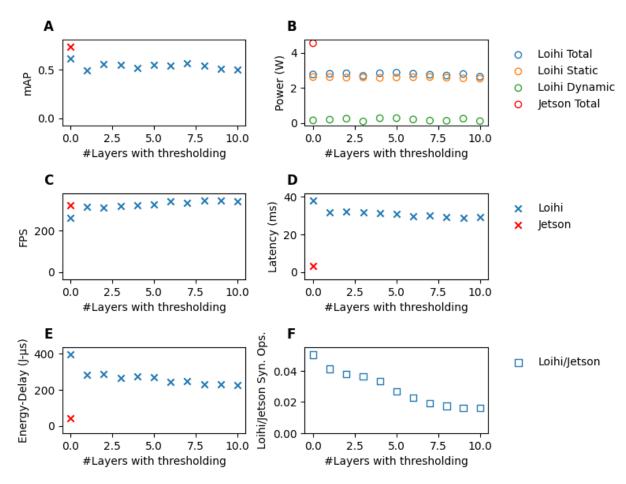


Fig. 2: Results from the model as run on the Jetson Xavier in full precision and as a SDNN on Loihi. Along the x-axis of each plot we vary the number of layers in the 10-layer network that have thresholds raised to 1 to increase sparsity. (A) Mean average precision. (B) Power usage. (C) Frames per second. (D) Time between input and corresponding output. (E) Energy-delay product $(J-\mu s)$ (F) Ratio of the Loihi synaptic operations per frame and the number of multiply accumulate operations performed per frame in the ANN network on the Jetson Xavier. As expected, increasing the thresholds dropped the accuracy, increased the speed, and reduced the number of operations performed.

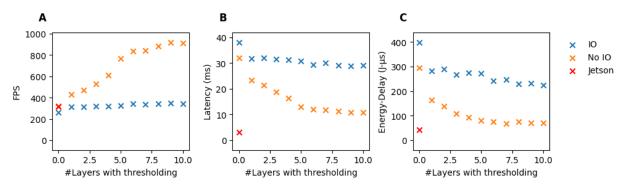


Fig. 3: Results from the model as run on Loihi with and without off-board IO with a varying number of layers with thresholds set to 1 to adjust sparsity. Input spikes were loaded into Loihi memory so that the model could run without off-board communication.

C. Power, Latency, and Throughput

The results from the Loihi activity probes showed that the SDNN had 0.056 of the synaptic operations as the ANN network and that, as expected, this ratio decreased as the

number of layers with thresholds >1 increased. The increased sparsity improved the throughput from 275 FPS to 341 FPS. The total power usage was lower for Loihi compared to the Jetson and remained relatively consistent for all experiments

TABLE II: PilotNet [6] and YOLO-KP model comparison

	PilotNet	YOLO-KP
Type	Conv/FC	Conv
Application	Angle Pred.	Obj. Detection
Parameters	0.35M	3.4M
Neurons	12K	2M
Loihi Chips	1	5

as it is dominated by static draw. The model running on Loihi executes a single time step in 3.63 ms and uses 10.4 mJ of energy of which 0.55 mJ is dynamic energy. The throughput and latency are somewhat worse than the Jetson Xavier which processes an entire frame in 3.1 ms and uses 14 mJ of energy (Figure 2). For the unbottlenecked trials that avoided using IO, the speed increased to 3.2 ms per timestep and used 8.86 mJ of energy per inference (Figure 3).

D. Comparison with Intel's published work

Intel has recently published a study that compares an SDNN run on Loihi 2 with the same network run on an NVIDA Jetson Orin Nano accelerator [6] which is similar to our Jetson Xavier. The network they tested (PilotNet) aimed to predict the steering wheel angle of a driving car based on dashcam footage taken during driving. The network had far lower input resolution ($66 \times 200 \times 3$) and a single-dimension of output (steering angle). It was therefore able to be run on a single Loihi 2 chip. The YOLO-KP model, had much larger input $(448 \times 448 \times 3)$ and output $(14 \times 14 \times 27)$ dimensions requiring 5 networked Loihi chips to execute. Since the power is dominated by static draw, the larger network requires proportionally more power to run. Inter-chip communication also increases execution time which in turn increases energy per frame. The fully-convolutional architecture of YOLO-KP required 3.4M parameters compared to PilotNet's 0.35M which used 5 convolution layers followed by 3 fully-connected layers. Model comparisons are shown in Table II. To compare the two studies we show the ratio of the Loihi result to the Jetson result for each study with and without IO in Table III. In each category (Energy, Latency, Throughput, and EDP), our results show less advantage over Jetson than for Loihi's PilotNet. This is particularly true for the no-IO case where PilotNet shows a 0.000872× reduction in EDP vs Jetson and YOLO-KP shows a 6.44× increase in EDP vs Jetson.

V. DISCUSSION

We were successfully able to train an ANN network to process videos in a drone detection task, quantize the network, and deploy it as an SDNN on Loihi 2. The deployed network was able to take advantage of a $> 17\times$ improvement in sparsity compared to the original ANN (Figure 2F) and used less power and energy per frame than the NVIDA Jetson Xavier. However, we found that the latency, throughput, and EDP were worse on Loihi, though they improved with higher thresholds. While the latency and throughput improved when IO bottlenecks were removed and the thresholds were increased, the EDP remained

worse on Loihi as compared with the Jetson. In comparing the two platforms, we note that one of the key design choices of Loihi is the use of SRAM for all weights and activations in the network. This dramatically reduces memory access times, but results in a large static power draw which increases with the number of Loihi chips used so that higher resolution inputs require more static power draw. Even if compilation and IO improvements are implemented to decrease the execution time of these networks on Loihi, traditional frame-based cameras may not fully leverage Loihi's asynchronous eventdriven architecture. Event-based cameras, with their nearcontinuous temporal resolution and inherent sparsity, could provide a more natural pairing with neuromorphic hardware like Loihi, potentially unlocking greater efficiency advantages for video analysis tasks. This complementary hardware approach may explain why lower resolution videos have shown more favorable comparisons with conventional accelerators [6]. Additionally, a larger single Loihi chip could offer the key benefit of reducing costly inter-chip communications making spiking networks more attractive. Currently, multichip Loihi networks are not as competitive with single-chip embedded GPUs.

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TABLE III: Ratio of Loihi's performance to Jetson's performance in our study with the YOLO-KP model running with thresholds of zero and Intel's previously published work [12] with PilotNet.

Model	Platform	Energy/frame (mJ \downarrow)	Latency (ms \downarrow)	Throughput (FPS \uparrow)	EDP $(nJs \downarrow)$
YOLO-KP	Loihi	10.4	36.3	275	379
YOLO-KP	Loihi no IO	8.86	31.8	314	282
YOLO-KP	Jetson Xavier	14.1	3.11	322	43.8
PilotNet	Loihi	1.26	65.4	137	82.5
PilotNet	Loihi no IO	0.09	1.21	7403	0.11
PilotNet	Jetson Nano	21.9	5.77	173	126
		Energy Ratio(↓)	Latency Ratio(↓)	Throughput Ratio(†)	EDP Ratio (↓)
YOLO-KP		0.74	11.7	0.855	8.65
YOLO-KP (no IO)		0.628	10.3	0.975	6.44
PilotNet		0.057	11.3	0.795	0.654
PilotNet (no IO)		0.0041	0.210	42.7	0.000872

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