Scalable Disk-Based Approximate Nearest Neighbor Search with Page-Aligned Graph

Dingyi Kang$^\alpha$, Dongming Jiang$^\alpha$, Hanshen Yang$^\beta$, Hang Liu$^\beta$ and Bingzhe Li$^\alpha$
$^\alpha$University of Texas at Dallas
$^\beta$Rutgers University

Abstract

Approximate Nearest Neighbor Search (ANNS), as the core of vector databases (VectorDBs), has become widely used in modern AI and ML systems, powering applications from information retrieval to bio-informatics. While graph-based ANNS methods achieve high query efficiency, their scalability is constrained by the available host memory. Recent disk-based ANNS approaches mitigate memory usage by offloading data to Solid-State Drives (SSDs). However, they still suffer from issues such as long I/O traversal path, misalignment with storage I/O granularity, and high in-memory indexing overhead, leading to significant I/O latency and ultimately limiting scalability for large-scale vector search.

In this paper, we propose PageANN, a disk-based approximate nearest neighbor search (ANNS) framework designed for high performance and scalability. PageANN introduces a page-node graph structure that aligns logical graph nodes with physical SSD pages, thereby shortening I/O traversal paths and reducing I/O operations. Specifically, similar vectors are clustered into page nodes, and a co-designed disk data layout leverages this structure with a merging technique to store only representative vectors and topology information, avoiding unnecessary reads. To further improve efficiency, we design a memory management strategy that combines lightweight indexing with coordinated memory–disk data allocation, maximizing host memory utilization while minimizing query latency and storage overhead. Experimental results show that PageANN significantly outperforms state-of-the-art (SOTA) disk-based ANNS methods, achieving 1.85x–10.83x higher throughput and 51.7%–91.9% lower latency across different datasets and memory budgets, while maintaining comparable high recall accuracy.

1 Introduction

Approximate Nearest Neighbor Search (ANNS), as the core of vector databases (VectorDBs), is a transformative technology that enables the extraction of meaning from massive datasets. ANNS is widely applied in domains such as machine learning [2, 5, 7, 8, 11, 14, 20, 21, 25, 26, 29, 39, 44, 53, 54, 58] and bioinformatics [6, 41], where the ability to efficiently identify data points most similar to a query drive key advancements. Recently, graph-based ANNS approaches [9, 15, 16, 28, 33, 34] have gained popularity due to their high query efficiency, achieved through fast graph traversal strategies. However, as
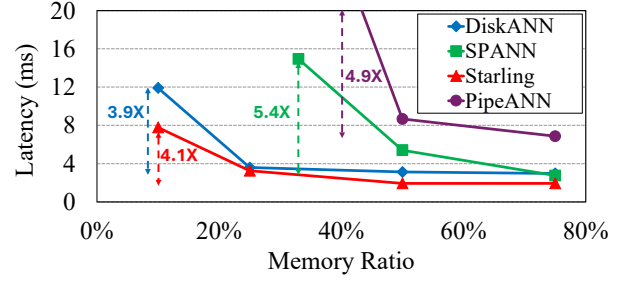

Figure 1. Impact of memory ratio on query latency for state-of-the-art disk-based ANN schemes (i.e., DiskANN [43], SPANN [10], Starling [49], and PipeANN [19]) on the SIFT dataset. The memory ratio represents the proportion of the dataset size that is available in host memory. (Due to the minimum memory requirement, PipeANN and SPANN cannot run with the memory ratio below 30%.)

vector datasets scale up (e.g., billions of vectors [16, 27, 50]), these methods face scalability challenges, since both the vectors and their associated indexes may not be fully stored in host memory.

To address this scalability challenge in large-scale vector search, disk-based graph ANNS solutions have been developed [10, 19, 36, 37, 43, 49]. These methods offload the data to disk and load it into memory only when needed, thereby reducing memory consumption. For example, the pioneer work DiskANN [43] store both the full vectors and the graph index on SSDs while retaining compressed vector representations in memory. During search, only the original vectors and the neighbor information along the search path are loaded from disk into memory. Subsequent studies such as SPANN [10], Starting [49], and PipeANN [19] adopt similar designs to further improve query efficiency for large-scale ANN search. However, these methods still face significant I/O latency, particularly under constrained host memory. Moreover, as datasets continue to scale, such approaches encounter persistent scalability bottlenecks.

As shown in Figure 1, existing schemes achieve relatively low query latencies when sufficient memory is available. However, as the available memory decreases, latencies increase significantly. For example, reducing the memory ratio from 50% to 10% can result in more than a threefold increase in latency. In some cases, such as SPANN and PipeANN, a minimum memory threshold is required for execution

(e.g., SPANN cannot operate with a memory ratio below 30%). Moreover, with higher memory ratio, the performance of those schemes are saturated. These observations underscore the scalability limitations of current disk-based ANN schemes as the size of vector datasets continues to grow.

To analyze the limitations of state-of-the-art (SOTA) disk-based ANN schemes, we identify three primary issues: **(1) Long I/O traversal path:** As the number of vectors grows, the corresponding graph expands significantly. Although graph algorithms such as Vamana [43] can reduce graph diameter and the average number of query hops, fewer search hops do not necessarily translate to reduced I/Os. **(2) Misalignment with storage I/O granularity:** During the search process, each step typically requires reading only a small amount of data (e.g., one or a few vectors per SSD page). However, SSDs must read entire pages to fulfill these requests. The misalignment between graph node size and SSD I/O granularity leads to wasted I/O bandwidth and underutilized reads. **(3) High in-memory indexing overhead:** Although SOTA disk-based ANN methods reduce memory usage by offloading part of the search data to disk, they still reserve substantial memory for essential data structures (e.g., compressed vector data for distance calculation or graph index for fast routing). For large-scale datasets, this memory requirement remains prohibitively high, limiting both applicability and scalability.

Given these limitations, we aim to enhance the scalability of disk-based ANN systems by developing a new vector indexing structure and reconstructing the data layout in storage. However, several critical questions must be addressed: *(1) What kind of graph structure can be designed to shorten the graph traversal paths and reduce I/O operations?* The gap between theoretical graph hops and the actual number of I/O operations must be bridged to improve overall query performance. *(2) How can the vector data layout in storage be reconstructed to align with I/O granularity?* While some prior work addresses vector locality by grouping them into a single SSD page, further improvements require jointly considering graph topology and vector data placement to optimize I/O performance. *(3) What in-memory indexing structure can balance both performance and scalability?* Existing methods often incur substantial memory overhead for storing index data or compressed vectors to accelerate queries. Therefore, a new indexing structure must be co-designed with the system to simultaneously achieve high performance and scalability.

To address these challenges, we propose PageANN, a framework that enables efficient large-scale ANN search under various memory budgets while maintaining high recall accuracy. The key innovation is a page-node graph structure for query search, which differs from prior vector-based graphs that treat each vector as an individual node in graphs. The page-node graph bridges the gap between theoretical hop counts and the number of read I/Os by aligning each logical page node with a physical SSD page. To construct this graph, we design a new algorithm that groups similar vectors into logical page nodes and leverages only representative vectors to establish connections with neighboring pages, ensuring both accuracy and efficiency.

Second, we design a new SSD data layout that cooperates with the page-node graph to optimize query processing. Each logical page node in the graph is allocated to a physical SSD page, and only representative vectors from neighboring pages are selected, to form inter-page connections. We incorporate a merging mechanism within each physical page to remove redundant data, resulting in storing more data and accelerating the search process. Additionally, each SSD page embeds its own topology information (i.e., neighbor IDs and their compressed values), eliminating the need for extra reads during query execution.

Lastly, we propose a new lightweight index that quickly routes incoming queries to page nodes near the target, reducing the length of the search path. Moreover, a memory-disk coordination strategy that determines search-related data stored in disk or memory based on the available memory budget. This combined approach improves the performance of disk-based ANN systems while maintaining low memory overhead and high scalability.

In summary, we develop the PageANN framework, comprising around 6K lines of code, and release it as open source[1]. Compared to other SOTA schemes, PageANN achieves from 1.85x to 10.83x higher throughput and reduces latency by 51.7% to 91.9% across datasets and memory budgets, while maintaining the same high recall accuracy.

The remainder of this paper is organized as follows: Section 2 presents the background and motivation for ANN. Section 3 discuss the specific motivation for this work. Section 4 introduces the the overall architecture of PageANN and its algorithms. Section 5 details its implementation. Section 6 shows the experimental results. Related work is given in Section 7. Finally, conclusions are drawn in Section 8.

2 Background

In this section, we present the background and basics of nearest neighbor search, and introduce SOTA disk-based graph ANNS schemes.

2.1 Nearest Neighbor Search

In the nearest neighbor search (NNS) problem in high dimensional spaces, data points are represented as d-dimensional vectors in $\mathbb{R}^d$, and the Euclidean distance is typically used as the distance metric. Throughout this paper, we use the terms *points* and *vectors* interchangeably. The Euclidean distance between two data points p and q is denoted as $\|p - q\|_2$.

Given a dataset $X = \{x_1, x_2, \ldots, x_n\}$, the k-nearest neighbor (kNN) search for a query point q is defined as finding a subset $k\text{NN}(q) \subseteq X$ such that:

- $|k\text{NN}(q)| = k$, and
- $\forall x \in k\text{NN}(q), \forall x' \in X \setminus k\text{NN}(q), \|x - q\|_2 \leq \|x' - q\|_2$.

However, in high-dimensional spaces, the computational cost of exact nearest neighbor search becomes prohibitively expensive due to the curse of dimensionality [23]. Consequently, research has increasingly focused on approximate nearest neighbor search (ANNS) methods, which trade a small amount of accuracy for substantial gains in efficiency.

Let the result returned by an ANNS algorithm be R, where $|R| = k$. The quality of R is commonly evaluated using recall@k, defined as:

$$\text{Recall@k} = \frac{|R \cap k\text{NN}(q)|}{k}.$$

2.2 Graph-based ANNS

Unlike tree-based methods [4, 17, 42] and hashing-based methods [12, 18, 22, 23, 30–32, 45, 47], which suffer from severe performance degradation and scalability issues as datasets grow, graph-based ANNS approaches [9, 15, 16, 28, 33, 34] have emerged as one of the most effective solutions for large-scale search in high-dimensional spaces, providing both high efficiency and accuracy.

In graph-based ANNS, vector data are represented as nodes connected to their nearest neighbors under a distance metric, forming a sparse yet well-connected topology that enables efficient navigation. The search begins from one or more entry points and iteratively progresses toward closer neighbors until a stopping condition is met, after which the top-k closest nodes are returned. By limiting distance computations to small local neighborhoods at each step, graph-based ANNS greatly reduces computational overhead. Moreover, by traversing proximity-based connections between data points, these methods effectively alleviate the curse of dimensionality and avoid boundary issues that commonly affect partitioning- and hashing-based approaches.

Although graph-based ANNS methods achieve excellent speed and accuracy, they often incur scalability issue due to substantial memory overhead. To address this issue, a range of disk-based graph ANNS solutions has been proposed [10, 19, 36, 37, 43, 49], which reduce memory consumption by offloading data to disk while striving to maintain high search performance. For example, DiskANN[43], Starling[49], and PipeANN[19] store original vectors and graph topology on SSDs while retaining only product quantization (PQ)−compressed vectors in memory. In contrast, SPANN[10] keeps the graph index entirely in memory and offloads only the vector data to SSDs, performing graph traversal in memory and issuing I/O requests only after traversal completes.

3 Motivation

Although existing disk-based solutions alleviate some issues in graph-based ANNS, they still suffer from severe search
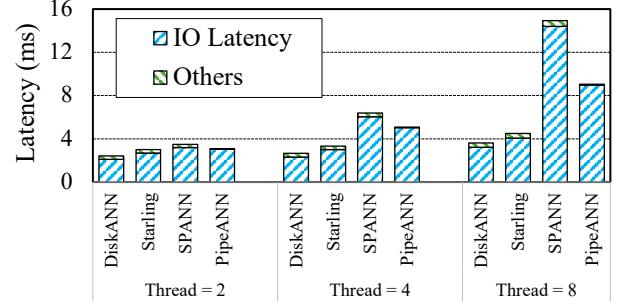

Figure 2. Query latency breakdown analysis for SOTA schemes.

Table 1. Read amplification of SOTA Disk-based ANN schemes.

Scheme\Dataset	SIFT100M	SPACEV100M	DEEP100M
DiskANN	18.29	20.08	8.00
Starling	1.71	1.95	1.28
PipeANN	18.29	20.08	8.00
SPANN	2.0	2.0	2.0

latency and scalability limitations. As shown in Figure 1, SOTA disk-based ANN experience scalability issues, particularly under limited host memory, where query latency can increase more than threefold compared to a sufficient memory configuration (e.g., 40% memory ratio). Furthermore, our analysis of performance bottlenecks, illustrated in Figure 2, shows that I/O latency accounts for over 90% of the total query latency across all schemes. Based on these observations, we identify the following reasons for the low scalability and performance of the SOTA schemes.

Long I/O graph traversal path. SOTA disk-based graph ANNS methods suffer from high I/O latency, primarily due to long traversal paths on disk during query processing. Each hop along the path triggers a batch of I/O read requests, which accumulate into substantial overhead as the search progresses. With increasing dataset size, the average length of search path grows, leading to more disk seeks and cache misses. As a result, query performance is constrained by I/O bottlenecks rather than computation, posing a significant challenge for large-scale deployments. Although Vamana graph construction [43] aims to reduce graph diameter (i.e., the maximum number of hops between any two nodes), such reductions in theoretical hops do not necessarily translate into fewer I/O operations. In fact, suboptimal data layouts can further prolong I/O traversal paths due to a mismatch between logical graph hops and actual storage accesses.

Misalignment of storage IO granularity. Another major source of excessive I/O latency is the mismatch between storage I/O granularity and the size of individual vectors.
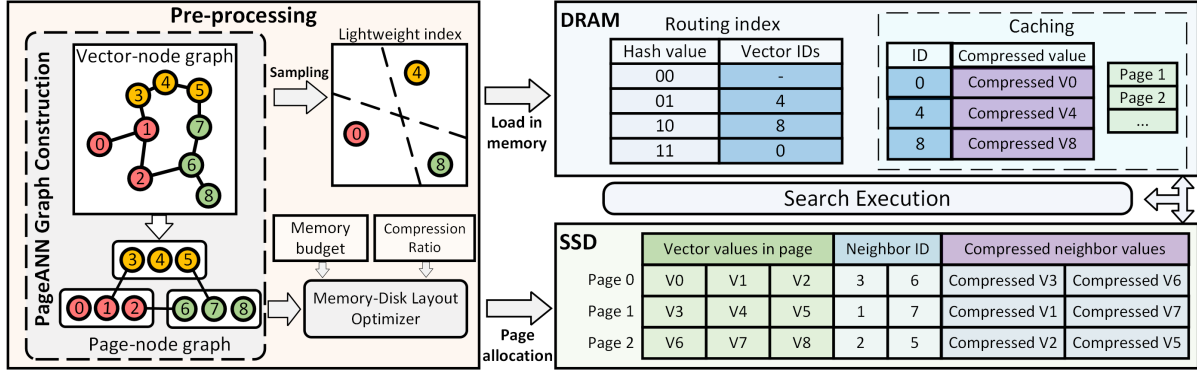
Figure 3. Overall structure of PageANN.

Even if the theoretical minimum graph size reduces the upper bound on I/O operations (i.e., the number of hops equals to the number of I/Os), the data in SSD pages may not be fully utilized due to misalignment between page granularity and graph node size, resulting in suboptimal latency. Modern SSDs typically enforce a minimum read unit of one page (often 4 KB or larger), which is significantly larger than a single vector (e.g., 128 bytes in the SIFT dataset [1]). Prior work has attempted to mitigate this problem by clustering similar nodes into the same page to reduce read amplification. However, the irregular structure of graphs and the unpredictable nature of query paths make it difficult to ensure that all data within a page are relevant and useful. Consequently, state-of-the-art schemes inevitably incur wasted reads during query processing. For example, as shown in Table 1, on the SIFT dataset [1] with an average graph degree of 24, existing methods exhibit read amplification from 1.28 to 20.8 during search. Therefore, efficiently addressing this misalignment is critical for eliminating read amplification and further reducing I/O cost.

Large in-memory indexing overhead. Although state-of-the-art disk-based schemes claim to offload data to storage to improve the scalability of ANN systems, they still require a substantial amount of memory for compressed data or indexing structures. For example, SPANN reserves more than 30% of the dataset size in memory for graph indexing. Below this threshold, it cannot operate reliably. DiskANN and Starling store compressed vector data in memory to accelerate queries. While they can operate with as little as 10% of the dataset size in memory, this comes with trade-offs: either reduced accuracy due to lossy compression or significantly increased latency caused by longer traversal paths needed to maintain accuracy. In summary, despite their claims of scalability through disk offloading, current disk-based systems remain constrained by substantial memory requirements, resulting in high latency or limited scalability.
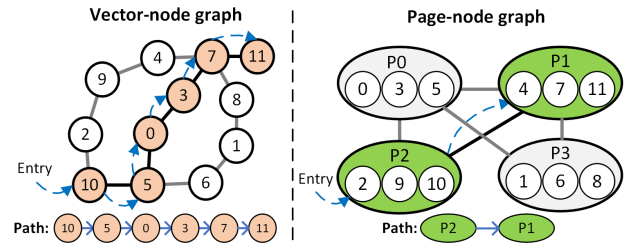

Figure 4. Main idea of page-node graph.

4 PageANN Design

In this section, we present the design of PageANN with a page-node graph structure that coordinates the logical graph with the physical characteristics of storage to accelerate query search and improve system scalability. As illustrated in Figure 3, PageANN operates in two major stages: pre-processing and query processing. In the pre-processing stage, vectors are organized into a page-node graph. Based on the available memory budget and a predefined compression ratio, the system determines the amount of compressed data to be allocated in memory. A lightweight index is also constructed to enable efficient query routing. In the query processing stage, the combination of caching and lightweight indexing enables fast traversal of the graph. A new disk layout is employed to support the page-node graph structure and to reduce I/O operations for subsequent disk-resident graph retrievals. The following subsections detail the specific design considerations for each component.

4.1 Page-Node Graph Construction in PageANN

The main idea of page-node graph in PageANN is to shift the granularity of the index graph from individual vectors to page nodes, aligning the graph structure with the I/O granularity of storage systems. As shown in Figure 4, this page-node graph preserves essential relationship between vectors while substantially reducing the overall graph size. However,

Algorithm 1 Page-Node Graph Construction

Require: Vector-based graph G_0; page-node capacity n; hop parameter h for candidate selection;

Ensure: Page-node graph stored on SSD, where each page contains its vectors and neighbors

1: $P \leftarrow$ empty list of pages
2: $UngroupedVectors \leftarrow$ all vectors in G_0
3: **while** $UngroupedVectors \neq \emptyset$ **do**
4:     $v \leftarrow UngroupedVectors.extract()$; $p \leftarrow [v]$
5:     $C \leftarrow G_0.ungroupedNbrsWithinHops(v, h)$
6:     $V \leftarrow$ top $(n - 1)$ closest vectors to v from C
7:     $p.append(V)$
8:     $UngroupedVectors.remove(V)$
9:     **while** $|p| < n$ and $UngroupedVectors \neq \emptyset$ **do**
10:         $p.append(UngroupedVectors.extract())$
11:     **end while**
12:     $P.append(p)$
13: **end while**
14: **for all** page $p \in P$ **do**
15:     $PageVecs \leftarrow$ empty list
16:     $PageNbrs \leftarrow$ empty set
17:     **for all** vector $v \in p$ **do**
18:         $PageVecs.append(G_0.getValue(v))$
19:         **for all** neighbor $u \in G_0.getNbrs(v)$ **do**
20:             **if** $u \notin p$ **then**
21:                 $PageNbrs.insert(u)$
22:             **end if**
23:         **end for**
24:     **end for**
25:     $writeIntoSSDPage(PageVecs, PageNbrs)$
26: **end for**

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designing such a graph introduces two key challenges. *(1) Translating reduced traversal paths in the graph into reduced I/O.* Shorter traversal paths in the graph do not necessarily lead to fewer I/O operations if the graph structure is not coordinated with storage characteristics. Consequently, the design must consider both the logical properties of the graph and the constraints of SSD hardware, as well as the intended search process. *(2) How should a page node be represented in the graph?* Each page node contains multiple vectors, and constructing meaningful neighbor connections is non-trivial. Using too few representative vectors to represent a page node (e.g., a single proxy vector for all vectors in a page) risks missing true neighbors due to poor coverage of the intra-page distribution. Using too many representatives can lead to redundant edges, increasing both search cost and storage overhead.

To address these challenges, we propose a topology-guided construction scheme that derives the page-node graph from a high-quality vector-based graph, as shown in Algorithm 1. We start with the Vamana graph [43], known for producing low-diameter, high-quality graphs, though our method is
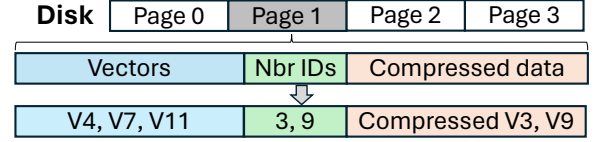

Figure 5. Disk layout of PageANN based on the graph example in Figure 4.

modular and can use any disk-friendly graph construction algorithm. As illustrated in Lines 1-13 of Algorithm 1, vectors are first grouped into page-nodes by clustering vectors with their $n - 1$ nearest neighbors within h hops, where n is the target page-node capacity and h is a tunable parameter. Once grouped, the external neighbors of each page node are determined by aggregating the vector-level edges from all its constituent vectors to vectors in other page nodes, removing intra-node edges, and merging duplicate connections to the same external neighbors (Lines 14-26). This preserves the essential connectivity of the original graph while eliminating redundancy.

The page-node graph offers three main advantages: (1) Aligning graph nodes with physical SSD pages maximizes the utility of each page read, reducing I/O operations during search. This alignment increases the effective search space per I/O read, thereby effectively shortening the search path. (2) Connections are derived from the vector-level graph, preserving the full descriptive power of the original vector relationships without incurring significant space overhead. (3) Merging and avoiding redundant edges (i.e., merging edges connecting to the same neighbors and removing internal connections within one page) reduces storage overhead, enabling more search-relevant data to fit within one page.

4.2 A New Disk Layout Supporting Page-node Graph

To fully leverage the benefits of the page-node graph and translate reduced traversal paths into lower I/O overhead, PageANN adopts a new data layout in storage that aligns the page-node abstraction with SSD access characteristics. This design also introduces an additional field that reduces the number of next-hop nodes to fetch, further decreasing I/O requests. As shown in Figure 5, each SSD page contains three major fields: (i) the vector values stored in the page, used for computing the actual distances to the query; (ii) the neighbor IDs, representing the topology of the page-node graph; and (iii) the compressed vectors of page neighbors, used for determining the next hops in the search.

First, as discussed earlier, reducing the number of graph traversal hops alone does not directly translate into fewer I/O requests. To bridge this gap, PageANN maps each page node to exactly one physical SSD page, ensuring that each visited graph node corresponds to a single SSD page read. This mapping allows the entire page data to be fully utilized.

In traditional disk-based graph search, the system reads the target node and its neighbor IDs, then issues separate I/O requests to fetch each neighbor for distance computation. In large-scale graphs, where a node may have tens or even hundreds of neighbors, this can result in excessive I/O. To address this, PageANN stores compressed neighbor vectors directly alongside their IDs within the same page, enabling next-hop computations to be performed entirely based on the current page without accessing additional pages.

Moreover, to ensure that all data associated with a page node fits into a single SSD page (typically 4KB, 8KB, or larger), PageANN determines the number of vectors per page node using the following equation:

$$N_{\text{nodes}} = \frac{S_{\text{page}} - 2 \cdot S_{\text{num\_nbrs}} - S_{\text{nbrID}} \cdot N_{\text{nbrs}} + S_{\text{CV}} \cdot N_{\text{CV}}}{D \cdot S_{\text{dtype}}}$$

where S_{page} denotes the page size; $S_{\text{num\_nbrs}}$ refers to the size of the variable used to store the total number of neighbors; S_{nbrID} is the size of each neighbor ID; N_{nbrs} is the total number of page neighbors; S_{CV} is the size of a compressed vector; N_{CV} is the number of neighbors with compressed vectors on disk; D is the vector dimension, and S_{dtype} is the size of the vector data type.

Based on the memory budget and S_{CV}, we can conservatively estimate the number of compressed values (N_{CV}) to be stored per page. To save space and accommodate more vectors per page, the system keeps only one copy of each compressed vector across memory and disk. This design not only optimizes SSD page usage but also reduces I/O during search. Further details on memory–disk coordination are provided in the following subsection.

4.3 PageANN Memory Management

To improve the scalability of ANNS while maintaining fast query processing, PageANN manages host memory through two components: lightweight indexing and caching with memory–disk cooperation. The lightweight index quickly routes incoming queries to page nodes near the target, reducing the length of the search path. The remaining memory stores compressed vector data and page node, enabling further path determination without accessing storage. Based on the available memory budget, the scheme decides which search-related data to keep in memory, ensuring full utilization of memory resources for optimal performance.

Caching for fast lightweight indexing. PageANN leverages a memory space to maintain a data caching to support a fast routing procedure. Given a memory budget, PageANN samples a subset of vectors and projects each onto randomly generated hyperplanes defined by a projection matrix. The sign of each projection is encoded as a bit, and the resulting bit sequence forms a binary hash code. Sampled vectors' IDs are assigned to hash buckets based on these codes. The Hamming distance between hash codes approximates vector similarity, allowing rapid identification of candidates near the

query. When additional memory is available, selected page nodes are stored in the caching area. First, PageANN performs a warm-up phase on a dataset to identify the most frequently visited nodes. Within the available budget, PageANN caches the corresponding page nodes for faster retrieval.

This approach offers key advantages: (1) reduced search length by narrowing the search space and providing closer candidates, thereby lowering the average number of hops in the subsequent graph traversal; (2) memory efficiency with lower overhead, since the hash table avoids repeatedly storing the same sampled vector IDs as in graph-based indexing methods.; and (3) fast computation with constant-time generation of query hash codes, bucket retrieval, and vector ID access.

Memory-disk coordination. PageANN balances the available memory budget with storage space overhead. As described in Section 4.2, each page node stores compressed neighbor data so that the next step in the search path can be determined directly from the current page. However, embedding these compressed neighbors within a page consumes storage space, reducing the number of vectors that can fit in that page. If this space were instead allocated to vectors, more vectors could be stored per page, further reducing the page-node graph size and thereby improving search efficiency. To leverage this trade-off, PageANN coordinates memory and disk to support the use of high-quality compressed vectors and to maximize the number of vectors stored per page within the given memory budget. This strategy further reduces the size of the page-node graph and amplifies the performance gains from fewer I/O operations.

The memory-disk coordination in PageANN balances accuracy, performance, and storage efficiency according to the available memory budget. (1) Under severely constrained memory conditions, all moderately compressed neighbor values are stored on the same SSD page as their associated page node, with merging and pruning eliminating redundancy and freeing space to accommodate necessary values without significant disk overhead. (2) With moderate memory budgets, PageANN employs a hybrid configuration where some compressed neighbor values are kept in memory while the rest remain on SSDs, enabling higher-accuracy data usage within budget constraints. (3) When memory is sufficient, all compressed neighbor values are stored in memory, and the freed disk space is reallocated to increase the number of vectors per page node, thereby reducing graph size, shortening traversal paths, and minimizing I/O operations to maximize retrieval efficiency.

4.4 PageANN Graph Search

Unlike traditional graphs that traverse from vector to vector, PageANN searches by traversing from page to page. To execute the search, PageANN maintains two key data structures: a candidate set, which stores the top-L vectors closest to the query based on compressed representations, and a result set,
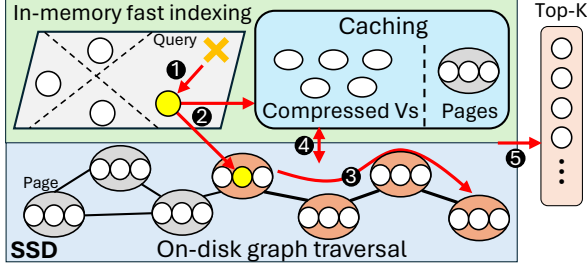
Figure 6. PageANN graph search process.

which holds the IDs of visited vectors along with their full-coordinate distances to the query. The search process unfolds in two phases: an in-memory routing phase followed by an on-disk graph traversal phase as detailed in Algorithm 2.

In-memory routing process. As shown in Figure 6, upon receiving a query, PageANN computes its binary hash and identifies all hash buckets within a small Hamming radius r (①). The vector IDs contained in these buckets are then retrieved, and their approximate distances to the query are estimated using in-memory compressed representations. As shown in Lines 4-7 of Algorithm 2, these vector IDs, along with their estimated distances, are inserted into the candidate set, which serves as the set of entry points for subsequent traversal of the page-node graph in disk.

Page-node graph traversal. As shown in Lines 11-19 of Algorithm 2, at each hop of the graph traversal, the algorithm selects the closest unvisited vectors from the candidate set, determines their SSD page IDs, and marks them as visited until no unvisited vectors remain in the candidate set. To avoid redundant I/Os, vectors located in the pages that have already been visited or are scheduled for reading are skipped. The collected page IDs are then used to issue batched I/O requests for the corresponding SSD pages.

The target page node will be either read from caching memory or from SSD if it is not in memory (②). Using the retrieved data, the next target page node is determined based on the stored topology and the compressed neighbor vectors contained in the SSD page (③). During this process, if the required data already reside in memory, PageANN directly accesses and utilizes them without additional retrieval I/O overhead (④). Also, the true distances between the query and all vectors in each page are computed and added to the result set along with their vector IDs, while the estimated distances between the query and each page's neighbor vectors are calculated and added to the candidate set along with the neighbors' IDs (Lines 20–27 in Algorithm 2) (⑤). This expansion process continues iteratively until no unvisited vectors remain in the candidate set. Finally, the result set is sorted by true distance, and the IDs of the top-k closest vectors to the query are returned.

Algorithm 2 PageANN Graph Search

Require: In-memory hash table H, routing search radius r, page-node graph G, query q, I/O batch size b
Ensure: Top-k nearest neighbors of q
1: $C \leftarrow$ empty heap ▷ Candidate set, a fixed-size min-heap
2: $V \leftarrow$ empty set ▷ Set of IDs of visited pages
3: $R \leftarrow$ empty set ▷ Result set
4: $E \leftarrow H.getAllVectorIDs(q, r)$ ▷ Retrieve entry vector IDs within Hamming radius r
5: **for all** $v \in E$ **do**
6:     $C \leftarrow C \cup \{(v, Estimated\_distance(v, q))\}$
7: **end for**
8: **while** C contains unvisited vectors **do**
9:     $P \leftarrow$ empty list ▷ Pages to read in this batch
10:     **while** C contains unvisited vectors **and** $|P| < b$ **do**
11:        $v \leftarrow$ closest unvisited vector in C
12:        $v.visited \leftarrow$ true
13:        $p\_ID \leftarrow calculate\_pageID(v)$
14:        **if** $p\_ID \notin V$ **then**
15:           $V \leftarrow V \cup \{p\_ID\}$
16:           $P \leftarrow P \cup \{p\_ID\}$
17:        **end if**
18:     **end while**
19:     $pages\_ready \leftarrow batchReadPagesFromSSD(P)$
20:     **for all** page $p \in pages\_ready$ **do**
21:        **for all** $v \in p.vectors$ **do**
22:           $R \leftarrow R \cup \{(v, exact\_distance(v, q))\}$
23:        **end for**
24:        **for all** $n \in p.neighbors$ **do**
25:           $C \leftarrow C \cup \{(n, estimated\_distance(b, q))\}$
26:        **end for**
27:     **end for**
28: **end while**
29: $sortAscendingByDistance(R)$
30: **return** Top-k vectors from R

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5 Implementation

PageANN is implemented in C++ with roughly 6K lines of code and can be deployed under diverse memory budgets, enabling efficient search over large-scale datasets.

Vector ID reassignment and data layout. After constructing the page-node graph, each vector ID is reassigned according to its page-node index and its offset within that page node. A mapping between the original and reassigned vector IDs is maintained to update all neighbor references accordingly during pre-processing stage. Each page node is then written to its corresponding SSD page using the `std::ofstream` APIs.

An I/O-computation pipeline. We implement a pipeline that overlaps primary computation with I/O latency by leveraging Linux AIO (Asynchronous I/O) commands such as `io_submit` and `io_getevents`. A pre-allocated buffer is used

to temporarily store vector data from loaded pages. When an asynchronous read completes, the vectors of the corresponding page are placed into the buffer without performing immediate distance computations. Instead, these computations are deferred and executed during the idle wait period of the next pending asynchronous I/O request.

Memory management for routing and caching. Based on the available memory budget, three main data structures are maintained in memory. First, a contiguous array stores the cached compressed vector values, along with a hash table that maps vector IDs to their corresponding indices in the array. Second, a hash table maps hash codes to the IDs of sampled vectors within their respective subspaces. Third, another contiguous array stores the contents of cached pages, accompanied by a hash table that maps cached page-node IDs to their indices in the array. To reduce the memory overhead of large hash tables, we employ `tsl::sparse_map`, which achieves high memory efficiency at the cost of a slight reduction in access speed.

6 Evaluation

In this section, we evaluates the performance of PageANN against SOTA disk-based ANN schemes under various workloads and memory budgets.

6.1 Experimental Setup

Hardware configuration. The experiments are conducted on a workstation running Ubuntu 24.04 under WSL2 with an Intel Core i9-14900K CPU (4.3 GHz, 24 cores), 64 GB DDR4 RAM RAM, and a 2 TB NVMe SSD.

Baselines. We compare PageANN with four SOTA disk-based ANNS methods including DiskANN [43], SPANN [10], Starling [49], and PipeANN [19].

Datasets. Those schemes are compared on five representative benchmark datasets covering diverse scales and vector dimensionalities: SIFT100M [24], SPACEV100M [35], DEEP-100M [3], SIFT1B [24], and SPACEV1B [35], as shown in Table 2.

Evaluation metrics. We evaluate and report the following key metrics: Recall@10 represents the fraction of the true 10 nearest neighbors retrieved in the top-10 results. Query latency indicates the average per-query processing time in millisecond (ms). Throughput refers to the number of queries processed per second under concurrent load (QPS).

Parameters. For a fair comparison, all systems are configured to operate under the same hardware, dataset, and index construction parameters, ensuring identical disk usage and in-memory footprint. Specifically, for DiskANN, Starling, PipeANN, and PageANN, we use the same parameters for average vector degree, vector compression ratio, candidate pool size during construction, and number of vectors per page. During search, the batch size of I/O read requests is fixed at 5, and the number of query threads is fixed at 16

Table 2. Characteristics of datasets.

Dataset	# of vectors	Dimension	Type	# of queries
SIFT100M [24]	100M	128	uint8	10000
SPACEV100M [35]	100M	100	int8	29316
DEEP100M [3]	100M	96	float	10000
SIFT1B [24]	1B	128	uint8	10000
SPACEV1B [35]	1B	100	int8	29316

across all datasets. SPANN follows the SPFresh [52] configuration, with two modifications: (i) the number of vector duplications is tuned to match the disk overhead of other systems, and (ii) the head selection ratio is adjusted to ensure a comparable in-memory index size.

6.2 Overall Performance

100M-scale results. First, we evaluate the overall performance of all schemes under a memory budget of approximately 30% of the dataset size on three million-scale datasets. Figure 7 shows query latency versus recall@10 across the 100-million–scale datasets. PageANN consistently achieves the lowest latency across the entire recall range compared to all baselines. The gap becomes more pronounced at higher recall levels (e.g., Recall@10 = 0.95), where competing methods require substantially larger search lists and consequently incur higher I/O overhead. For example, on SPACEV100M, PageANN achieves an average query latency of 12 ms, whereas Starling and DiskANN exceed 25 ms and 31 ms, respectively.

The throughput results, shown in Figure 8, lead to a similar conclusion. At Recall@10 = 0.9, PageANN achieves 2.50× higher throughput than DiskANN on SIFT100M, 2.21× higher than Starling, 4.35× higher than PipeANN, and 7× higher than SPANN. Similar margins are observed on SPACEV100M and DEEP100M. As recall increases, competing systems suffer sharp throughput drops due to longer search lists and higher I/O latency. In contrast, PageANN maintains stable performance through page-level traversal and a co-located layout, which together reduce the number of I/O operations.

Table 3 further confirms these findings. At Recall@10 = 0.9, PageANN achieves 46.0% fewer I/O operations, 54.7% lower latency, and more than 85.4% higher throughput than the second-best SOTA scheme. Overall, these results demonstrate that under fair memory budgets (30% of dataset size), PageANN consistently outperforms competing systems, which either consume more memory (e.g., SPANN, PipeANN) or exhibit significantly higher latency.

Billion-scale results. We further evaluate PageANN on SIFT1B and SPACEV1B, compared against DiskANN and PipeANN. Other baselines are excluded as their construction or search phase exceeds the memory capacity of our setup. Both PageANN and DiskANN are evaluated with a memory budget of approximately 20% of the dataset size. For PipeANN, we follow the setup provided in its open-source Github repository, which requires a memory ratio greater than 20%. As shown
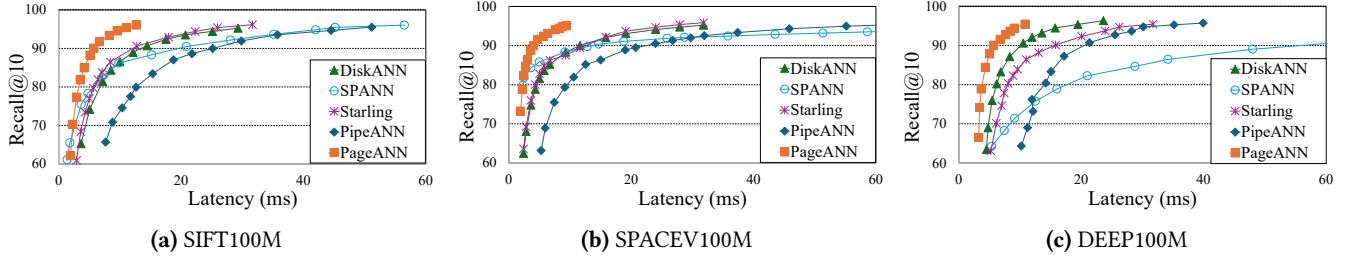
Figure 7. The query latency vs. Recall@10 with the memory ratio of 30% for all schemes on million-scale datasets.
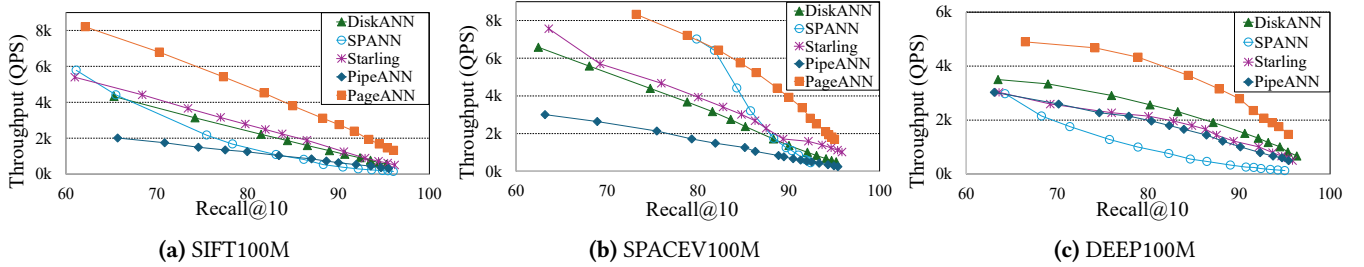

Figure 8. The query throughput vs. Recall@10 with the memory ratio of 30% for all schemes on million-scale datasets.

Table 3. The comparison of throughput, latency and average I/Os at Recall@10 = 0.9 with the memory ratio of 30%.

| Scheme\Dataset	SIFT100M			SPACE100M			DEEP100M		
	Throughput (QPS)	Latency (ms)	Mean I/Os	Throughput (QPS)	Latency (ms)	Mean I/Os	Throughput (QPS)	Latency (ms)	Mean I/Os
DiskANN [43]	1099.62	14.45	187.43	1369.51	11.62	141.13	1511.31	10.50	135.32
SPANN [10]	383.40	20.86	299.61	1089.56	14.68	96.84	257.51	62.22	296.96
Starling [49]	1246.94	12.75	157.79	1677.33	9.49	114.53	1008.23	15.80	189.08
PipeANN [19]	632.16	25.16	168.51	662.73	14.19	154.47	734.33	23.98	139.52
PageANN (ours)	**2749.36**	**5.78**	**85.14**	**3918.03**	**4.05**	**59.93**	**2788.73**	**5.07**	**83.94**

in Figure 9, PageANN consistently achieves substantially higher throughput and lower latency across the entire recall spectrum. On SIFT1B (Figure 9a) and SPACEV1B (Figure 9b), at Recall@10 = 0.9, PageANN delivers up to 1.9×–3.8× higher throughput, 48%–71% lower latency. At Recall@10 = 0.95, the advantage widens: PageANN achieves 2.2×–7.5× higher throughput, 55%–87% lower latency. These results demonstrate PageANN's robustness and scalability on billion-scale datasets, where existing methods incur significant I/O bottlenecks and degraded efficiency.

### 6.3 Impact of Available Memory on Performance

We examine the impact of available memory (expressed as the memory ratio, i.e., memory budget normalized by dataset size) on the performance of all schemes.

Performance sensitivity to memory budget. Figure 10 examines how performance responds as varying memory budget from around 0% to 30% of the dataset size (i.e., memory ratio). PageANN consistently outperforms all baselines across datasets under different memory ratios. PageANN sustains high throughput and low latency across all settings:

relative to the 30% configuration, throughput decreases by only 8.7% at 20% memory ratio and 15.2% at 10% memory ratio, with latency increasing only marginally. In contrast, most baselines exhibit sharp performance degradation as memory decreases. DiskANN and PipeANN both suffer significant throughput drops to below 20% of their original values, while SPANN fails to execute reliably when the memory budget falls below 30% memory ratio. These results illustrate the high stability of PageANN under diverse memory scenarios. **Minimum memory requirement for high recall.** The minimum memory required by each system to achieve high recall accuracy is also investigated. Table 4 reports the smallest memory footprint needed to reach Recall@10 = 0.9 on SIFT100M. PageANN achieves the target accuracy and latency with only 0.05 GB (0.05% of the dataset size), whereas competing systems demand orders of magnitude more memory. Remarkably, even at a memory ratio of around 0%, PageANN delivers substantially better performance than state-of-the-art baselines running with a 10% memory ratio.
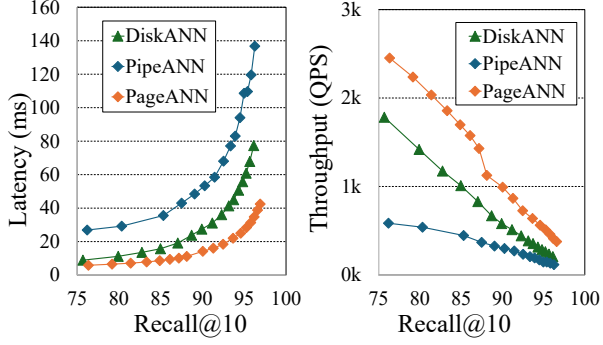
(a) SIFT1B
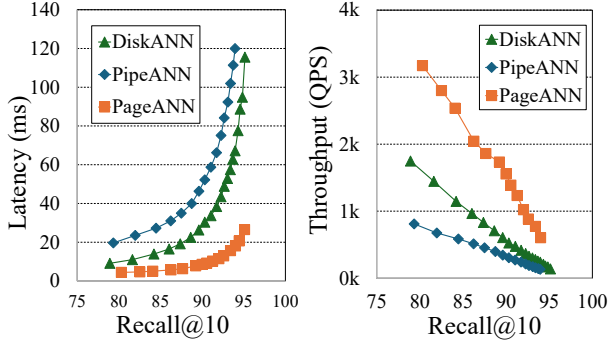
(b) SPACEV1B

Figure 9. Latency and throughput comparison of DiskANN, PipeANN and PageANN on billion-scale datasets (SIFT1B and SPACEV1B).
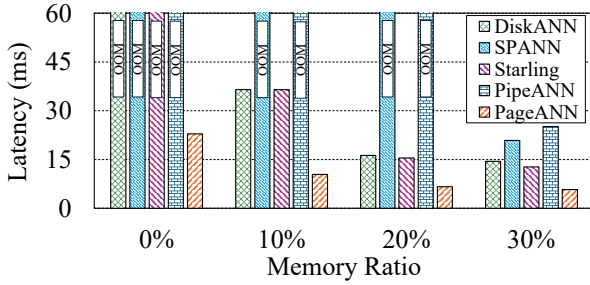

Figure 10. Latency vs. memory ratio from 0% (around 0.05%) to 30% on SIFT100M across different schemes. The label "OOM" means a scheme runs out of memory and cannot operate under the corresponding memory budget.

Table 4. Minimum memory size (GB) on SIFT100M to achieve Recall@10 = 0.9.

Method	DiskANN	SPANN	Starling	PipeANN	PageANN
Min. Size	1.2	3.2	1.2	5.4	**0.05**

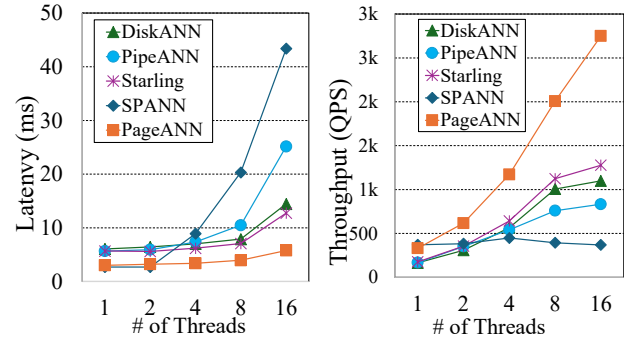**Performance of PageANN under varying memory ratio.**
As shown in Figure 11, the latency and throughput performance of PageANN improves significantly as the memory
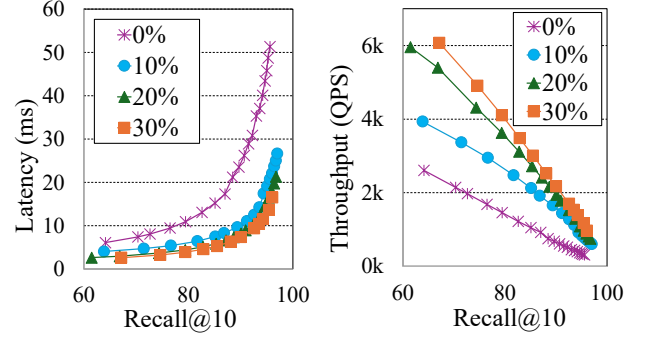
(a) Latency **(b)** Throughput

Figure 11. Latency and throughput of PageANN as varying memory ratio and recall accuracy on SIFT100M.

(a) Latency **(b)** Throughput

Figure 12. Latency and throughput comparison as varying the number of query threads on SIFT100M (Recall@10 = 0.9)

budget increases from 0% to 10%. This improvement arises because the memory–disk coordination in PageANN allows low-compression vectors to be leveraged even under tight memory constraints. When the budget grows from 10% to 20%, the performance gains are more pronounced because all compressed vectors can now fit in memory and each page contains more vectors. As a result, the page-node graph shrinks further and the search path shortens. In addition, the in-memory fast routing procedure is applied. By contrast, the performance increase from 20% to 30% is relatively modest, mainly due to the use of additional cached pages.

6.4 Throughput and Scalability

We evaluate the scalability of PageANN by measuring its throughput and average query latency as the number of concurrent query threads increases from 1 to 16 on the SIFT100M dataset with Recall@10=0.9 as shown in Figure 12. As the number of threads increases, PageANN achieves near-linear throughput scaling, with an 8.34× improvement from single-thread to 16-thread execution. At 16 threads, PageANN delivers 150% higher throughput than DiskANN, 230% higher than

Table 5. Graph construction time (hours) during pre-processing and CPU utilization (%) during query process.

Method	SIFT100M		SPACE100M		DEEP100M	
	Graph	CPU	Graph	CPU	Graph	CPU
DiskANN	1.20	47%	1.26	145%	2.64	171%
Starling	3.03	106%	2.37	144%	7.11	152%
PipeANN	1.21	1548%	1.27	1026%	2.65	1053%
PageANN	1.68	168%	1.59	334%	3.50	217%

PipeANN, and 115% higher than Starling. Latency remains low even under high concurrency, increasing by less than 92% from 1 to 16 threads, in contrast to DiskANN where latency more than triples and PipeANN where it increases over fivefold. Overall, PageANN achieves both high throughput and low latency across varying concurrency levels, demonstrating strong scalability for large-scale ANN search.

6.5 Overhead Analysis

We evaluate the offline graph construction time and the online CPU utilization during query processing for each method across the three representative datasets. As shown in Table 5, PipeANN exhibits slightly higher graph contruction time compared to the fastest schemes, due to the additional page-node graph construction. Beyond build time, PageANN generally show higher CPU usage, as it adopts a pipeline design and fully utilizes all data in each loaded page during computation. In summary, while PageANN introduces a modest computational and pre-processing overhead compared to the fastest scheme, this overhead is acceptable given the substantial performance gains it delivers.

7 Related Work

In-memory ANNS approaches. Research on in-memory ANNS is generally categorized into three types: tree-based [4, 17, 42], hashing-based [12, 18, 22, 23, 30–32, 45, 47], and graph-based methods [9, 15, 16, 28, 33, 34]. Among these, graph-based approaches stand out in large-scale, high-dimensional search by offering both high speed and accuracy. However, as dataset sizes continue to grow, the memory overhead of in-memory graph-based ANNS becomes a significant bottleneck, limiting their scalability and applicability. PageANN addresses these memory and scalability challenges by offloading the search graph and vector values to SSDs and fully leveraging SSD characteristics to maximize search performance.

Distributed ANNS approaches To address the memory overhead and scalability issues of in-memory graph-based ANNS, many distributed ANNS methods have been proposed. These methods fall into two categories: independent sharding [13, 48, 50] and global indexing [56]. Independent sharding offers a simpler system design but suffers from computational inefficiency. In contrast, global indexing avoids redundant computation but incurs significant network communication overhead. PageANN, on the other hand, fully resolves the scalability challenges of graph-based ANNS with a simple system design, efficient computation, minimal I/O latency, and no communication overhead.

Disk-based ANNS approaches To effectively alleviate the memory constraints of graph-based ANNS, disk-based approaches offload part or all search-related data from memory to disk. A pioneer work, DiskANN [43], retains only compressed vector values in memory while storing the original vectors and graph index on SSDs. Building on this, DiskANN++ [36] and Starling [49] optimize SSD page layouts and integrate an in-memory routing process. LM-DiskANN [37] offloads all compressed values to disk at the cost of significantly increased disk usage, while PipeANN [19] aligns the search algorithm with SSD characteristics. In contrast, SPANN [10] keeps the graph in memory and offloads vector values to SSDs, performing graph traversal entirely in memory and issuing all I/O requests only after traversal completes. However, as discussed earlier, all these methods still suffer from high search latency and scalability limitations. PageANN addresses the scalability issue while greatly reducing search latency and increasing throughput. Another types of disk-based ANN schemes focus on the dynamic ANN system to mainly minimize the insertion and graph construction overhead, which is out of the scope with this paper [38, 51, 52, 57].

Specialized hardware ANNS approaches. Recent methods such as FusionANNS [46], HM-ANN [40], and SmartANN [55] address memory and I/O bottlenecks by leveraging specialized hardware. FusionANNS utilizes GPUs in collaboration with CPUs to reduce I/O operations, HM-ANN exploits heterogeneous memory (DRAM + persistent memory module) to balance cost and performance, and SmartANN employs computational storage devices (SmartSSDs) to minimize host I/O operations and enable near-data processing. However, their reliance on specialized hardware limits flexibility and increases deployment complexity. Unlike these methods, PageANN does not depend on specialized hardware and can be deployed on any machine with varying memory budgets.

8 Conclusion

In this work, we presented PageANN, a scalable disk-based ANN framework that addresses the key limitations of existing state-of-the-art solutions through a co-design of graph structure, storage layout, and memory management. By introducing a page-based graph that aligns with SSD I/O granularity, a storage layout that leverages spatial locality and merging, and a dynamic memory management strategy with lightweight routing, PageANN achieves high throughput and scalability across diverse memory budgets. Experimental results on large-scale datasets demonstrate that PageANN

delivers 1.85x–10.83x higher throughput and 51.7%–91.9% lower latency across datasets and memory budgets, while maintaining the same high recall accuracy.

9 Acknowledgment

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