ECOLE SUPÉRIEURE POLYTECHNIQUE INTERNATIONALE PRIVÉE
DE SFAX

Chapter 3

Combinational circuits

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Introduction

Combinational circuit is a circuit in which we combine the different gates in the circuit, for example encoder, decoder, multiplexer and demultiplexer. Some of the characteristics of combinational circuits are following:

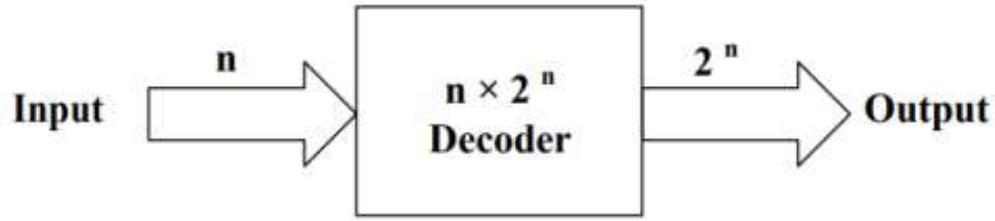
- The output of combinational circuit at any instant of time, depends only on the levels present at input terminals.
- The combinational circuit do not use any memory. The previous state of input does not have any effect on the present state of the circuit.
- A combinational circuit can have an n number of inputs and m number of outputs.

Decoder and Encoder

- The encoders and decoders play an essential role in digital electronics projects;
- Encoders and decoders are combinational circuits that used to convert data from one form to another form.
- These are frequently used in communication system such as telecommunication, networking, etc.. to transfer data from one end to the other end.
- Similarly, in the digital domain, for easy transmission of data, it is often encrypted or placed within codes, and then transmitted. At the receiver, the coded data is decrypted or gathered from the code and is processed in order to be displayed or given to the load accordingly.

Decoder

- The process of taking some type of code and determining what it represents in terms of a recognizable number or character is called decoding.
- A decoder is a combinational logic circuit that performs the decoding function, and produce an output that indicates the (meaning) of the input code.
- A decoder is a combinational circuit. It has n input and to a maximum $m = 2^n$ outputs



Block diagram of decoder

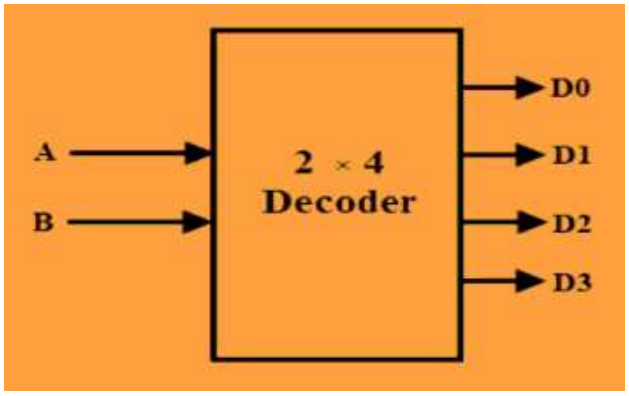
- Exactly one output will be active for each input combination
- Examples of Decoders are Code converters, BCD to seven segment decoders and Nixie tube decoders

Decoder

2 to 4 Line Decoder

- A and B are the two inputs where D_0, D_1, D_2, D_3 are the four outputs.
- Truth table explains the operations of a decoder. It shows that each output is 1 for only a specific combination of inputs.

Block diagram



Truth table

Input		Output			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

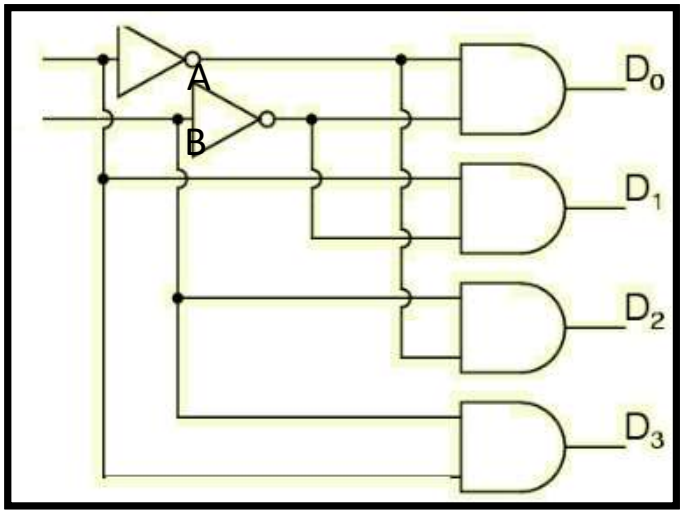
$$D_0 = \bar{A}\bar{B}$$

$$D_1 = A\bar{B}$$

$$D_2 = \bar{A}B$$

$$D_3 = AB$$

Decoder



$$D_0 = \bar{A}\bar{B}$$

$$D_1 = A\bar{B}$$

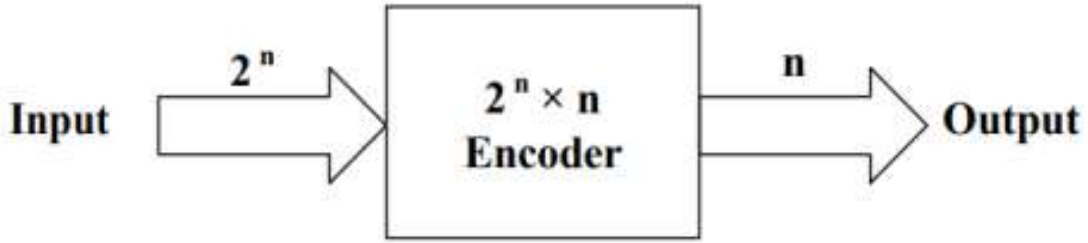
$$D_2 = \bar{A}B$$

$$D_3 = AB$$

2-to-4-Decoder Circuit

Encoder

- Encoder is a combinational circuit which is designed to perform the inverse operation of the decoder.
- An encoder has maximum of 2^n number of input lines and n number of output lines.
- An encoder produces an n bit binary code corresponding to the digital input number.
- The encoder accepts an 2^n input digital word and converts it into an n bit another digital word.



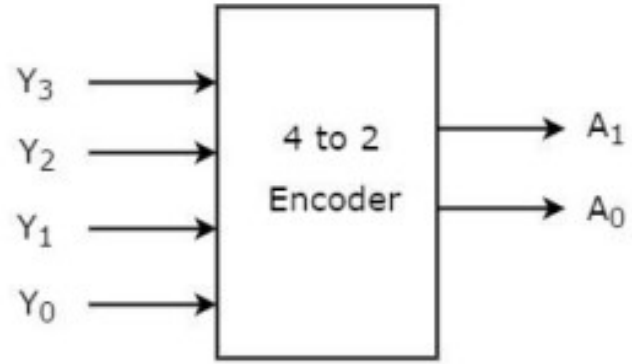
Block diagram of encoder

- Only one of the inputs can be active '1' in order to get the respective binary code at the output.
- Examples of Encoders are following : Decimal to BCD encoder, Octal to binary encoder, Hexadecimal to binary encoder

Encoder

4-to-2 Encoder

- Let 4 to 2 Encoder has four inputs Y_3, Y_2, Y_1 & Y_0 and two outputs A_1 & A_0.



The block diagram of 4-to-2 Encoder

- At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output

Encoder

Truth table of 4 to 2 encoder

Input				Output	
Y_3	Y_2	Y_1	Y_0	A1	A0
0	0	0	0	x	x
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

K-map for A1

y_3y_2 \ y_1y_0	00	01	11	10
00	x	0	x	0
01	1	x	x	x
11	x	x	x	x
10	1	x	x	x

$$A_1 = y_2 + y_3$$

K-map for A0

y_3y_2 \ y_1y_0	00	01	11	10
00	x	0	x	1
01	0	x	x	x
11	x	x	x	x
10	1	x	x	x

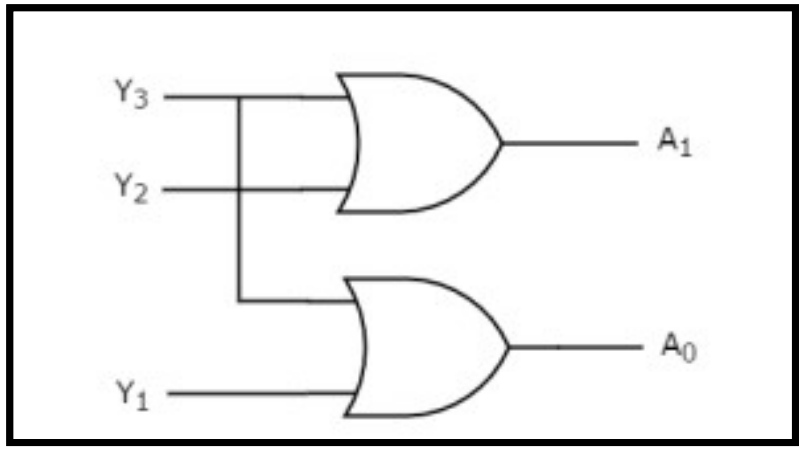
$$A_0 = y_1 + y_3$$

Encoder

- From Truth table, we can write the **Boolean functions** for each output as:

$A_1 = Y_2 + Y_3$ $\qquad$ $A_0 = Y_1 + Y_3$

- We can implement the above two Boolean functions by using two input OR gates.

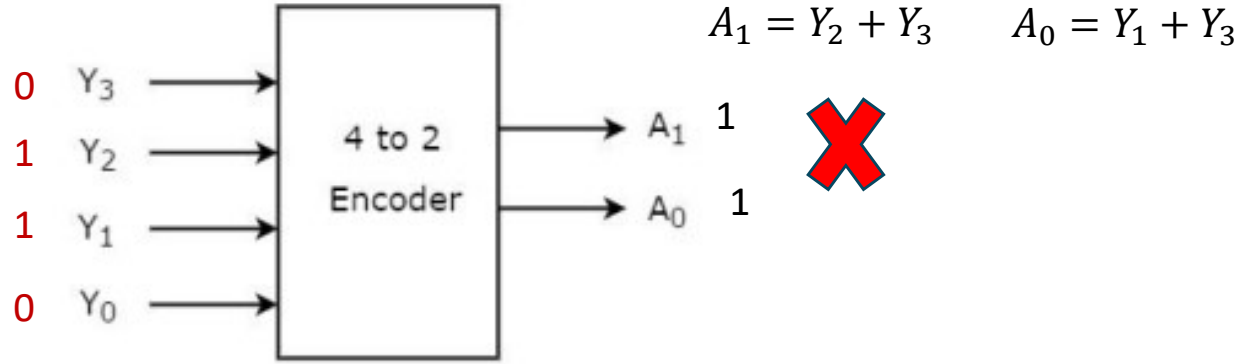


The circuit diagram of 4 to 2

Encoder

Drawbacks of Encoder

- If more than one input is active High, then the encoder produces an output, which may not be the correct code. For example, if both Y1 and Y2 are ‘1’, then the encoder produces 11 at the output. This is neither equivalent code corresponding to Y1, when it is ‘1’ nor the equivalent code corresponding to Y2, when it is ‘1’.



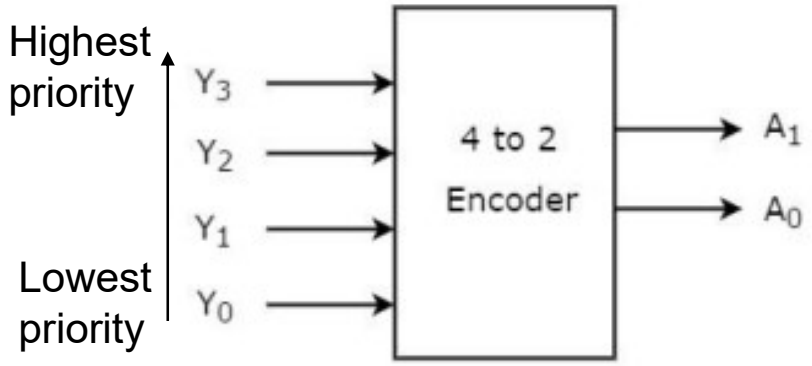
- So, to overcome these difficulties, we should assign priorities to each input of encoder. Then, the output of encoder will be the binary code corresponding to the active High inputs, which has higher priority. This encoder is called as **priority encoder**.

Priority Encoder

- A 4 to 2 priority encoder has four inputs Y3, Y2, Y1 & Y0 and two outputs A1 & A0.
- Here, the input, Y3 has the highest priority, whereas the input, Y0 has the lowest priority.
- In this case, even if more than one input is '1' at the same time, the output will be the binary code corresponding to the input, which is having higher priority.

Input				Output	
Y_3	Y_2	Y_1	Y_0	A1	A0
0	0	0	0	x	x
0	0	0	1	0	0
0	0	1	x	0	1
0	1	x	x	1	0
1	x	x	x	1	1

Truth table of 4 to 2 priority encoder



Priority Encoder

Input				Output	
Y_3	Y_2	Y_1	Y_0	A1	A0
0	0	0	0	x	x
0	0	0	1	0	0
0	0	1	x	0	1
0	1	x	x	1	0
1	x	x	x	1	1

K-map for A1

y_3y_2 \ y_1y_0	00	01	11	10
00	x	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$$A_1 = y_2 + y_3$$

K-map for A0

y_3y_2 \ y_1y_0	00	01	11	10
00	x	0	1	1
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$$A_0 = y_3 + y_1\overline{y_2}$$

Multiplexer and Demultiplexer

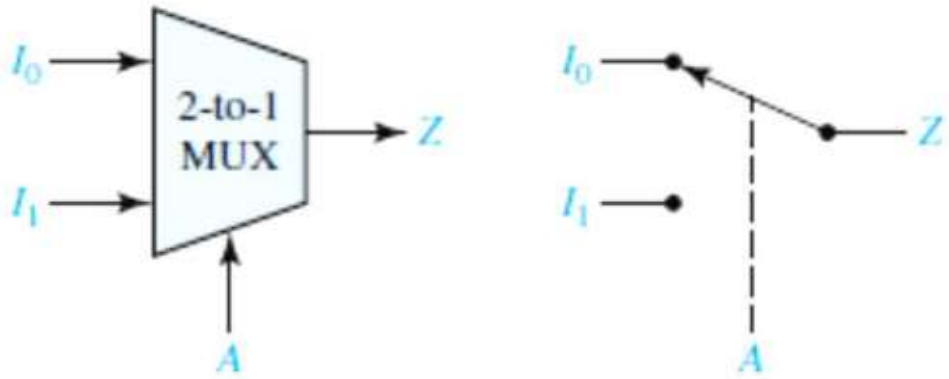
- The multiplexers and demultiplexers are digital electronic devices that are used to control applications.
- A simple data transmission system can be implemented using a multiplexer and a demultiplexer in conjunction with an interconnecting single line link.
- Such a system can result in a significant reduction in the number of lines required to transmit the data.

Multiplexer

- A multiplexer (MUX) is a combinational circuit that has
  - 2^n data inputs
  - n control inputs
  - A single output
- The control inputs select which data inputs to be connected to the output
- Since there are 'n' selection lines(control inputs), there will be 2^n possible combinations of zeros and ones. So, each combination will select only one data input.
- Multiplexer is also called as Mux.

Multiplexer

2 data input MUX and switching analog



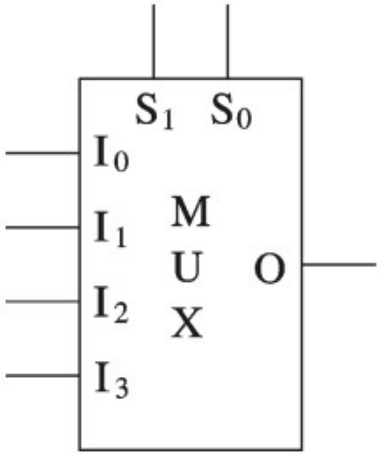
- When the control input A is 0, data input I0 will be connected to the output Z (i.e. Z=I0)
- When A=1 we will have Z=I1 .
- The logic equation of 2-to-1 Mux is:

$$Z = \bar{A}I_0 + AI_1$$

A	Z
0	I_0
1	I_1

Multiplexer

4 data input Mux

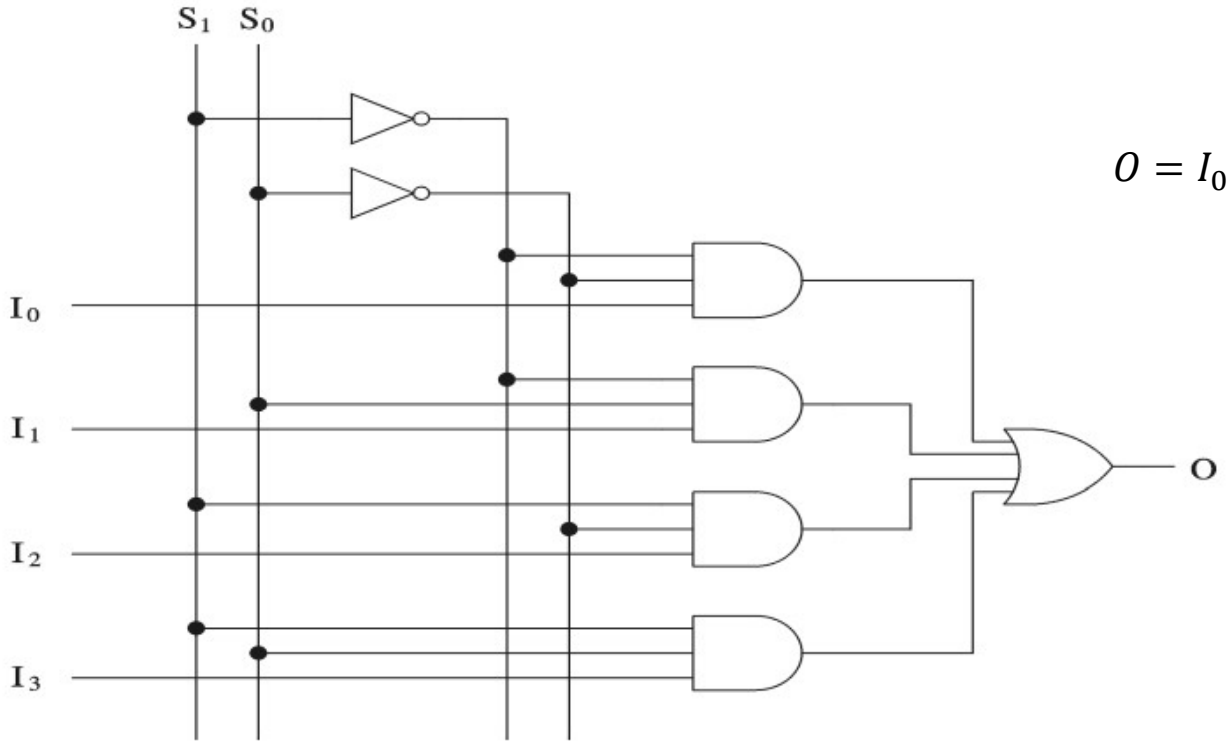


S_1	S_0	O
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$O = I_0\overline{S_1}\,\overline{S_0} + I_1 S_0\overline{S_1} + I_2 S_1\overline{S_0} + I_3 S_1 S_0$$

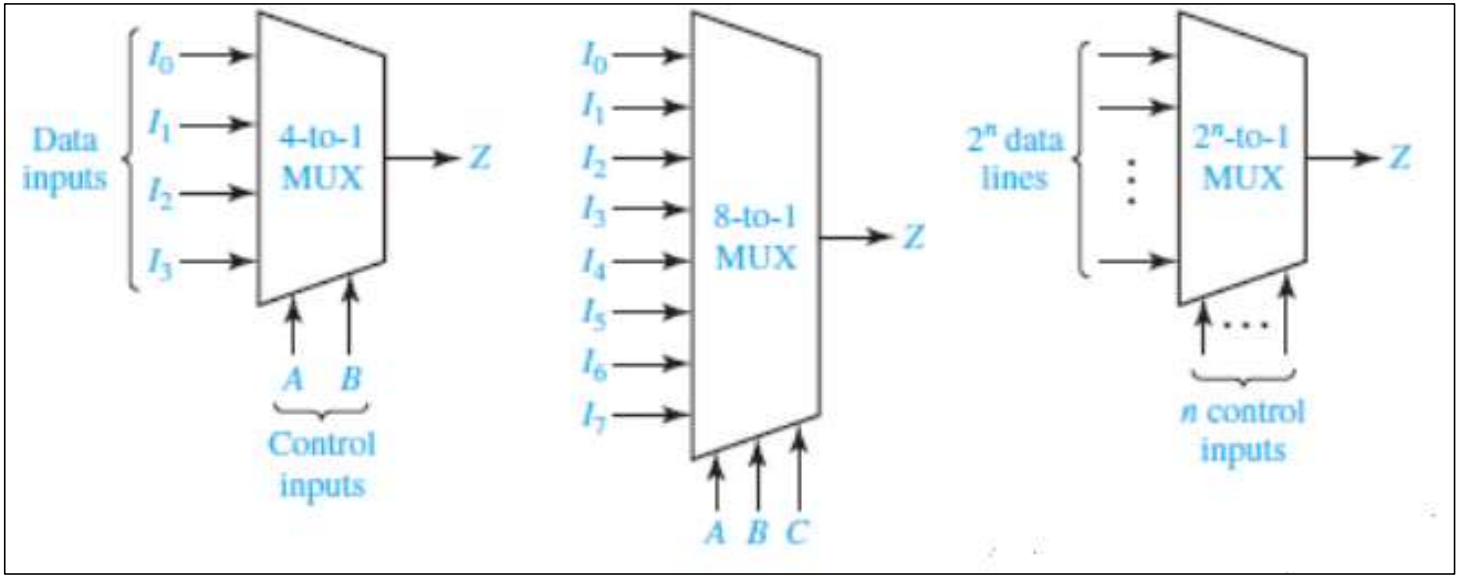
Multiplexer

4 data input Mux implementation



$$O = I_0\overline{S_1}\,\overline{S_0} + I_1 S_0\overline{S_1} + I_2 S_1\overline{S_0} + I_3 S_1 S_0$$

Multiplexers



Multiplexers : 4-to-1, 8-to-1 and 2n-to-1 Mux

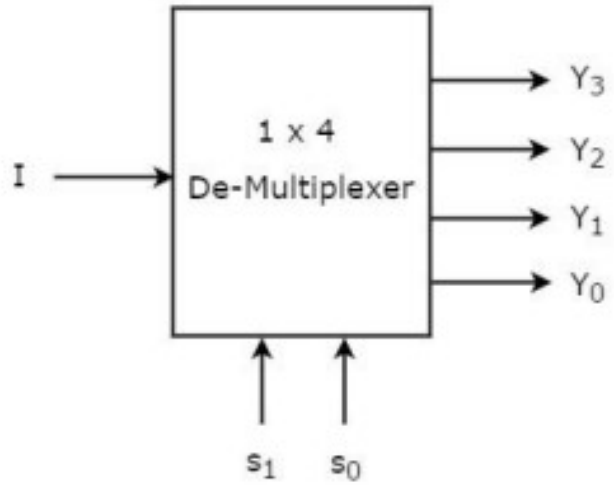
De-Multiplexer

- De-Multiplexer is a combinational circuit that performs the reverse operation of Multiplexer. It receives one input and distributes it over several outputs.
- It has single input, 'n' selection lines and maximum of 2^n outputs.
- The input will be connected to one of these outputs based on the values of selection lines.
- Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination can select only one output.
- De-Multiplexer is also called as De-Mux.

De-Multiplexer

1x4 De-Multiplexer

- 1x4 De-Multiplexer has one input I, two selection lines, s1 & s0 and four outputs Y3, Y2, Y1 &Y0.



The single input 'I' will be connected to one of the four outputs, Y3 to Y0 based on the values of selection lines s1 & s0.

De-Multiplexer

- The Truth table of 1x4 De-Multiplexer is shown below:

Selection Inputs		Outputs			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

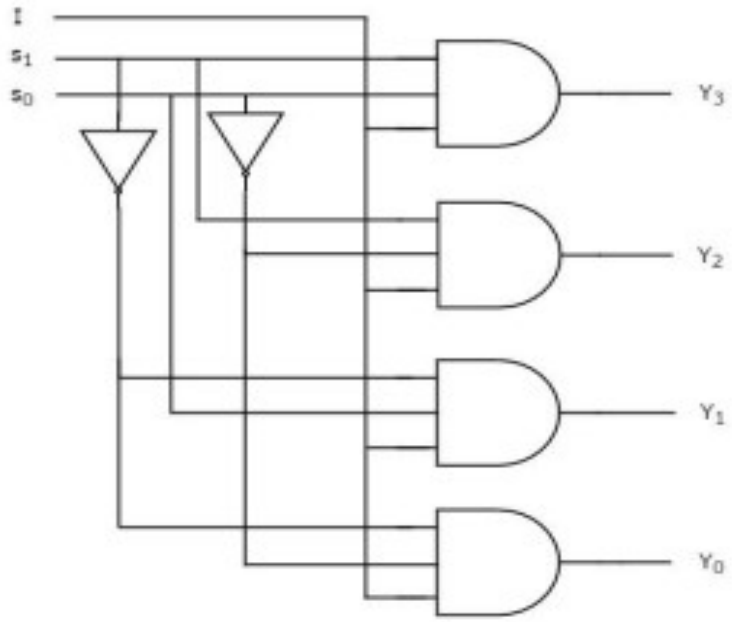
- From the above Truth table, we can directly write the Boolean functions for each output as:

$Y_3 = S_1 S_0 I$ $Y_2 = S_1 \overline{S_0} I$ $Y_1 = \overline{S_1} S_0 I$ $Y_0 = \overline{S_1}\,\overline{S_0} I$

De-Multiplexer

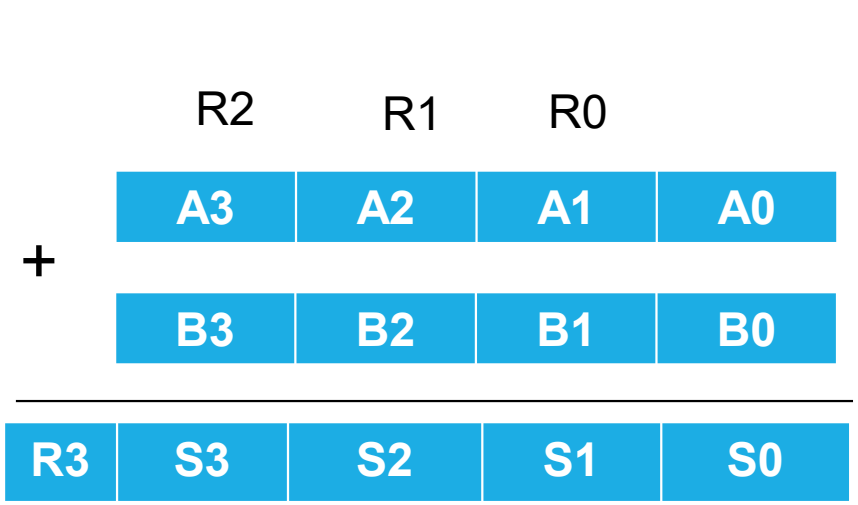
- We can implement these Boolean functions using Inverters & 4-input AND gates.

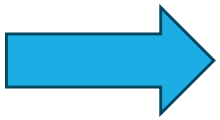
The circuit diagram of 1x4 De-Multiplexer

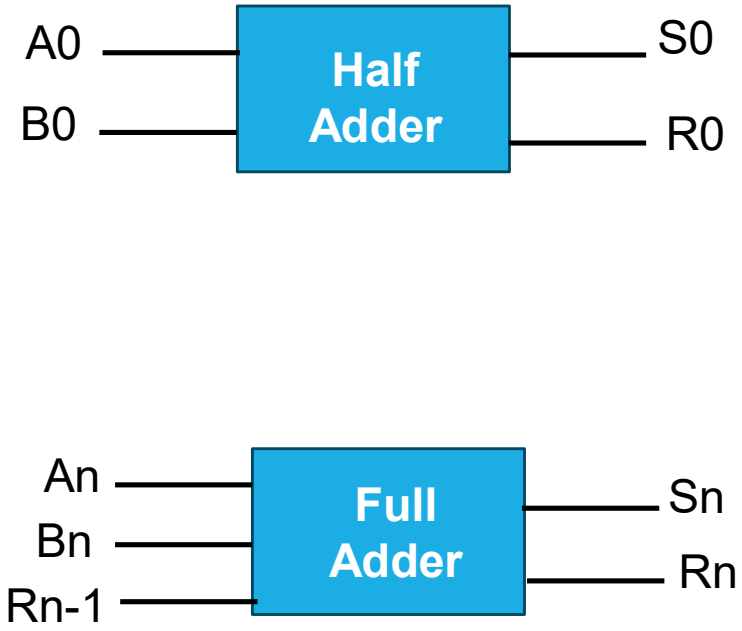


- Similarly, you can implement 1x8 De-Multiplexer and 1x16 De-Multiplexer by following the same procedure.

Half Adder and Full Adder







Half Adder and Full Adder

Half Adder

Truth table

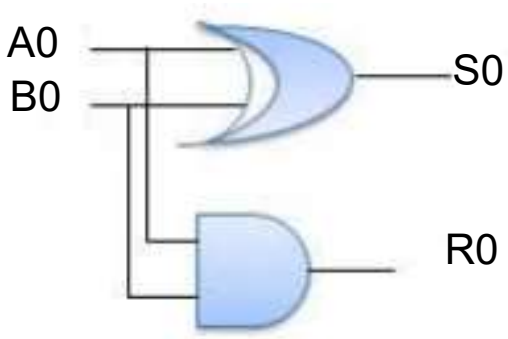
Input		Output	
A0	B0	S0	R0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean equations of the ouputs

$$S_0 = \overline{A_0}B_0 + A_0\overline{B_0} = A_0 \oplus B_0$$

$$R_0 = A_0B_0$$

Circuit Diagram



Half Adder and Full Adder

Full Adder

Input			Output	
An	Bn	Rn-1	Sn	Rn
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S_n = \overline{A_n}\,\overline{B_n}\,R_{n-1} + \overline{A_n}B_n\overline{R_{n-1}} + A_n\overline{B_n}\,\overline{R_{n-1}} + A_nB_nR_{n-1}$$
$$= \overline{A_n}\,(\overline{B_n}\,R_{n-1} + B_n\overline{R_{n-1}}) + A_n(\overline{B_n}\,\overline{R_{n-1}} + B_nR_{n-1})$$
$$= \overline{A_n}(B_n \oplus R_{n-1}) + A_n(\overline{B_n \oplus R_{n-1}}) = A_n \oplus B_n \oplus R_{n-1}$$

$$R_n = \overline{A_n}B_nR_{n-1} + A_n\overline{B_n}R_{n-1} + A_nB_n\overline{R_{n-1}} + A_nB_nR_{n-1}$$
$$= R_{n-1}(\overline{A_n}B_n + A_n\overline{B_n}) + A_nB_n = R_{n-1}\,(A_n \oplus B_n)) + A_nB_n$$

Half Adder and Full Adder

Addition of two 4 bits numbers