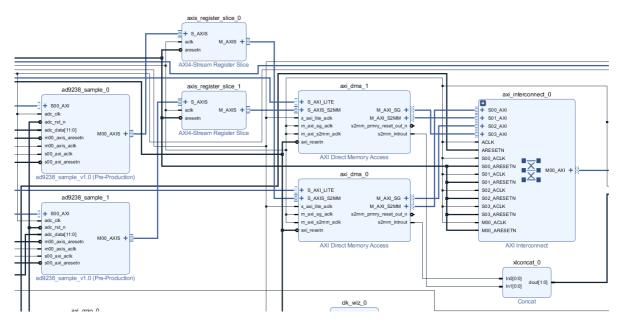
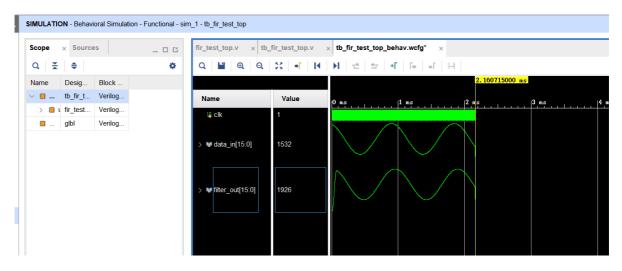
FIR 滤波器

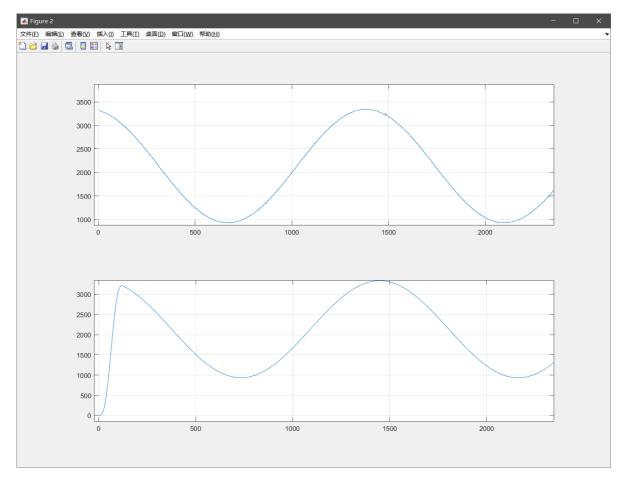
AD采样数据以AXI STREAM 总线连接



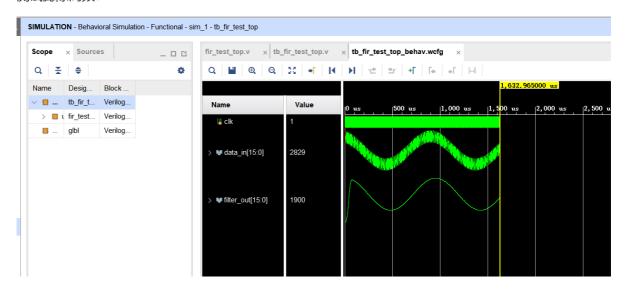
测试滤波输出:

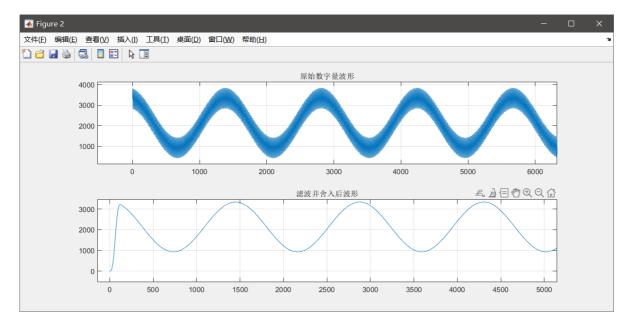
700hz 1024*257点





测试滤除高频:

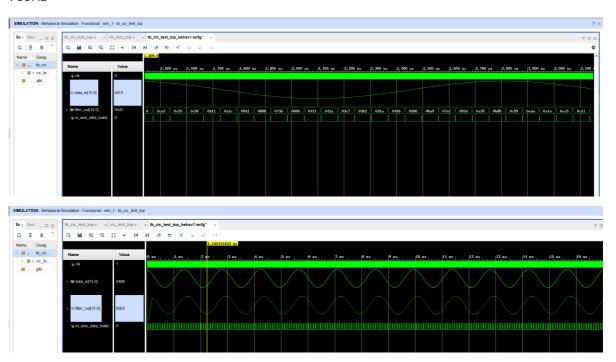




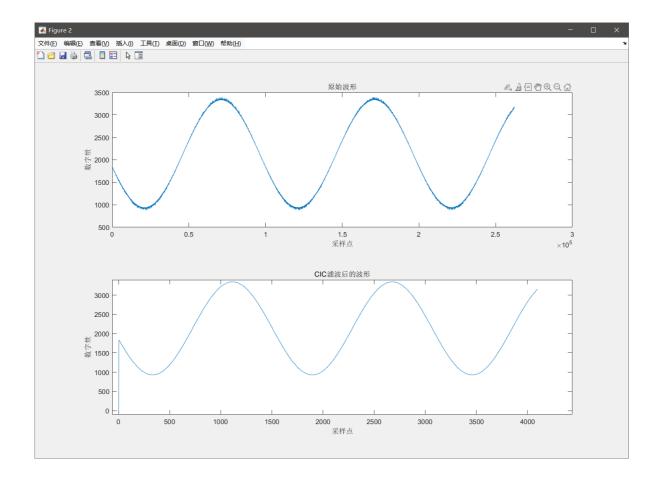
CIC 抽取滤波器

1024*256点 抽取为4096点

700Hz



10Hz



2024年11月6日

待调整 CIC 的接口,残血AXI STREAM。

ADC M00_AXIS

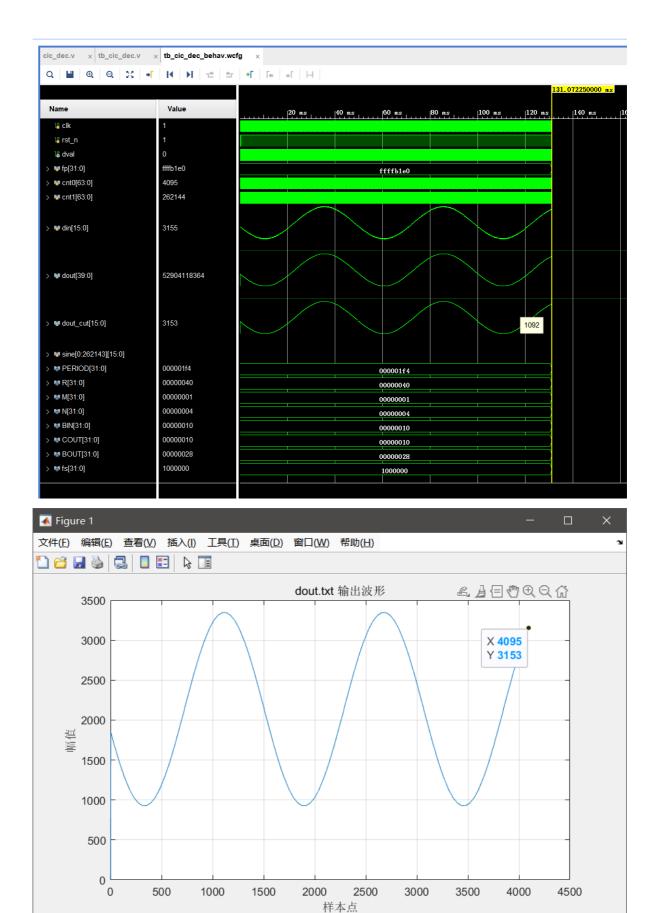
∨ ⊕ M00_AXIS	master							
m00_axis_tlast			ref	out				std_logic
m00_axis_tdata			ref	out	15	0		std_logic_vector
m00_axis_tvalid			ref	out				std_logic
m00_axis_tkeep			ref	out	1	0		std_logic_vector
			ref	in				std_logic

```
    S_AXIS
    s_axis_tdata[15:0]
    s_axis_tlast
    s_axis_tvalid
    s_axis_tready
    s_axis_tvalid
    m_axis_tvalid
    m_axis_tvalid
    m_axis_tvalid
    m_axis_tready
    aclk
    m_axis_tkeep[1:0]
    aresetn
```

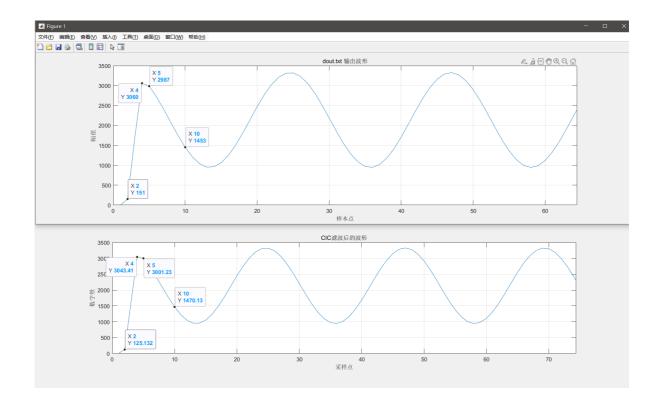
CIC 滤波器 (咸鱼) E:\ALINX_Project\CIC_by

测试降采样 1024*256点 dout输出4096点

R: 64
M: 1
N: 4
BIN: 16 bits
BOUT: 40 bits
COUT: 16 bits
cut method: ROUND
input nyquist freq: 500000 Hz
output nyquist freq: 7812 Hz
cnt0 width: 6 bits



同样数据 700Hz 1024*256点 上图为 FPGA CIC模块仿真输出,下图为matlab 设计的CIC滤波器输出, 趋势相同,数值问题为,FPGA仿真输出为之间截取(ROUND为四舍五入)16位(便于传输),原始输 出应为37位,没有保留完整数值特性,所以有差异,后续可以考虑拓展为32位。 ADC采集数据是12 位,首位补0拓展为16位便于传输,进入滤波器后,输出32位,结果较精确,



测试滤除高频

10hz 叠加 18khz 1024*256点 dout输出4096点

