11.Design and implement 2-bit half adder with NAND using logisim simulator.

AIM: To design and implement the two bit half adder with NAND using Logisim simulator.

TRUTH TABLE:-

The half-adder is a digital circuit that adds 2 bits (A and B) generating 2 bits at the output for the sum (S) and carry (C). Its truth table is shown in below table.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

THE FOLLOWING STEPS IS USED TO DRAW A HALF-ADDER CIRCUIT.

⇒Insert 2 inputs into the canvas. o Label the inputs (A & B) by setting the attribute 'Label' in the attribute table.

Note that both inputs have now 0s inside their green spots. These are the current bit value of the input.

⇒Insert one NAND gate and one NAND gate into the canvas.

⟶The two gates are located inside the 'Gates' library in the explorer pane.

⟶Change the 'Number of Inputs' in the attribute table to 2.

⇒Insert 2 outputs in the canvas

Label the outputs (S & C).

Note that both outputs have X inside the dots.

⇒X indicates an invalid value for the output.

Connect the inputs to the NAND gate.

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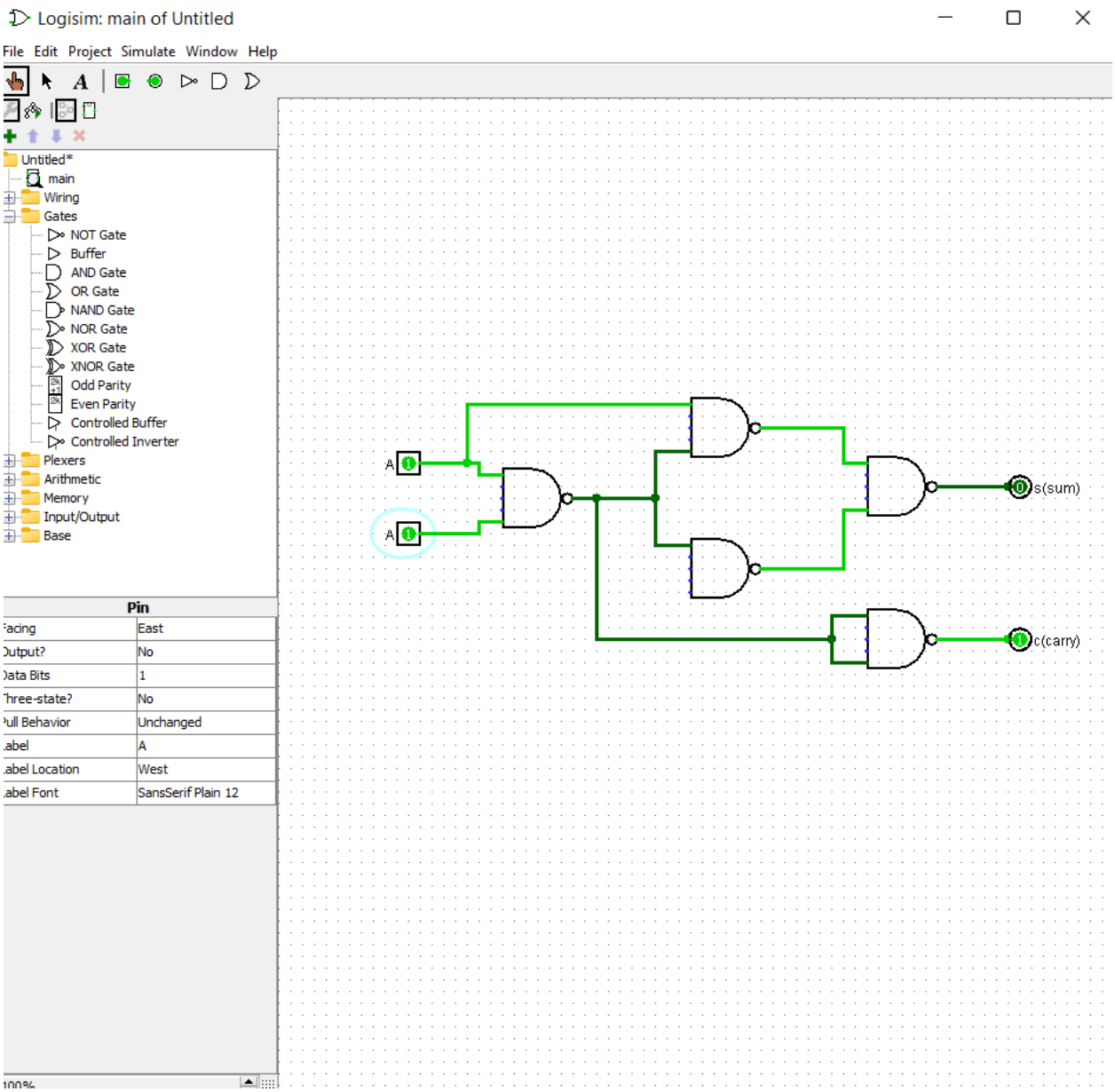
⇒Start the connection on the NAND gate input and finish it on the wire reaching the designated input.

Connect the outputs to the gates.



RESULT:-

Hence the designing of the 2-bit half adder using logisim simulator has been implemented successfully.