|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **eZ430-RF2500T** | | **eZ430-F2013** | |
| **Pin** | **Function** | **Description** | **Function** | **Description** |
| 1 | GND | Ground reference | VCC | Supply voltage |
| 2 | VCC | Supply voltage | P1.0/TACLK/ACLK/A0+ | General-purpose digital I/O pin  Timer\_A, clock signal TACLK input ACLK signal output  SD16\_A positive analog input A0 |
| 3 | P2.0 / ACLK / A0 / OA0I0 | General-purpose digital I/O pin / ACLK output / ADC10, analog input A0 | P1.1/TA0/A0-/A4+ | General-purpose digital I/O pin  Timer\_A, capture: CCI0A input, compare: Out0 output SD16\_A negative analog input A0  SD16\_A positive analog input A4 |
| 4 | P2.1 / TAINCLK / SMCLK / A1 / A0O | General-purpose digital I/O pin / ADC10, analog input A1 Timer\_A, clock signal at INCLK, SMCLK signal output | P1.2/TA1/A1+/A4- | General-purpose digital I/O pin  Timer\_A, capture: CCI1A input, compare: Out1 output SD16\_A positive analog input A1  SD16\_A negative analog input A4 |
| 5 | P2.2 / TA0 / A2 / OA0I1 | General-purpose digital I/O pin / ADC10, analog input A2 Timer\_A, capture: CCI0B input/BSL receive, compare: OUT0 output | P1.3/VREF/A1- | General-purpose digital I/O pin  Input for an external reference voltage/internal reference voltage output (can be used as mid-voltage)  SD16\_A negative analog input A1 |
| 6 | P2.3 / TA1 / A3 / VREF– / VeREF– / OA1I1 / OA1O | General-purpose digital I/O pin / Timer\_A, capture: CCI1B input, compare: OUT1 output / ADC10, analog input A3 / negative reference voltage output/input | P1.4/SMCLK/A2+/TCK | General-purpose digital I/O pin  SMCLK signal output SD16\_A positive analog input A2  JTAG test clock, input terminal for device programming and test |
| 7 | P2.4 / TA2 / A4 / VREF+ / VeREF+ / OA1I0 | General-purpose digital I/O pin / Timer\_A, compare: OUT2 output / ADC10, analog input A4 / positive reference voltage output/input | P1.5/TA0/A2-/SCLK/TMS | General-purpose digital I/O pin  Timer\_A, compare: Out0 output  SD16\_A negative analog input A2  USI: external clock input in SPI or I2C mode; clock output in SPI mode  JTAG test mode select, input terminal for device programming and test |
| 8 | P4.3 / TB0 / A12 / OA0O | General-purpose digital I/O pin / ADC10 analog input A12 / Timer\_B, capture: CCI0B input, compare: OUT0 output | P1.6/TA1/A3+/SDO/SCL/ TDI/TCLK | General-purpose digital I/O pin  Timer\_A, capture: CCI1B input, compare: Out1 output  SD16\_A positive analog input A3 USI: Data output in SPI mode; I2C clock in I2C mode  JTAG test data input or test clock input during programming and test |
| 9 | P4.4 / TB1 / A13 / OA1O | General-purpose digital I/O pin / ADC10 analog input A13 / Timer\_B, capture: CCI1B input, compare: OUT1 output | P1.7/A3-/SDI/SDA/ TDO/TDI(1) | General-purpose digital I/O pin  SD16\_A negative analog input A3 USI: Data input in SPI mode; I2C data in I2C mode  JTAG test data output terminal or test data input during programming and test |
| 10 | P4.5 / TB2 / A14 / OA0I3 | General-purpose digital I/O pin / ADC10 analog input A14 / Timer\_B, compare: OUT2 output | RST/NMI/SBWTDIO | Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test |
| 11 | P4.6 / TBOUTH / A15 / OA1I3 | General-purpose digital I/O pin / ADC10 analog input A15 / Timer\_B, switch all TB0 to TB3 outputs to high impedance | TEST/SBWTCK | Selects test mode for JTAG pins on Port 1. The device protection fuse is  connected to TEST.  Spy-Bi-Wire test clock input during programming and test |
| 12 | GND | Ground reference | XOUT/P2.7 | Output terminal of crystal oscillator General-purpose digital I/O pin(2) |
| 13 | P2.6 / XIN (GDO0) | General-purpose digital I/O pin / Input terminal of crystal oscillator | XIN/P2.6/TA1 | Input terminal of crystal oscillator  General-purpose digital I/O pin  Timer\_A, compare: Out1 output |
| 14 | P2.7 / XOUT (GDO2) | General-purpose digital I/O pin / Output terminal of crystal oscillator | Vss | Ground reference |
| 15 | P3.2 / UCB0SOMI / UCB0SCL | General-purpose digital I/O pin USCI\_B0 slave out/master in when in SPI mode, SCL I2C clock in I2C mode |  |  |
| 16 | P3.3 / UCB0CLK / UCA0STE | General-purpose digital I/O pin USCI\_B0 clock input/output / USCI\_A0 slave transmit enable |  |  |
| 17 | P3.0 / UCB0STE / UCA0CLK / A5 | General-purpose digital I/O pin / USCI\_B0 slave transmit enable / USCI\_A0 clock input/output / ADC10, analog input A5 |  |  |
| 18 | P3.1 / UCB0SIMO / UCB0SDA | General-purpose digital I/O pin / USCI\_B0 slave in/master out in SPI mode, SDA I2C data in I2C mode |  |  |
| **Pin** | **Function** | **Description** |  |  |
| 1 | P3.4 / UCA0TXD / UCA0SIMO | General-purpose digital I/O pin / USCI\_A0 transmit data output in UART mode (UART communication from 2274 to PC), slave in/master out in SPI mode |  |  |
| 2 | GND | Ground reference |  |  |
| 3 | RST / SBWTDIO | Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test |  |  |
| 4 | TEST / SBWTCK | Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test |  |  |
| 5 | VCC (3.6V) | Supply voltage |  |  |
| 6 | P3.5 / UCA0RXD / UCA0SOMI | General-purpose digital I/O pin / USCI\_A0 receive data input in UART mode (UART communication from 2274 to PC), slave out/master in when in SPI mode |  |  |