PIC24FV32KA304 Family Silicon Errata and Data Sheet Clarification

The PIC24FV32KA304 family devices that you have received conform functionally to the current Device Data Sheet (DS39995**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FV32KA304 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FV32KA304 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A4			A4
PIC24F32KA304	4516h	0004h	PIC24FV32KA304	4517h	0004h
PIC24F32KA302	4512h		PIC24FV32KA302	4513h	
PIC24F32KA301	4518h		PIC24FV32KA301	4519h	
PIC24F16KA304	4506h		PIC24FV16KA304	4507h	
PIC24F16KA302	4502h		PIC24FV16KA302	4503h	
PIC24F16KA301	4508h		PIC24FV16KA301	4509h	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FXXKA1XX/KA3XX Flash Programming Specifications"* (DS39919) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A4
Core	Low-Voltage Regulator	1.	High-voltage programming entry unavailable in Low-Voltage Sleep modes.	X
Reset	BOR	2.	Unexpected BOR events when BOR is disabled in Sleep mode.	X
A/D	Threshold Detect	3.	Auto-scan feature may not trigger correctly in Sleep mode.	X
UART	TX Buffer	4.	Out-of-order transmit data when buffer is filled.	X
UART	Transmit	5.	UxTXBF flag may not indicate correctly.	X
A/D	Threshold Detect	6.	Current in Auto-Scan mode may exceed expected values.	X
A/D	Threshold Detect	7.	Interrupt may not trigger in certain Auto-Scan modes.	X
HLVD	DC18 Value Changes	8.	Change in trip points.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Core (Low-Voltage Regulator)

When operating in Low-Voltage Sleep mode, LVREN = 1 (RCON<12>) and LVRCFG = 0 (FPOR<2>), the device may not be able to enter programming modes using high-voltage entry (V_{IHH} applied to $\overline{MCLR}$).

Work around

If entry into a programming mode is required while the device is in Low-Voltage Sleep mode, use low-voltage entry into programming. Verify that $\overline{MCLR}$ functionality is enabled, MCLRE = 1 (FPOR<7>), before attempting programming.

Affected Silicon Revisions

A4							
X							

2. Module: Reset (BOR)

Under certain conditions, the device may improperly perform a Brown-out Reset upon wake-up from a Sleep mode. This has been observed under two conditions:

1. When the BOR is disabled in Sleep mode, BOREN<1:0> = 10 (FPOR<1:0>), a BOR may occur when the device wakes from Sleep, regardless of the supply voltage.
2. When the BOR is configured for software control (BOREN<1:0> = 01), the device enters and wakes from Sleep normally while the BOR is disabled in software, SBOREN = 0 (RCON<13>). However, if the BOR was disabled prior to entering Sleep mode and is subsequently enabled after waking from Sleep, a BOR may occur, regardless of the supply voltage.

BOR functions normally when it is always enabled or disabled (BOREN<1:0> = 11 or 00).

Work around

Do not use Sleep mode when BOREN<1:0> = 10.

If the BOR is to operate under software control, always enable the HLVD module, HLVDEN = 1 (HLVDCON<15>), before enabling the BOR in software (SBOREN = 1). This procedure activates the internal band gap reference and assures its stability for the BOR circuit.

Affected Silicon Revisions

A4							
X							

3. Module: A/D (Threshold Detect)

When the auto-scan feature of the Threshold Detect is enabled (AD1CON5<15> = 1), automatic scan may fail when these conditions occur together:

- the Device is in Sleep mode, and
- Timer1 is selected as the sample trigger clock source (AD1CON1<7:4> = 0101).

Timer1 and other timers will function correctly as sample triggers in other power-saving modes, such as Idle mode.

Work around

If auto-scan functionality is required during Sleep, use INT0 as the sample trigger.

Affected Silicon Revisions

A4							
X							

4. Module: UART (TX Buffer)

If the transmit buffer is filled sequentially with four characters, the characters may not be transmitted in the correct order.

Work around

Do not completely fill the buffer before transmitting data; send three characters or less at a time.

Affected Silicon Revisions

A4							
X							

5. Module: UART (Transmit)

The Transmit Buffer Full flag, UTXBF (UxSTA<9>), may become cleared before data starts moving out of the full buffer. If the flag is used to determine when data can be written to the buffer, new data may not be accepted and data may not be transmitted.

Work around

Poll the Transmit Buffer Empty flag (TRMT, UxSTA<8>) to determine when the transmit buffer is empty and can be written to.

Alternatively, configure the UART to set the Transmit Interrupt Flag (UxTXIF) whenever a character is shifted into the Transmit Shift register (UTXISEL<1:0> = 00). When a transmit interrupt occurs, this indicates that at least one buffer position is open and that the buffer can be written to.

Affected Silicon Revisions

A4							
X							

6. Module: A/D (Threshold Detect)

In Auto-Scan mode, with low power enabled (AD1CON5<15> = 1, AD1CON5<14> = 1) and the device in Sleep mode, the ADRC may not turn off between scans, resulting in a higher current draw than anticipated.

Work around

None.

Affected Silicon Revisions

A4							
X							

7. Module: A/D (Threshold Detect)

In Auto-Scan mode (AD1CON5<15> = 1), when the Auto-Scan Interrupt mode bits are set to '11' (AD1CON5<9:8> = 11), the highest number channel selected for scanning in AD1CSSL or AD1CSSH may not trigger an interrupt on a valid comparison.

Work around

Add a dummy channel to the scanning sequence. For example, when scanning AN0 and AN1, set AD1CSSL to 0x0007, or 0x8003, or whatever is practical given the implementation.

Also, if the highest number channel needs to be scanned, the AD1CHITH bit can be polled to observe a valid comparison.

Affected Silicon Revisions

A4							
X							

8. Module: HLVD (DC18 Value Changes)

The maximum and minimum values of the High/Low-Voltage Detect Characteristics (DC18), shown in Table 29-4 of the data sheet, have changed for this revision. The new values are shown in Table 3.

Affected Silicon Revisions

A4							
X							

TABLE 3: HIGH/LOW–VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX **2.0V to 5.5V PIC24FV32KA3XX** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0000(2)	—	—	2.01	V	
			HLVDL<3:0> = 0001	1.91	—	2.25	V	
			HLVDL<3:0> = 0010	2.12	—	2.48	V	
			HLVDL<3:0> = 0011	2.27	—	2.67	V	
			HLVDL<3:0> = 0100	2.36	—	2.76	V	
			HLVDL<3:0> = 0101	2.55	—	2.99	V	
			HLVDL<3:0> = 0110	2.79	—	3.27	V	
			HLVDL<3:0> = 0111	2.93	—	3.43	V	
			HLVDL<3:0> = 1000	3.06	—	3.60	V	
			HLVDL<3:0> = 1001	3.23	—	3.79	V	
			HLVDL<3:0> = 1010(1)	3.40	—	4.00	V	
			HLVDL<3:0> = 1011(1)	3.61	—	4.23	V	
			HLVDL<3:0> = 1100(1)	3.83	—	4.49	V	
			HLVDL<3:0> = 1101(1)	4.08	—	4.80	V	
			HLVDL<3:0> = 1110(1)	4.38	—	5.14	V	

Note 1: These trip points should not be used on PIC24FXXKA30X devices.

2: This trip point should not be used on PIC24FVXXKA30X devices.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39995**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Overview (and Other Locations)

In several locations throughout the document, references are made to, and information provided for, devices in 20-pin QFN packages. In fact, PIC24FV32KA304 family devices are not available in this package type.

All data for 20-pin QFN packages for this family is to be disregarded. This includes:

- Table 1-3, “PIC24FV32KA304 Family Pinout Descriptions” in **Section 1.0 “Device Overview”**.
- Table 29-2, “Thermal Packaging Characteristics” in **Section 29.0 “Electrical Characteristics”**.

2. Module: Overview

Throughout Table 1-3 (“PIC32FV32KA304 Family Pinout Descriptions”), the pin assignments for some functions have been incorrectly listed for some package types. These include:

- All CTMU Edge Detect Inputs (CTEDn)
- Input Capture 1
- Output Compare 1 and 3
- Output Compare Fault Input B
- ICSP™ Ports 2 and 3 (PGEC/D 2 and 3)
- I2C2 Clock
- SPI1 and 2 Pins (SCK1 and 2, SDI1 and 2, SDO2, $\overline{SS2}$)
- UART1 Transmit and Receive

In some cases, the pin assignments listed were in error. In others, multiple pin assignments were listed where only one existed.

Corrected values for the affected pin functions are provided in Table 3 (corrections in **bold**). Pin functions and assignments that are not shown in this table may be assumed to be correct in the original device data sheet. In addition, the fully multiplexed pin names, shown in the package diagrams at the beginning of the data sheet, may be assumed to be correct.

TABLE 3: PIC24FV32KA304 FAMILY AMENDED PINOUTS

Function	F					FV				
	Pin Number					Pin Number				
	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN	20-Pin PDIP/ SSOP/ SOIC	28-Pin SPDIP/ SSOP/ SOIC	28-Pin QFN	44-Pin QFN/ TQFP	48-Pin UQFN
CTED1	**14**	20	17	7	7	11	2	27	19	21
CTED2	**15**	**23**	**20**	**10**	**11**	**15**	**23**	**20**	**10**	**11**
CTED3	—	**19**	**16**	**6**	**6**	—	**19**	**16**	**6**	**6**
CTED4	**13**	**18**	**15**	**1**	**1**	**13**	**18**	**15**	**1**	**1**
CTED5	**17**	**25**	**22**	**14**	**15**	**17**	**25**	**22**	**14**	**15**
CTED6	**18**	**26**	**23**	**15**	**16**	**18**	**26**	**23**	**15**	**16**
CTED7	**—**	**—**	**—**	**5**	**5**	**—**	**—**	**—**	**5**	**5**
CTED8	**—**	**—**	**—**	**13**	**14**	**—**	**—**	**—**	**13**	**14**
CTED9	**—**	**22**	**19**	**9**	**10**	**—**	**22**	**19**	**9**	**10**
CTED10	**12**	**17**	**14**	**44**	**48**	**12**	**17**	**14**	**44**	**48**
CTED11	—	**21**	**18**	**8**	**9**	—	**21**	**18**	**8**	**9**
CTED12	**5**	**5**	**2**	**22**	**24**	**5**	**5**	**2**	**22**	**24**
CTED13	**6**	**6**	**3**	**23**	**25**	**6**	**6**	**3**	**23**	**25**
IC1	**14**	19	16	6	6	11	19	16	6	6
OC1	**14**	20	17	7	7	11	16	13	43	47
OC3	5	**21**	**18**	**12**	**13**	5	**21**	**18**	**12**	**13**
OFCB	16	24	21	**32**	**35**	16	24	21	**32**	**35**
PGEC2	2	**22**	**19**	**9**	**10**	2	**22**	**19**	**9**	**10**
PGED2	3	**21**	**18**	**8**	**9**	3	**21**	**18**	**8**	**9**
PGEC3	10	**15**	**12**	**42**	**46**	10	**15**	**12**	**42**	**46**
PGED3	9	**14**	**11**	**41**	**45**	9	**14**	**11**	**41**	**45**
SCK1	15	**22**	**19**	**9**	**10**	15	**22**	**19**	**9**	**10**
SCK2	2	**14**	**11**	**38**	**41**	2	**14**	**11**	**38**	**41**
SCL2	18	**7**	**4**	**24**	**26**	18	**7**	**4**	**24**	**26**
SDI1	17	**21**	**18**	**8**	**9**	17	**21**	**18**	**8**	**9**
SDI2	4	**19**	**16**	**36**	**39**	4	**19**	**16**	**36**	**39**
SDO2	3	**15**	**12**	**37**	**40**	3	**15**	**12**	**37**	**40**
$\overline{SS2}$	15	23	20	**35**	**38**	15	23	20	**35**	**38**
U1RX	6	6	3	**2**	**2**	6	6	3	**2**	**2**
U1TX	11	16	13	**3**	**3**	11	16	13	**3**	**3**

3. Module: A/D Converter

In Figure 22-2, the CHOLD capacitor is listed with an incorrect value. The correct value is 32 pF.

4. Module: A/D Converter

Bit 10 of AD1CON1, previously labelled as reserved in the Device Data Sheet (DS39995**B**), is actually implemented as a control bit. This bit, MODE12, selects the module's operating resolution.

Register 22-1 is amended, as shown below (changes in **bold**). Only the relevant portions of the register are shown.

5. Module: A/D Converter

Certain values for the PVCFG bits (AD1CON2<15:14>) are not correctly defined in the Device Data Sheet (DS39995**B**). Register 22-2 is amended with the new definitions and additional footnotes 2 and 3, as shown below (changes in **bold**). Only the relevant portions of the register are shown.

6. Module: A/D Converter

For the AD1CHS register (Register 22-5), the text of Footnote 3 is amended to read (changes in **bold**):

"3. **The actual band gap value used is 2x or 4x the internal VBG, selected whenever PVCFG<1:0> = 1x**."

REGISTER 22-1: AD1CON1: A/D CONTROL REGISTER 1 (PARTIAL REPRESENTATION)

R/W-0	U-0	R/W-0	U-0	U-0	**R/W-0**	R/W-0	R/W-0
ADON	—	ADSIDL	—	—	**MODE12**	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0 HSC	R/C-0 HSC
SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE
bit 7							bit 0

bit 10 **MODE12: 12-Bit Operation Mode bit**
1 = 12-bit A/D operation
0 = 10-bit A/D operation

REGISTER 22-2: AD1CON2: A/D CONTROL REGISTER 2 (PARTIAL REPRESENTATION)

bit 15-14 **PVCFG<1:0>:** Converter Positive Voltage Reference Configuration bits
11 = **4 * Internal VBG(2)**
10 = **2 * Internal VBG(3)**
01 = External VREF+
00 = AVDD

Note 1: Only applicable when the buffer is used in FIFO mode (BUFREGEN = 0). In addition, BUFS is only used when BUFM = 1.
2: Voltage reference setting will not be within specification with VDD below 4.5V.
3: Voltage reference setting will not be within specification with VDD below 2.3V.

7. Module: A/D Converter

In **Section 22.3 "Transfer Function"**, the text of the final bullet point is corrected to read:

- An input voltage greater than (V_{R-}) + (4095 ((V_{R+}) – (V_{R-}))/4096) converts as 1111 1111 1111.

8. Module: Comparator

In Register 23-1, the description of the CCH bits is corrected for CCH<1:0> = 11. This option is changed to V_{BG}, instead of $V_{BG}/2$.

9. Module: Comparator

In Register 23-2, the description of the CMIDL bit's function has been updated for CMIDL = 1. The new descriptive text reads: "Disable comparator interrupts in Idle mode; enabled comparators remain operational."

10. Module: Flash Program Memory

In Examples 5-2 and 5-4, the statement defining the variable, `offset`, is changed to provide the correct syntax in C. This is shown in context in Example 1 (change in **bold**). The change is identical for both code examples.

EXAMPLE 1: CHANGES TO EXAMPLES 5-2 AND 5-4

```
// Set up pointer to the first memory location to be written
    TBLPAG = __builtin_tblpage(&progAddr);    // Initialize PM Page Boundary SFR
    offset = __builtin_tbloffset(&progAddr); // Initialize lower word of address
```

11. Module: Electrical Specifications

In Table 29-28, incorrect values for the clock parameters, AD50, AD51 and AD60, are shown. The correct values are shown below. Also, the values for the conversion time, AD55, have been clarified and augmented to specify 10 and 12-bit operation. Changes are in **bold**; the bold in the original is removed for clarity.

All other information in the table remains unchanged.

TABLE 29-28: ADC CONVERSION TIMING REQUIREMENTS (PARTIAL REPRESENTATION)

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V PIC24F32KA3XX 2.0V to 5.5V PIC24FV32KA3XX Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period	**600**	—	—	ns	TCY = **600** ns, AD1CON3 in default state
AD51	TRC	ADC Internal RC Oscillator Period	—	**1.67**	—	**μs**	
AD55	TCONV	Conversion Time	— —	**12** **14**	— —	TAD TAD	**10-bit result** **12-bit result**
AD60	TDIS	Discharge Time	**12**	**—**	—	**TAD**	

12. Module: A/D Converter

The description of CSCNA (AD1CON2<10>) needs to be modified. The description should read (changes in **bold**):

CSCNA: Scan Input Selections for CH0+ **S/H Input for MUX A Input Multiplexer Setting** bit

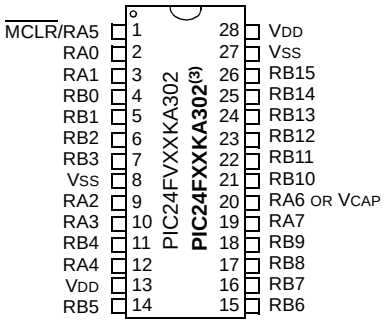
1 = Scan inputs
0 = Do not scan inputs

13. Module: Pin Diagrams

In the Pin Diagrams at the beginning of the data sheet, the following pinouts need to be modified. The correct pin changes are shown in **bold**; the bold in the original diagram is removed for clarity. All other information in the pin features remains unchanged.

Pin Diagrams

28-Pin SPDIP/SSOP/SOIC(1,2)



Pin	Pin Features	
	PIC24FVXXKA302	PIC24FXXKA302
1	MCLR/VPP/RA5	MCLR/VPP/RA5
2	VREF+/CVREF+/AN0/C3INC/CTED1/CN2/RA0	**VREF+/CVREF+/AN0/C3INC/CN2/RA0(3)**
3	CVREF-/VREF-/AN1/CN3/RA1	CVREF-/VREF-/AN1/CN3/RA1
4	PGED1/AN2/ULPWU/CTCMP/C1IND/C2INB/C3IND/U2TX/CN4/RB0	PGED1/AN2/ULPWU/CTCMP/C1IND/C2INB/C3IND/U2TX/CN4/RB0
5	PGEC1/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1	PGEC1/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1
6	AN4/C1INB/C2IND/SDA2/T5CK/T4CK/U1RX/CTED13/CN6/RB2	AN4/C1INB/C2IND/SDA2/T5CK/T4CK/U1RX/CTED13/CN6/RB2
7	AN5/C1INA/C2INC/SCL2/CN7/RB3	AN5/C1INA/C2INC/SCL2/CN7/RB3
8	VSS	VSS
9	OSCI/AN13/CLKI/CN30/RA2	OSCI/AN13/CLKI/CN30/RA2
10	OSCO/AN14/CLKO/CN29/RA3	OSCO/AN14/CLKO/CN29/RA3
11	SOSCI/AN15/U2RTS/CN1/RB4	SOSCI/AN15/U2RTS/CN1/RB4
12	SOSCO/SCLKI/U2CTS/CN0/RA4	SOSCO/SCLKI/U2CTS/CN0/RA4
13	VDD	VDD
14	PGED3/ASDA(1)/SCK2/CN27/RB5	PGED3/ASDA(1)/SCK2/CN27/RB5
15	PGEC3/ASCL(1)/SDO2/CN24/RB6	PGEC3/ASCL(1)/SDO2/CN24/RB6
16	U1TX/C2OUT/OC1/INT0/CN23/RB7	U1TX/INT0/CN23/RB7
17	SCL1/U1CTS/C3OUT/CTED10/CN22/RB8	SCL1/U1CTS/C3OUT/CTED10/CN22/RB8
18	SDA1/T1CK/U1RTS/IC2/CTED4/CN21/RB9	SDA1/T1CK/U1RTS/IC2/CTED4/CN21/RB9
19	SDI2/IC1/CTED3/CN9/RA7	SDI2/IC1/CTED3/CN9/RA7
20	VCAP	C2OUT/OC1/CTED1/INT2/CN8/RA6
21	PGED2/SDI1/OC3/CTED11/CN16/RB10	PGED2/SDI1/OC3/CTED11/CN16/RB10
22	PGEC2/SCK1/OC2/CTED9/CN15/RB11	PGEC2/SCK1/OC2/CTED9/CN15/RB11
23	AN12/LVDIN/SS2/IC3/CTED2/INT2/CN14/RB12	AN12/LVDIN/SS2/IC3/CTED2/CN14/RB12
24	AN11/SDO1/OCFB/CTPLS/CN13/RB13	AN11/SDO1/OCFB/CTPLS/CN13/RB13
25	CVREF/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14	CVREF/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14
26	AN9/C3INA/T3CK/T2CK/REFO/SS1/CTED6/CN11/RB15	AN9/C3INA/T3CK/T2CK/REFO/SS1/CTED6/CN11/RB15
27	VSS/AVSS	VSS/AVSS
28	VDD/AVDD	VDD/AVDD

Legend: Pin numbers in bold indicate pin function differences between PIC24FV and PIC24F devices.

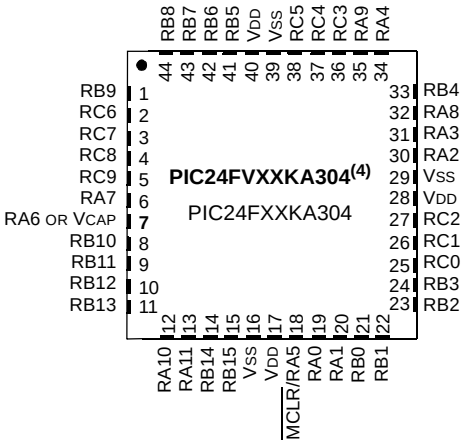
Note 1: Alternative multiplexing for SDA1(ASDA1) and SCL1 (ASCL1) when the I2CSEL Configuration bit is set.

2: PIC24F32KA304 device pins have a maximum voltage of 3.6V and are not 5V tolerant.

3: CTED1 has been removed from Pin 2 of the PIC24FXXKA302 device. There are no changes made to the PIC24FVXXKA302 pin features.

Pin Diagrams

44-Pin TQFP/QFN(1,2,3)



Legend: Pin numbers in **bold** indicate pin function differences between PIC24FV and PIC24F devices.

Note 1: Exposed pad on underside of device is connected to VSS.

2: Alternative multiplexing for SDA1 (ASDA1) and SCL1 (ASCL1) when the I2CSEL Configuration bit is set.

3: PIC24F32KA304 device pins have a maximum voltage of 3.6V and are not 5V tolerant.

4: The OC1 feature is included on Pin 43 of the PIC24FVXXKA302 device. There are no changes made to the PIC24FXXKA302 pin features.

Pin	Pin Features	
	PIC24FVXXKA304	PIC24FXXKA304
1	SDA1/T1CK/U1RTS/CTED4/CN21/RB9	SDA1/T1CK/U1RTS/CTED4/CN21/RB9
2	U1RX/CN18/RC6	U1RX/CN18/RC6
3	U1TX/CN17/RC7	U1TX/CN17/RC7
4	OC2/CN20/RC8	OC2/CN20/RC8
5	IC2/CTED7/CN19/RC9	IC2/CTED7/CN19/RC9
6	IC1/CTED3/CN9/RA7	IC1/CTED3/CN9/RA7
7	VCAP	C2OUT/OC1/CTED1/INT2/CN8/RA6
8	PGED2/SDI1/CTED11/CN16/RB10	PGED2/SDI1/CTED11/CN16/RB10
9	PGEC2/SCK1/CTED9/CN15/RB11	PGEC2/SCK1/CTED9/CN15/RB11
10	AN12/LVDIN/CTED2/INT2/CN14/RB12	AN12/LVDIN/CTED2/CN14/RB12
11	AN11/SDO1/CTPLS/CN13/RB13	AN11/SDO1/CTPLS/CN13/RB13
12	OC3/CN35/RA10	OC3/CN35/RA10
13	IC3/CTED8/CN36/RA11	IC3/CTED8/CN36/RA11
14	CVREF/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14	CVREF/AN10/C3INB/RTCC/C1OUT/OCFA/CTED5/INT1/CN12/RB14
15	AN9/C3INA/T3CK/T2CK/REFO/SS1/CTED6/CN11/RB15	AN9/C3INA/T3CK/T2CK/REFO/SS1/CTED6/CN11/RB15
16	VSS/AVSS	VSS/AVSS
17	VDD/AVDD	VDD/AVDD
18	MCLR/VPP/RA5	MCLR/VPP/RA5
19	VREF+/CVREF+/AN0/C3INC/CTED1/CN2/RA0	VREF+/CVREF+/AN0/C3INC/CN2/RA0
20	CVREF-/VREF-/AN1/CN3/RA1	CVREF-/VREF-/AN1/CN3/RA1
21	PGED1/AN2/ULPWU/CTCMP/C1IND/C2INB/C3IND/U2TX/CN4/RB0	PGED1/AN2/ULPWU/CTCMP/C1IND/C2INB/C3IND/U2TX/CN4/RB0
22	PGEC1/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1	PGEC1/AN3/C1INC/C2INA/U2RX/CTED12/CN5/RB1
23	AN4/C1INB/C2IND/SDA2/T5CK/T4CK/CTED13/CN6/RB2	AN4/C1INB/C2IND/SDA2/T5CK/T4CK/CTED13/CN6/RB2
24	AN5/C1INA/C2INC/SCL2/CN7/RB3	AN5/C1INA/C2INC/SCL2/CN7/RB3
25	AN6/CN32/RC0	AN6/CN32/RC0
26	AN7/CN31/RC1	AN7/CN31/RC1
27	AN8/CN10/RC2	AN8/CN10/RC2
28	VDD	VDD
29	VSS	VSS
30	OSCI/AN13/CLKI/CN30/RA2	OSCI/AN13/CLKI/CN30/RA2
31	OSCO/AN14/CLKO/CN29/RA3	OSCO/AN14/CLKO/CN29/RA3
32	OCFB/CN33/RA8	OCFB/CN33/RA8
33	SOSCI/AN15/U2RTS/CN1/RB4	SOSCI/AN15/U2RTS/CN1/RB4
34	SOSCO/SCLKI/U2CTS/CN0/RA4	SOSCO/SCLKI/U2CTS/CN0/RA4
35	SS2/CN34/RA9	SS2/CN34/RA9
36	SDI2/CN28/RC3	SDI2/CN28/RC3
37	SDO2/CN25/RC4	SDO2/CN25/RC4
38	SCK2/CN26/RC5	SCK2/CN26/RC5
39	VSS	VSS
40	VDD	VDD
41	PGED3/ASDA1(2)/CN27/RB5	PGED3/ASDA1(2)/CN27/RB5
42	PGEC3/ASCL1(2)/CN24/RB6	PGEC3/ASCL1(2)/CN24/RB6
43	**INT0/OC1/CN23/RB7(4)**	INT0/CN23/RB7
44	SCL1/U1CTS/C3OUT/CTED10/CN22/RB8	SCL1/U1CTS/C3OUT/CTED10/CN22/RB8

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (3/2011)

Initial release of this document; issued for revision A4. Includes silicon issues 1 (Core, Low-Voltage Regulator) and 2 (Reset, BOR).

Rev B Document (5/2011)

Adds silicon issue 3 (A/D, Threshold Detect) to silicon revision A4.

Adds data sheet clarifications 1 (Overview and Other Locations), 2 (Overview) and 3 (A/D, Threshold Detect) for data sheet revision B.

Rev C Document (9/2011)

Adds silicon issues 4 (UART, TX Buffer), 5 (UART, Transmit), 6 (A/D, Threshold Detect), 7 (A/D, Threshold Detect) and 8 (HLVD, DC18 Value Changes) to silicon revision A4. Typographical correction in issue 1 (Core, Low-Voltage Regulator).

Adds data sheet clarifications 4 through 7 (A/D Converter), 8 and 9 (Comparator), 10 (Flash Program Memory), 11 (Electrical Specifications), 12 (A/D Converter) and 13 (Pin Diagrams) to data sheet revision B.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

ISBN: 978-1-61341-600-6

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2009

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/02/11