Homework Assignment 8

CS/ECE 3810: Computer Organization
Oct 26, 2020

Sequential Circuits and Finite State Machine

Due Date: Nov 02, 2020
(100 points)

Important Notes:

- Solutions turned in must be your own. Please, mention references (if any) at the end of each question. *Please refrain from cheating.*
- All solutions must be accompanied by the equations used/logic/intermediate steps. Writing only the final answer will receive **zero** credits.
- Partial score of every question is dedicated to each correct final answer provided by you. Please ensure both your equation/logic and final answer are correct. Moreover, you are expected to provide explanation for your solutions.
- All units must be mentioned wherever required.
- Late submissions **(after 11:59PM on 11/02/2020)** will not be accepted.
- We encourage all solutions to be typed in for which you could use software programs like LaTeX, Microsoft Word etc. If you submit handwritten solutions, they must be readable by the TAs to receive credits.
- Submit a .pdf file containing your answers for questions: 1-4.

Adders. Different adder circuits were discussed in the class: full adder, carry ripple adder, and carry look-ahead adder. Carry-look ahead adders calculate one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.
Refer to slides #5-10 of the 'Sequential Circuits' lecture.

Question 1. In this question, consider the design of a 16-bit carry look-ahead adder as discussed in the class. Two levels of the propagate and generate signals are produced in groups of four for the inputs A and B, compute the following.
Note. The input carry to bit position 0 (Co) is zero.

A = 0000 1010 1100 0011 and B = 0101 0101 0111 0101

Question 1A. Calculate the propagate and generate signals (all p, g, P, and G signals).**(20 points)**

Generate signal: $a_i.b_i$
Propagate signal: $a_i + b_i$

A = 0000 1010 1100 0011
B = 0101 0101 0111 0101
g = 0000 0000 0100 0001
p = 0101 1111 1111 0111

P 0 1 1 0
G 0 0 1 0

Question 1B. Calculate the carry out of all 4-bit groups (C1, C2, C3, and C4).**(20 points)**

$C_{i+1} = G_i + P_i.C_i$

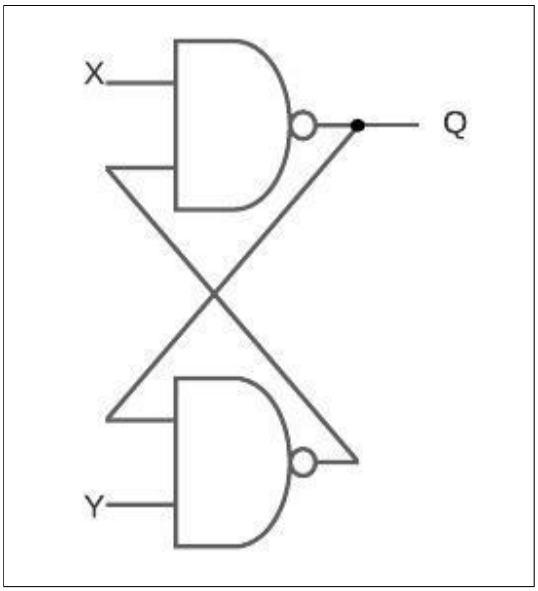
$C_0 = 0$ given
$C_1 = G_0 + P_0.C_0 = 0$
$C_2 = G_1 + P_1.C_1 = 1$
$C_3 = G_2 + P_2.C_2 = 1$
$C_4 = G_3 + P_3.C_3 = 0$

Latches. Latches sample inputs based on specific patterns and hold onto the sampled values until the next sample happens. Latches are used to create memory elements, such as flip-flops and registers, in microprocessors.
Refer to slides #16-18 of the 'Sequential Circuits' lecture

Truth table for NAND:

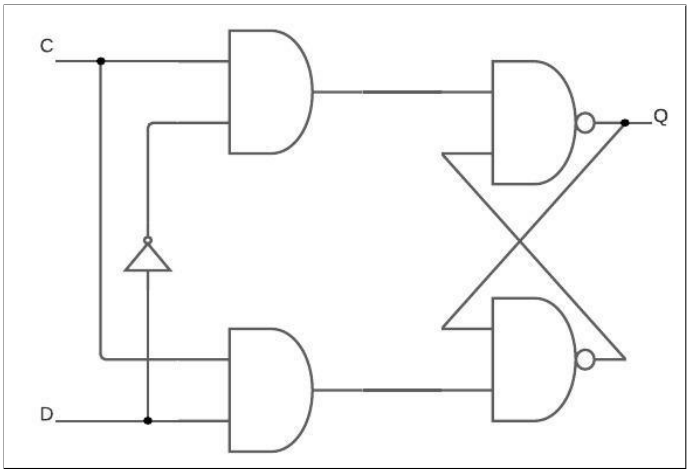
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

Question 2.A. Below is a variation of the set-reset latch discussed in the class. Compute the output (Q) for all four possible combinations of the inputs (X and Y) by filling the table below.
Note: Unlike the circuit discussed in the class, the following circuit does not have the output $\bar{Q}$ **(15 points)**



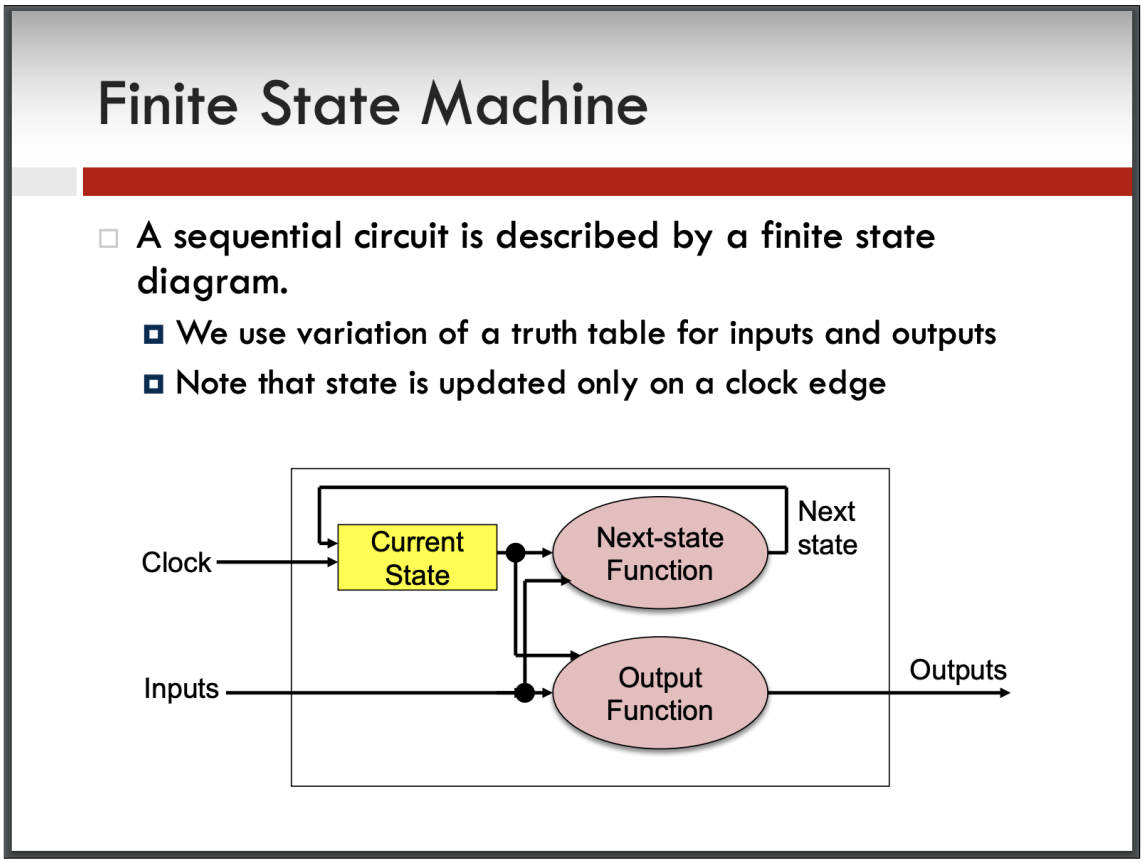
X	Y	Q
0	0	1
0	1	1
1	0	0
1	1	0

Question 2.B. Below is a logic circuit designed by a Computer Engineering student at the University of Utah. Compute the output (Q) of the circuit for all four possible combinations of the inputs (C and D) by filling the table below.
(15 points)



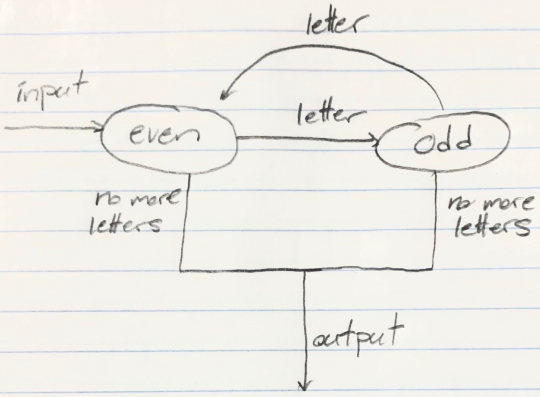
C	D	Q
0	0	1
0	1	1
1	0	0
1	1	1

Finite State Machine. A Finite State Machine is a computational model that can be used to simulate sequential logic. They are used to model problems in many fields, including mathematics and AI. The following two questions are based on FSM.

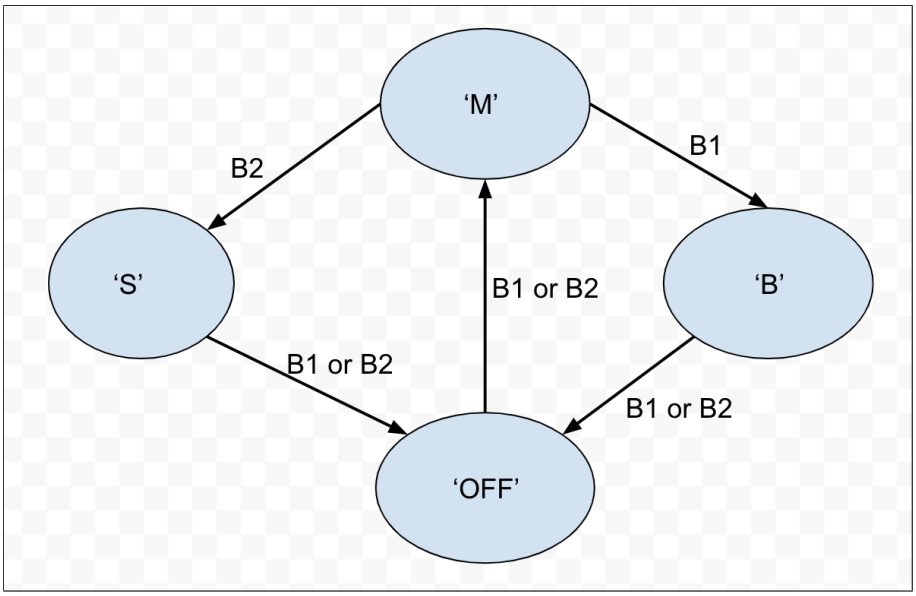


Question 3. Design a finite state machine (FSM) with two states (ODD and EVEN) that receives strings of any length containing only two letters a and b. At any given time, if the number of input letter 'a' is even, the state machine is at the EVEN state; otherwise; it is at the ODD state. Initially, the state machine is in the EVEN state. For example, after receiving all the letters in each of the strings aabaa and ababbb, your FSM should end up in the EVEN state; whereas for aaab and abbaaaa, it should be at the ODD state.
Note: For this question, hand drawn diagram submissions are allowed. However, please make sure that the drawings are legible. Lack of clarity in the drawings may result in a penalty. **(15 points)**

HW 8 Q3


letter
input
letter
even
Odd
no more letters
no more letters
output

Question 4. Imagine a scenario where your room has two buttons (B1 and B2) that control 3 lights in the room. By default, the state is: 'OFF'. When you press any of those 2 buttons, the room's main light (M) turns on ('M' state). In the 'M' state, if you press button B1, the room's main light turns off and the bed light (B) turns on ('B' state). But if you are in 'M' state and press button B2, the room's main light turns off and the study lamp(S) turns on('S' state). If you are in either states 'S' or 'B', pressing any of the two buttons, results in turning off the lights and transitioning to the 'OFF' state.



Question 4A. Carefully evaluate the Finite State machine diagram above that explains this scenario and complete the state table below, the 1st entry in the state table is added for your reference.**(10 points)**

State	Input	Output State
OFF	B1 Pressed	M
OFF	B2 Pressed	M
M	B1 Pressed	B
M	B2 Pressed	S
B	B1 Pressed	OFF
B	B2 Pressed	OFF
S	B1 Pressed	OFF
S	B2 Pressed	OFF

Question 4B. Starting from the 'B' state, find an input pattern with the minimum number of button presses to make the study lamp on ('S' state). **(5 points)**

B1 $\rightarrow$ B1 $\rightarrow$ B2 is the input pattern that gives:
B $\rightarrow$ OFF $\rightarrow$ M $\rightarrow$ S