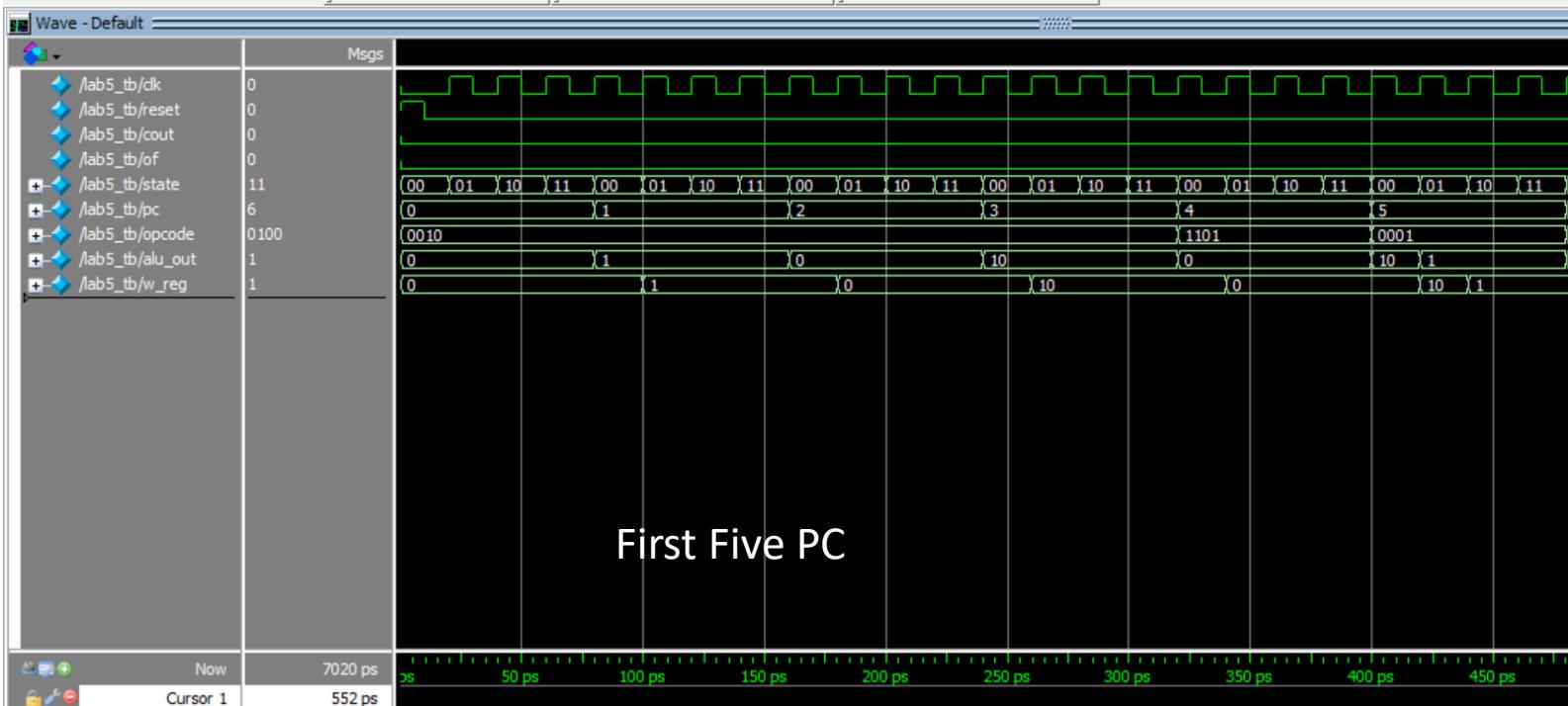


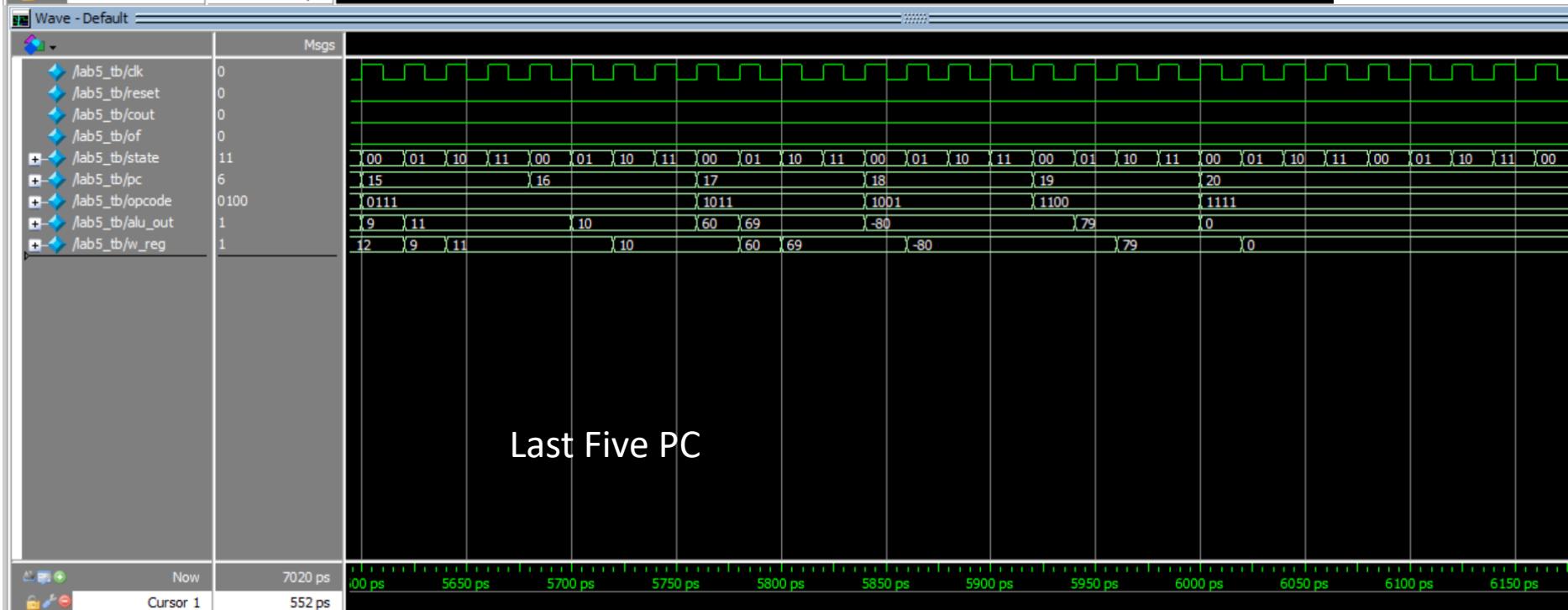
Lab 5: Microprocessor

Kyle Clark

Testbench Waveforms pt 3



First Five PC



Last Five PC

Pin Planner pt. 5

Pin Planner - C:/Users/Kyle/Documents/GitHub/EEE333Verilog/Lab 5 Microprocessor/lab5_pv - lab5_pv

File Edit View Processing Tools Window Help

Report not available

Groups Report

Tasks Early Pin Planning Early Pin Planning Run I/O Assignment

Top View - Wire Bond MAX 10 - 10M50DAF484C6GES

Symbol Pin Type

- User I/O
- User assi...
- Fitter assi...
- Unbonde...
- Reserved ...
- Other co...
- DEV_OE
- DEV_CLR
- DIFF_n

Filter: Pins: all

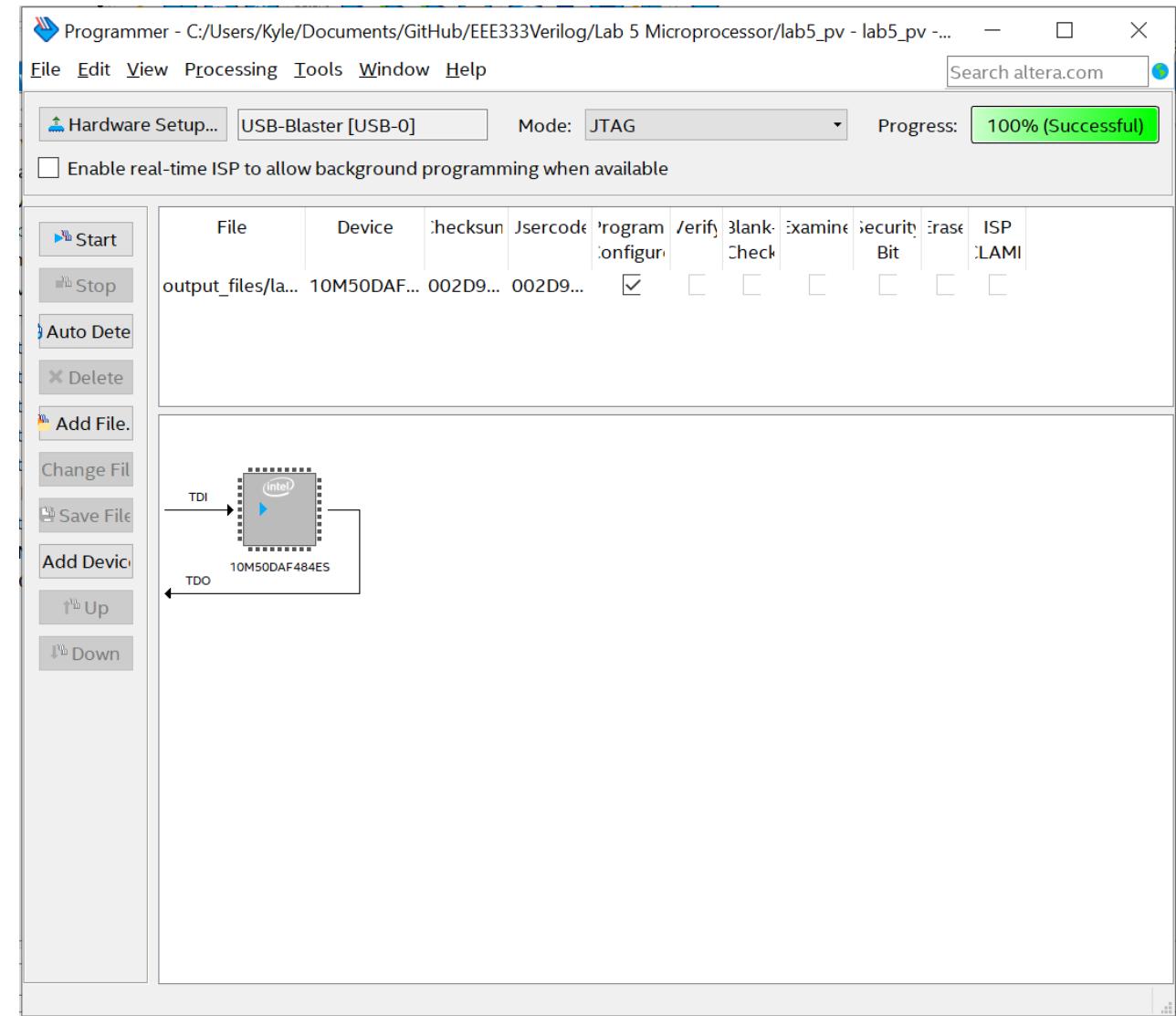
Node Name	Direction	Location	I/O Bank	R/REF Group	Iter Locatitc	I/O Standard	Reserved	Current Strength	Slew Rate	Differential P.	Alt Preserva
KEY0	Input	PIN_B8	7	B7_N0	PIN_B8	3.3...VTTL		8mA ..ult)			
LED0	Output	PIN_A8	7	B7_N0	PIN_A8	3.3...VTTL		8mA ..ult)	2 (default)		
LED1	Output	PIN_A9	7	B7_N0	PIN_A9	3.3...VTTL		8mA ..ult)	2 (default)		
LED2	Output	PIN_A10	7	B7_N0	PIN_A10	3.3...VTTL		8mA ..ult)	2 (default)		
LED3	Output	PIN_B10	7	B7_N0	PIN_B10	3.3...VTTL		8mA ..ult)	2 (default)		
LED4	Output	PIN_D13	7	B7_N0	PIN_D13	3.3...VTTL		8mA ..ult)	2 (default)		
LED5	Output	PIN_C13	7	B7_N0	PIN_C13	3.3...VTTL		8mA ..ult)	2 (default)		
LED6	Output	PIN_E14	7	B7_N0	PIN_E14	3.3...VTTL		8mA ..ult)	2 (default)		
LED7	Output	PIN_D14	7	B7_N0	PIN_D14	3.3...VTTL		8mA ..ult)	2 (default)		
SW0	Input	PIN_C10	7	B7_N0	PIN_C10	3.3...VTTL		8mA ..ult)			
SW1	Input	PIN_C11	7	B7_N0	PIN_C11	3.3...VTTL		8mA ..ult)			
SW2	Input	PIN_D12	7	B7_N0	PIN_D12	3.3...VTTL		8mA ..ult)			
SW3	Input	PIN_C12	7	B7_N0	PIN_C12	3.3...VTTL		8mA ..ult)			
SW4	Input	PIN_A12	7	B7_N0	PIN_A12	3.3...VTTL		8mA ..ult)			
SevSeg0[6]	Output	PIN_C17	7	B7_N0	PIN_C17	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg0[5]	Output	PIN_D17	7	B7_N0	PIN_D17	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg0[4]	Output	PIN_E16	7	B7_N0	PIN_E16	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg0[3]	Output	PIN_C16	7	B7_N0	PIN_C16	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg0[2]	Output	PIN_C15	7	B7_N0	PIN_C15	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg0[1]	Output	PIN_E15	7	B7_N0	PIN_E15	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg0[0]	Output	PIN_C14	7	B7_N0	PIN_C14	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg1[6]	Output	PIN_B17	7	B7_N0	PIN_B17	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg1[5]	Output	PIN_A18	7	B7_N0	PIN_A18	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg1[4]	Output	PIN_A17	7	B7_N0	PIN_A17	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg1[3]	Output	PIN_B16	7	B7_N0	PIN_B16	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg1[2]	Output	PIN_E18	6	B6_N0	PIN_E18	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg1[1]	Output	PIN_D18	6	B6_N0	PIN_D18	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg1[0]	Output	PIN_C18	7	B7_N0	PIN_C18	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg2[6]	Output	PIN_B22	6	B6_N0	PIN_B22	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg2[5]	Output	PIN_C22	6	B6_N0	PIN_C22	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg2[4]	Output	PIN_B21	6	B6_N0	PIN_B21	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg2[3]	Output	PIN_A21	6	B6_N0	PIN_A21	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg2[2]	Output	PIN_B19	7	B7_N0	PIN_B19	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg2[1]	Output	PIN_A20	7	B7_N0	PIN_A20	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg2[0]	Output	PIN_B20	6	B6_N0	PIN_B20	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg3[6]	Output	PIN_E17	6	B6_N0	PIN_E17	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg3[5]	Output	PIN_D19	6	B6_N0	PIN_D19	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg3[4]	Output	PIN_C20	6	B6_N0	PIN_C20	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg3[3]	Output	PIN_C19	7	B7_N0	PIN_C19	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg3[2]	Output	PIN_E21	6	B6_N0	PIN_E21	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg3[1]	Output	PIN_E22	6	B6_N0	PIN_E22	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg3[0]	Output	PIN_F21	6	B6_N0	PIN_F21	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg4[6]	Output	PIN_F20	6	B6_N0	PIN_F20	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg4[5]	Output	PIN_F19	6	B6_N0	PIN_F19	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg4[4]	Output	PIN_H19	6	B6_N0	PIN_H19	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg4[3]	Output	PIN_J18	6	B6_N0	PIN_J18	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg4[2]	Output	PIN_E19	6	B6_N0	PIN_E19	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg4[1]	Output	PIN_E20	6	B6_N0	PIN_E20	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg4[0]	Output	PIN_F18	6	B6_N0	PIN_F18	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg5[6]	Output	PIN_N20	6	B6_N0	PIN_N20	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg5[5]	Output	PIN_N19	6	B6_N0	PIN_N19	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg5[4]	Output	PIN_M20	6	B6_N0	PIN_M20	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg5[3]	Output	PIN_N18	6	B6_N0	PIN_N18	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg5[2]	Output	PIN_L18	6	B6_N0	PIN_L18	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg5[1]	Output	PIN_K20	6	B6_N0	PIN_K20	3.3...VTTL		8mA ..ult)	2 (default)		
SevSeg5[0]	Output	PIN_J20	6	B6_N0	PIN_J20	3.3...VTTL		8mA ..ult)	2 (default)		
<<new node>>	Input	PIN_P11	3	B3_N0	PIN_P11	3.3...VTTL					

0% 00:00:00

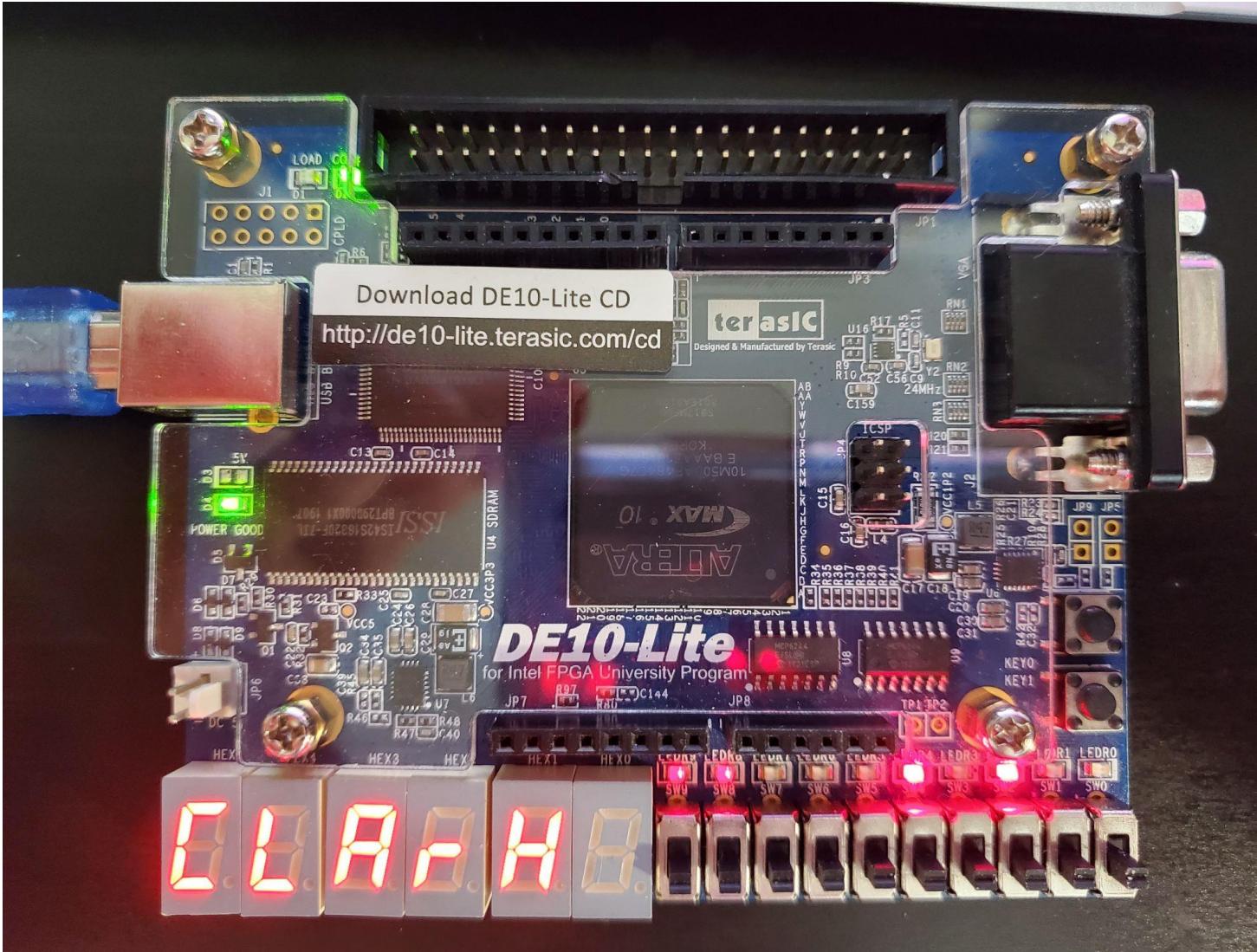
Flow Summary & Program pt. 6

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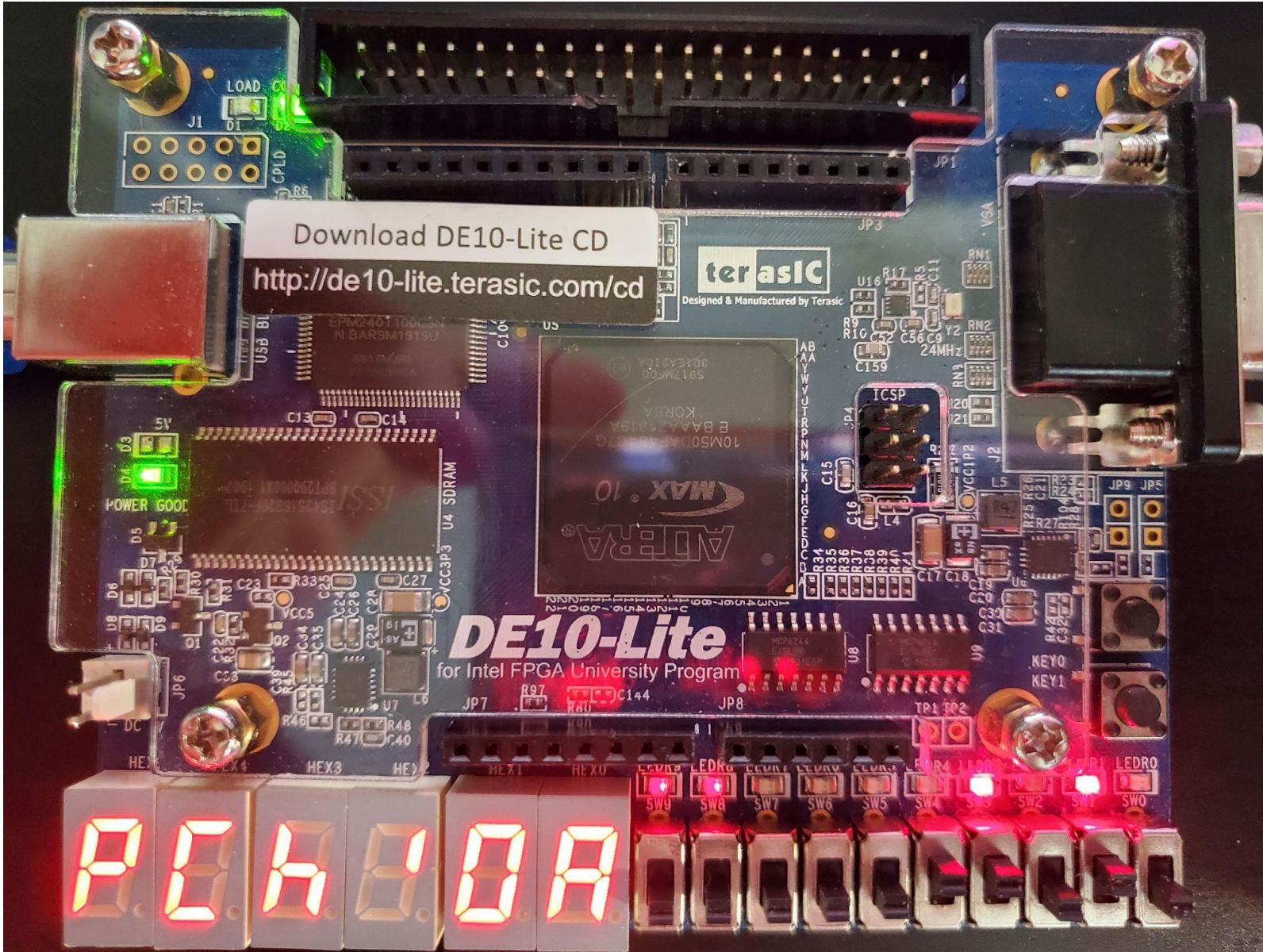
Flow Summary	
Flow Status	Successful - Wed Jul 06 18:15:10 2022
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	lab5_pv
Top-level Entity Name	lab5_pv
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	586 / 49,760 (1 %)
Total registers	179
Total pins	57 / 360 (16 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	1 / 288 (< 1 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)



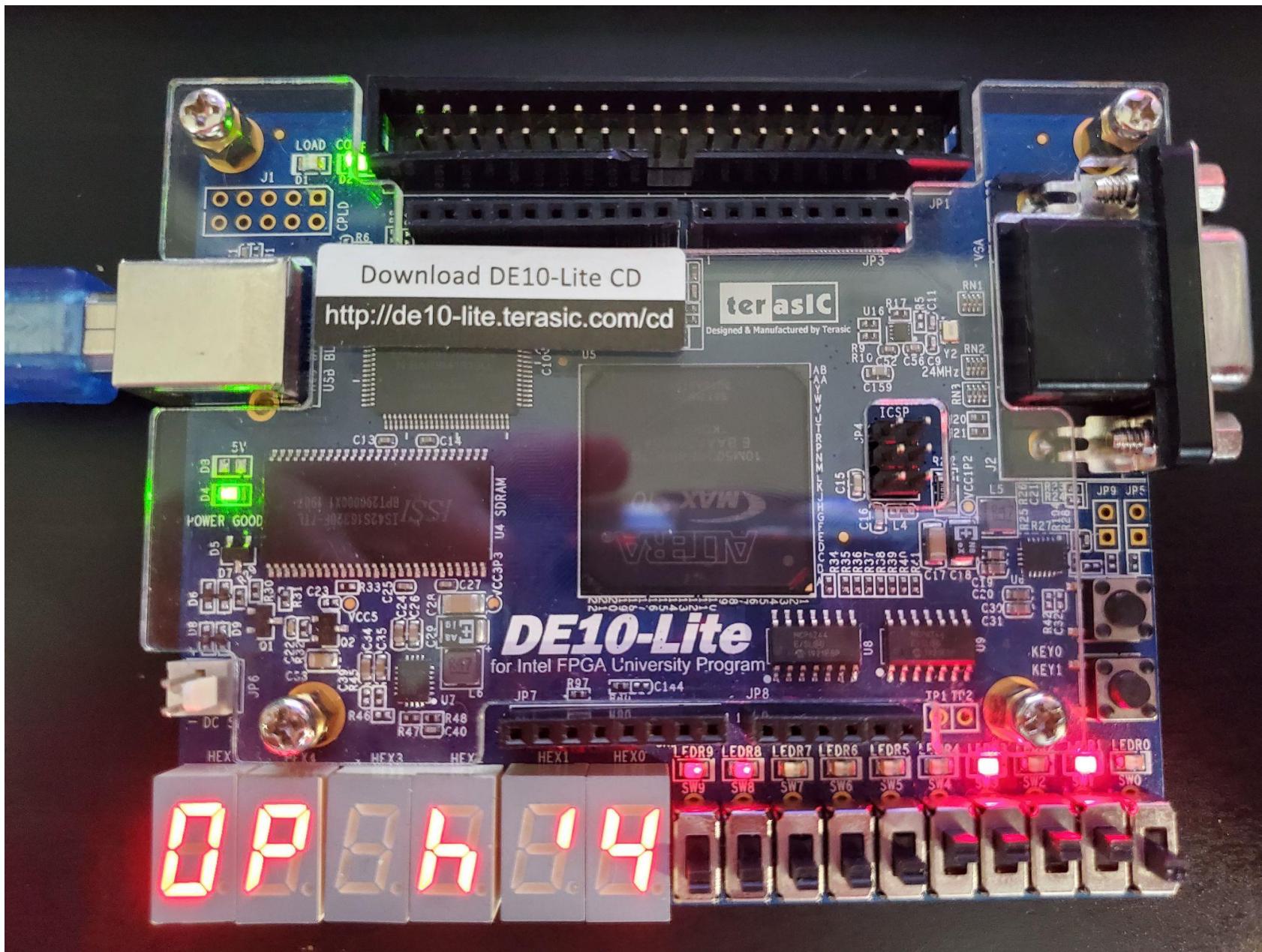
Physical Validation pt. 7



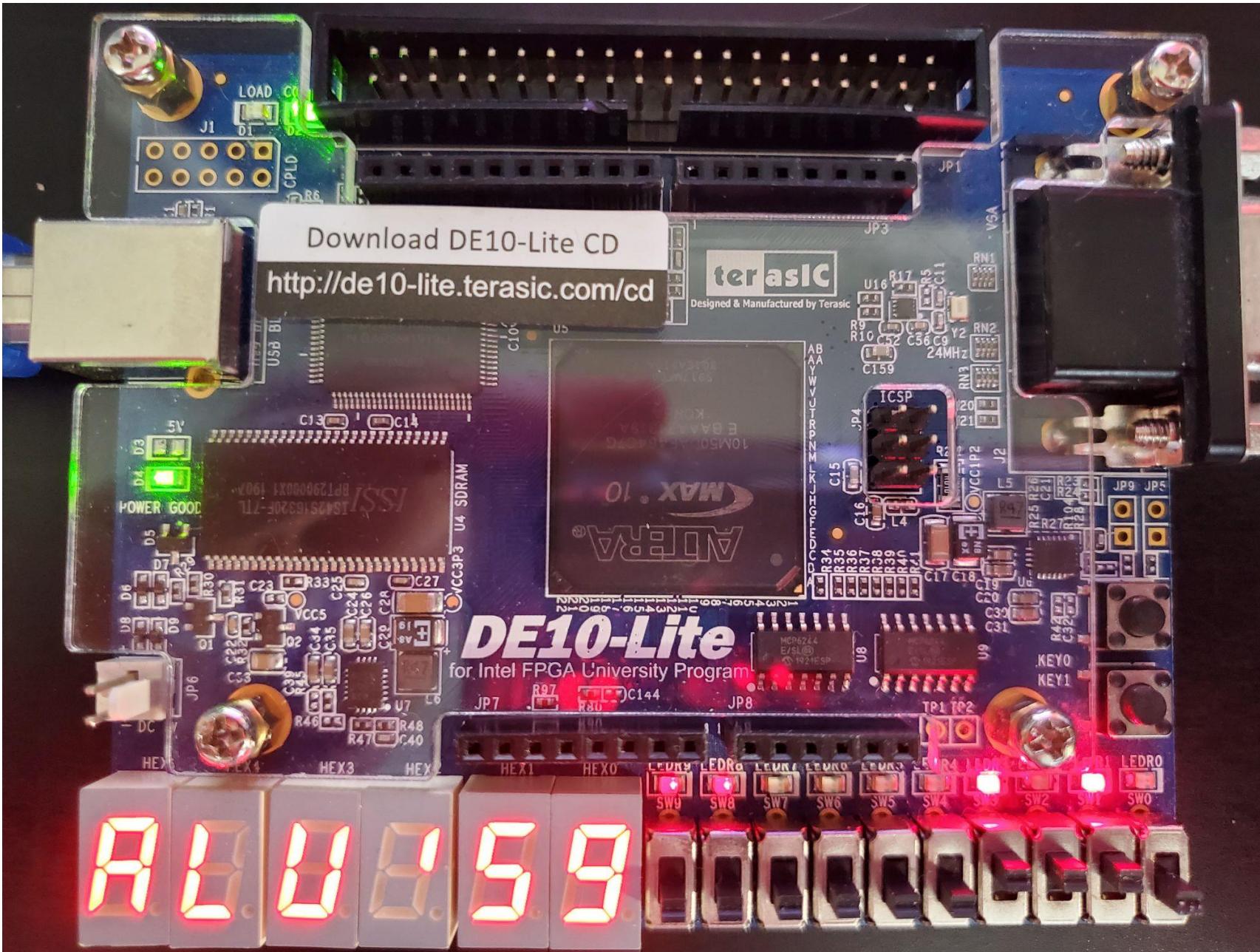
PC: h'0A



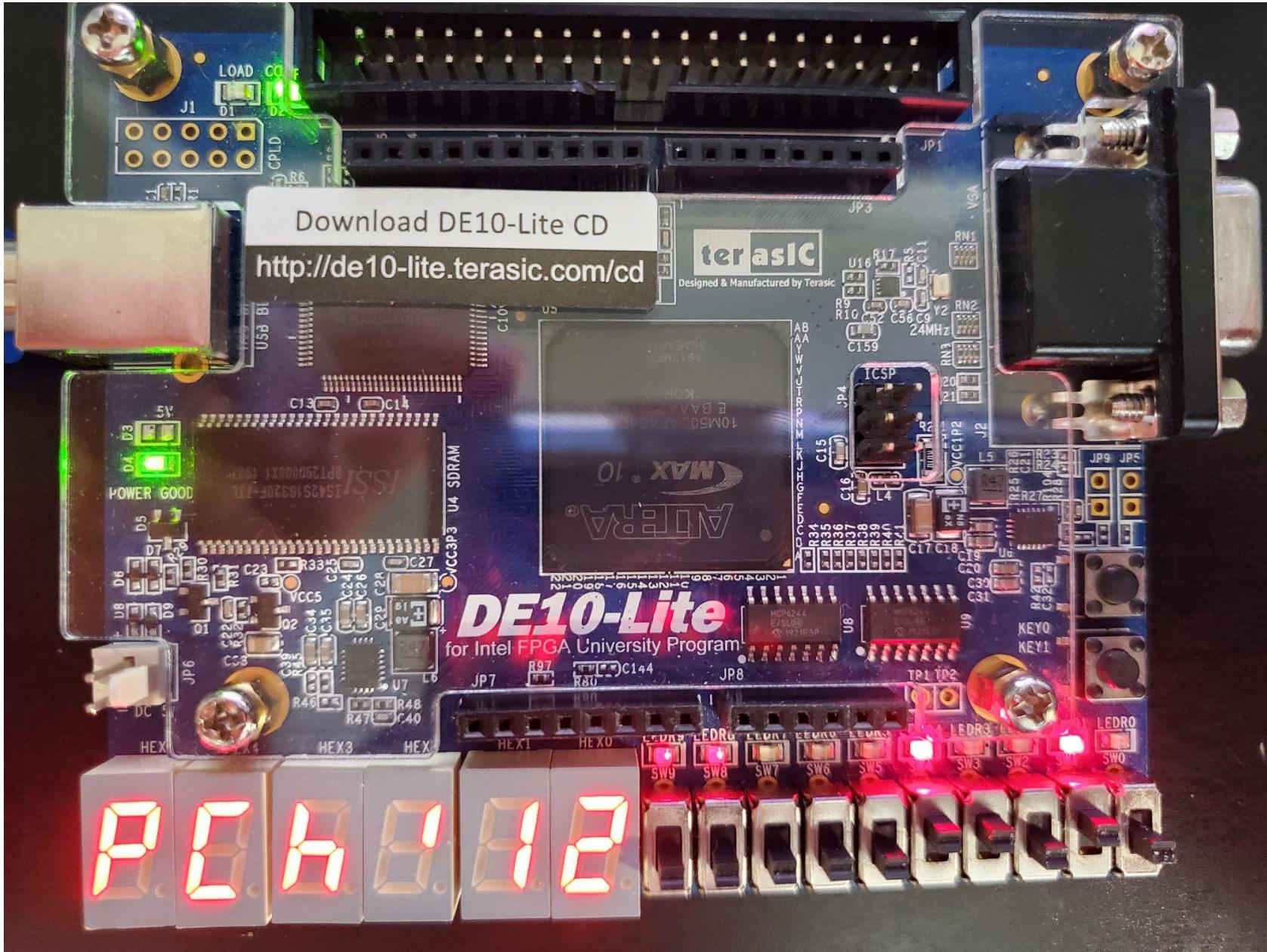
PC: h'0A



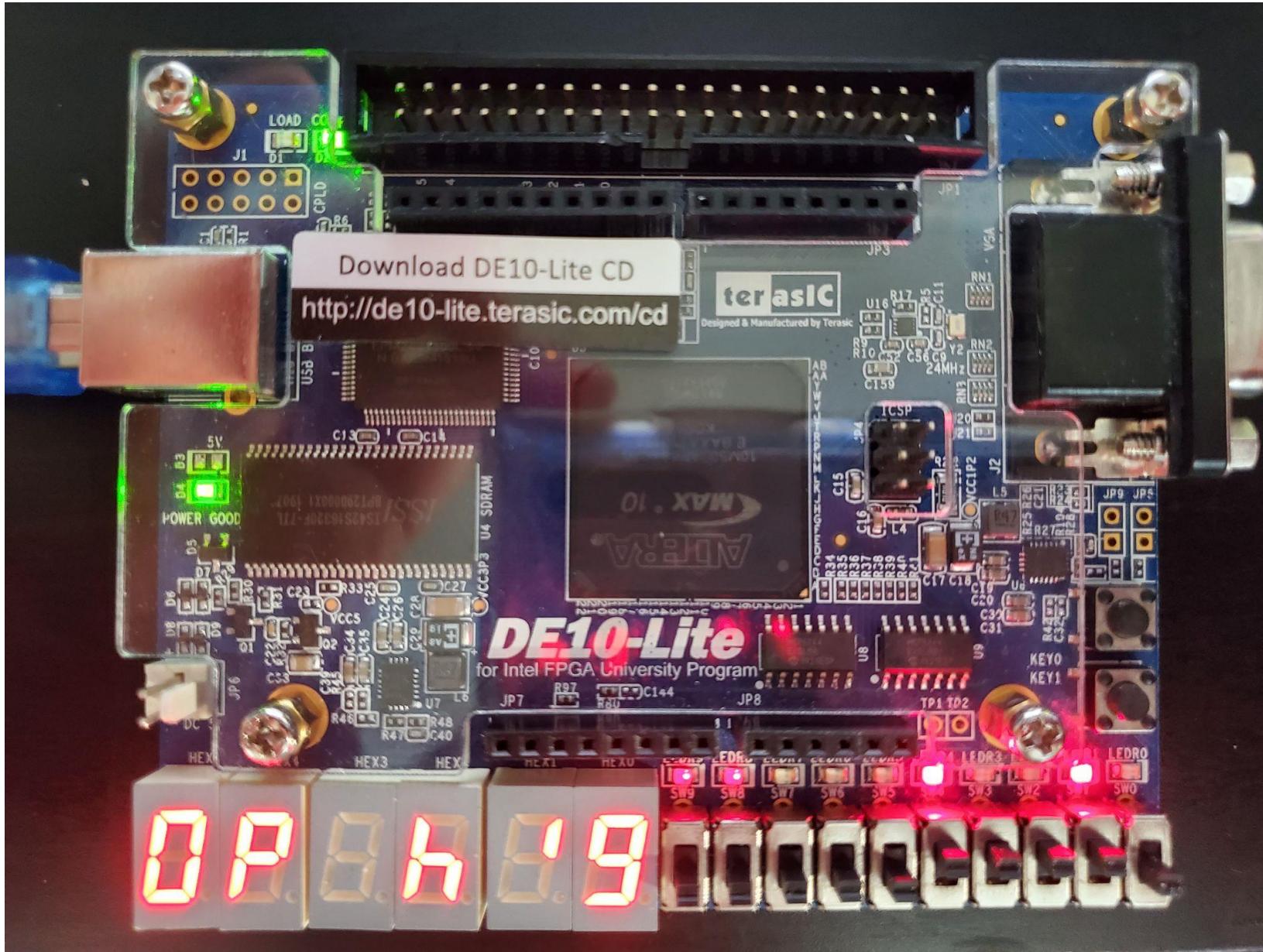
PC: h'0A



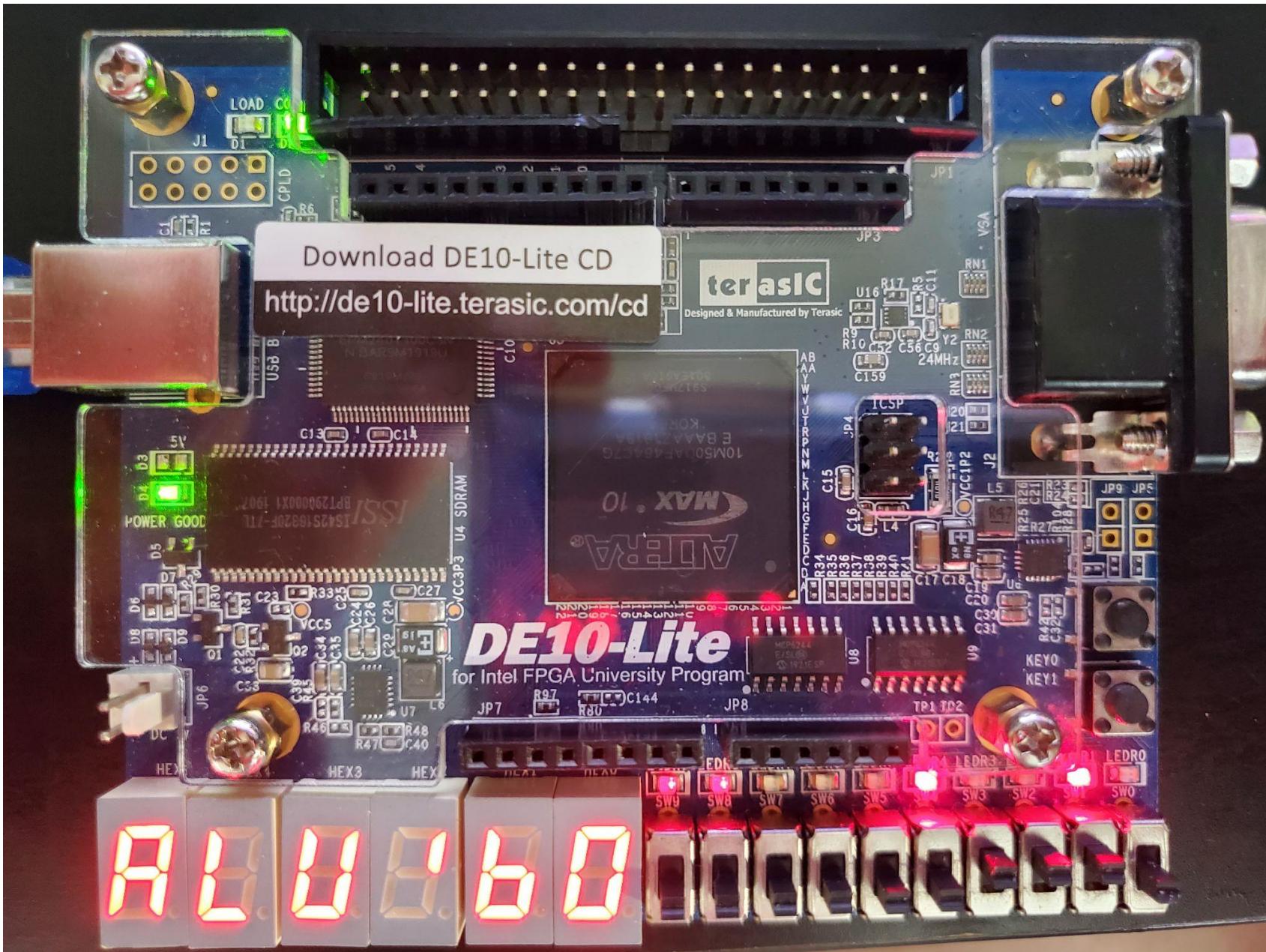
PC: h'12



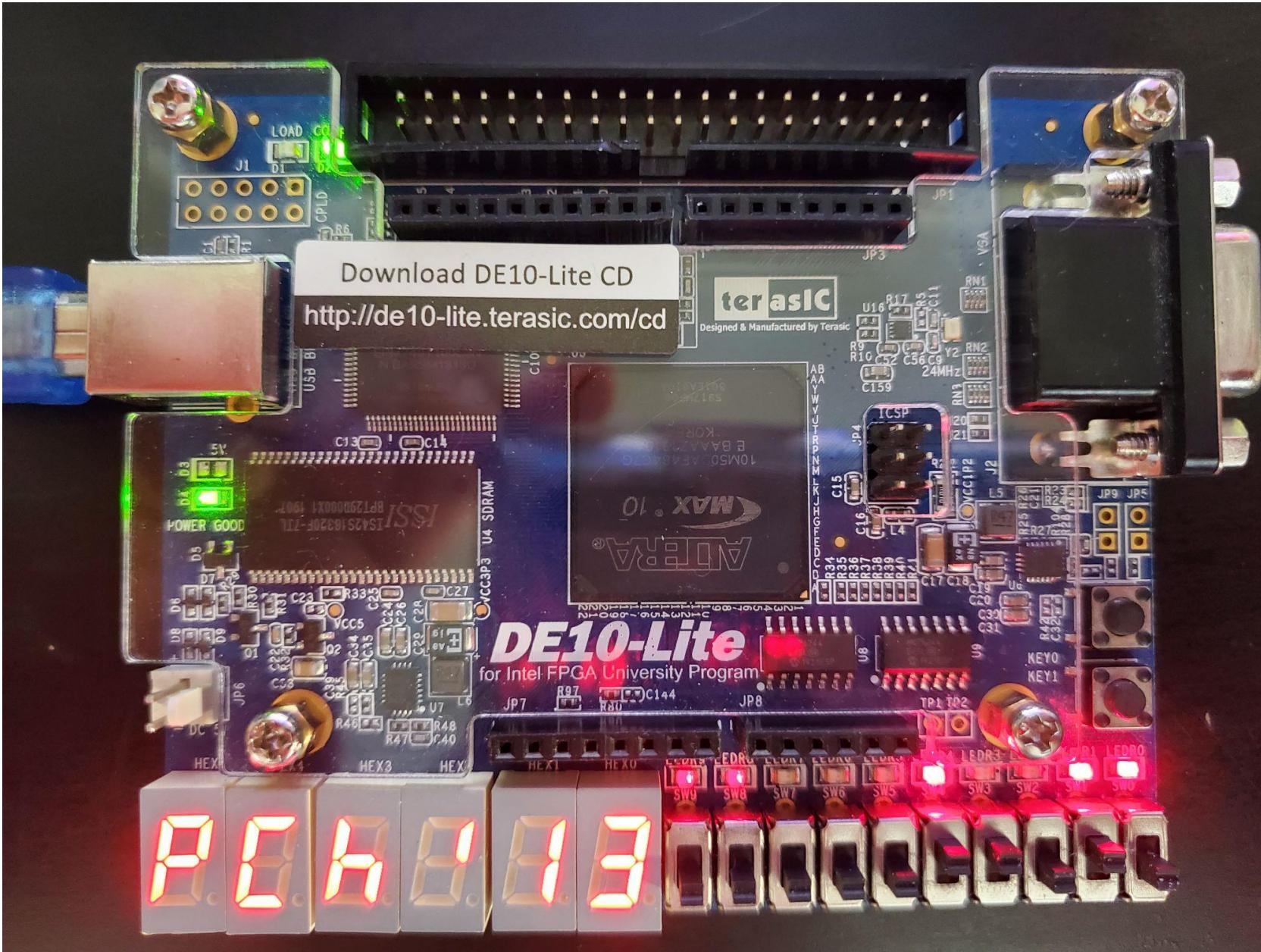
PC: h'12



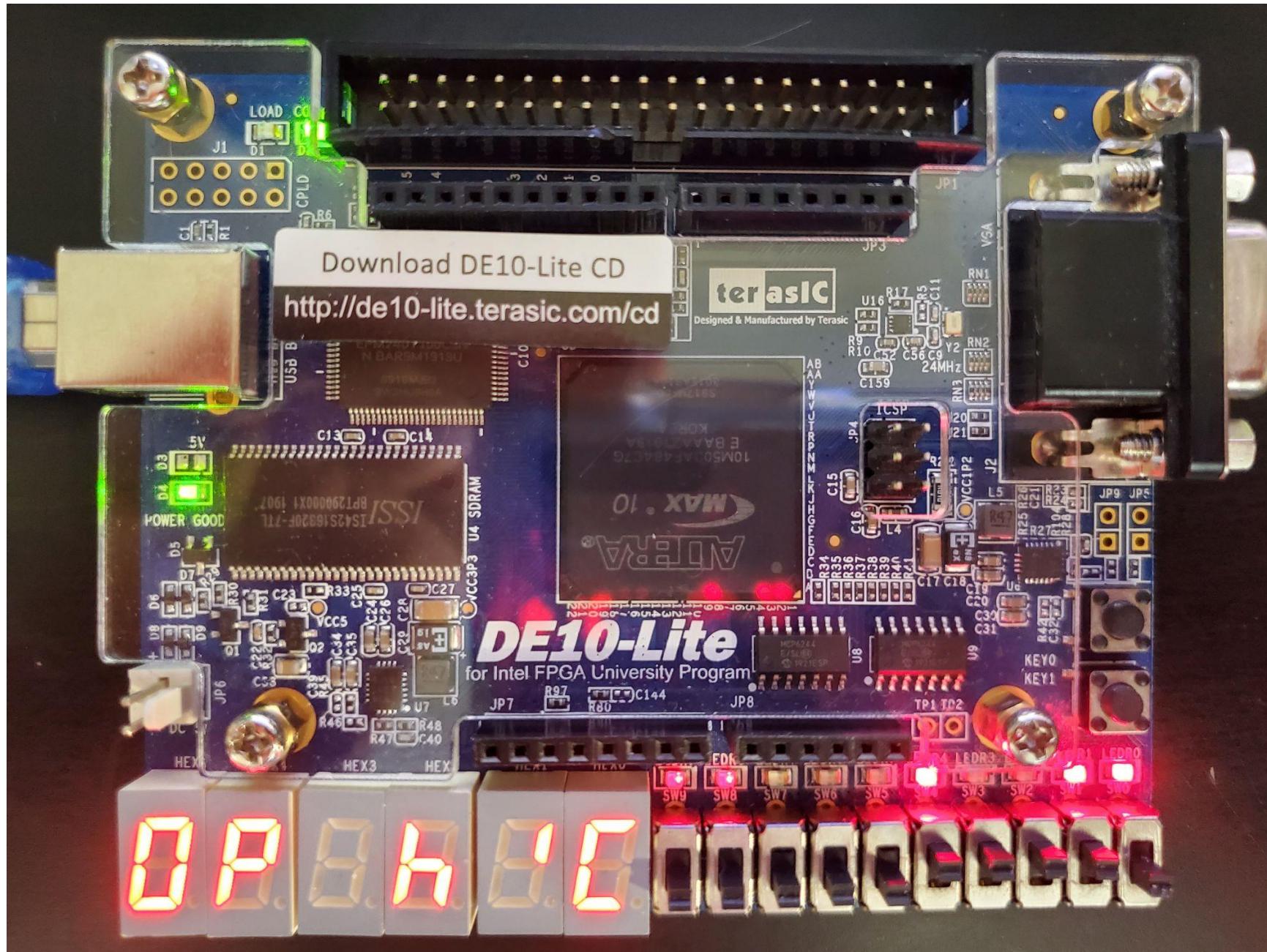
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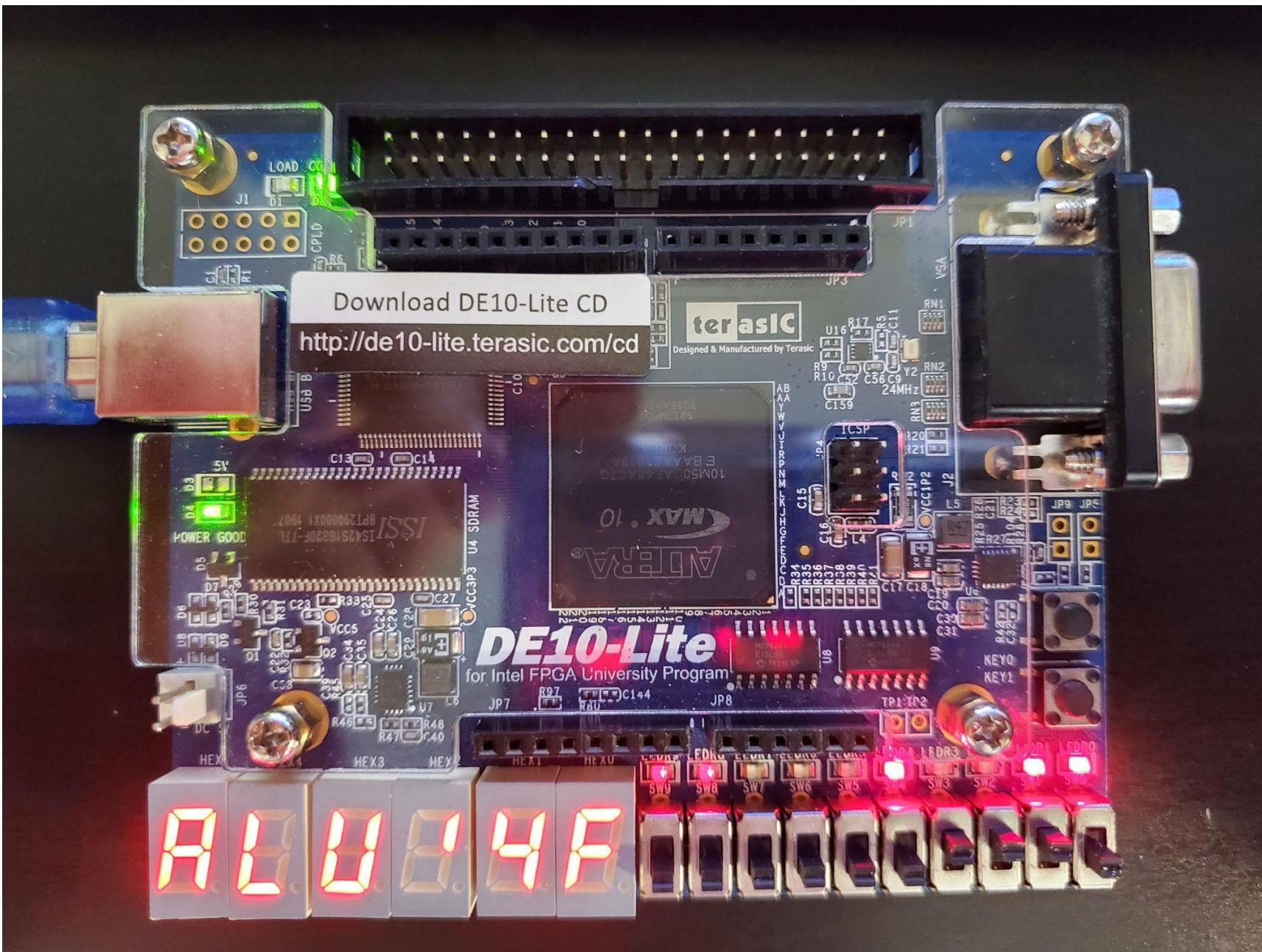
PC: h'13



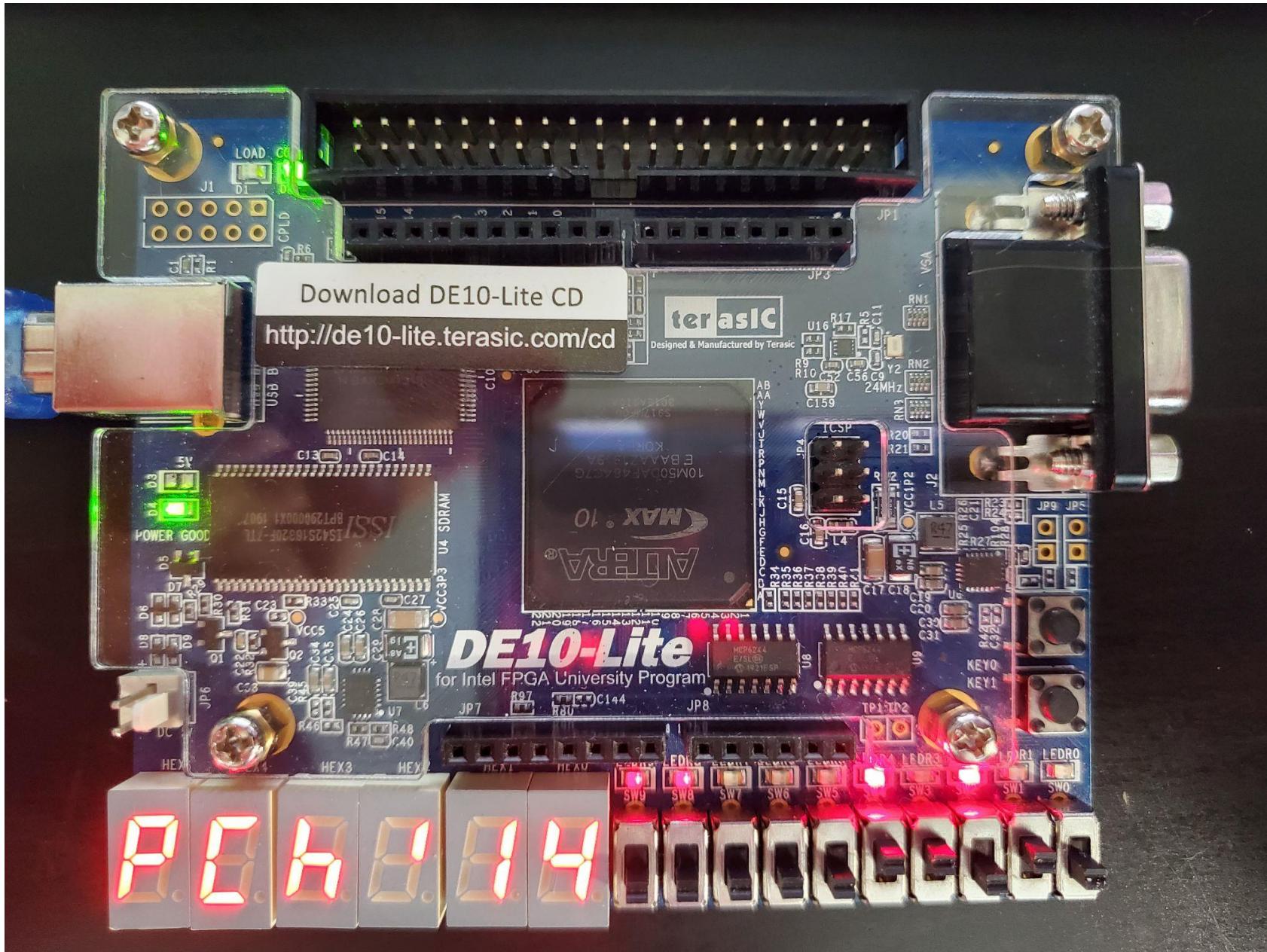
PC: h'13



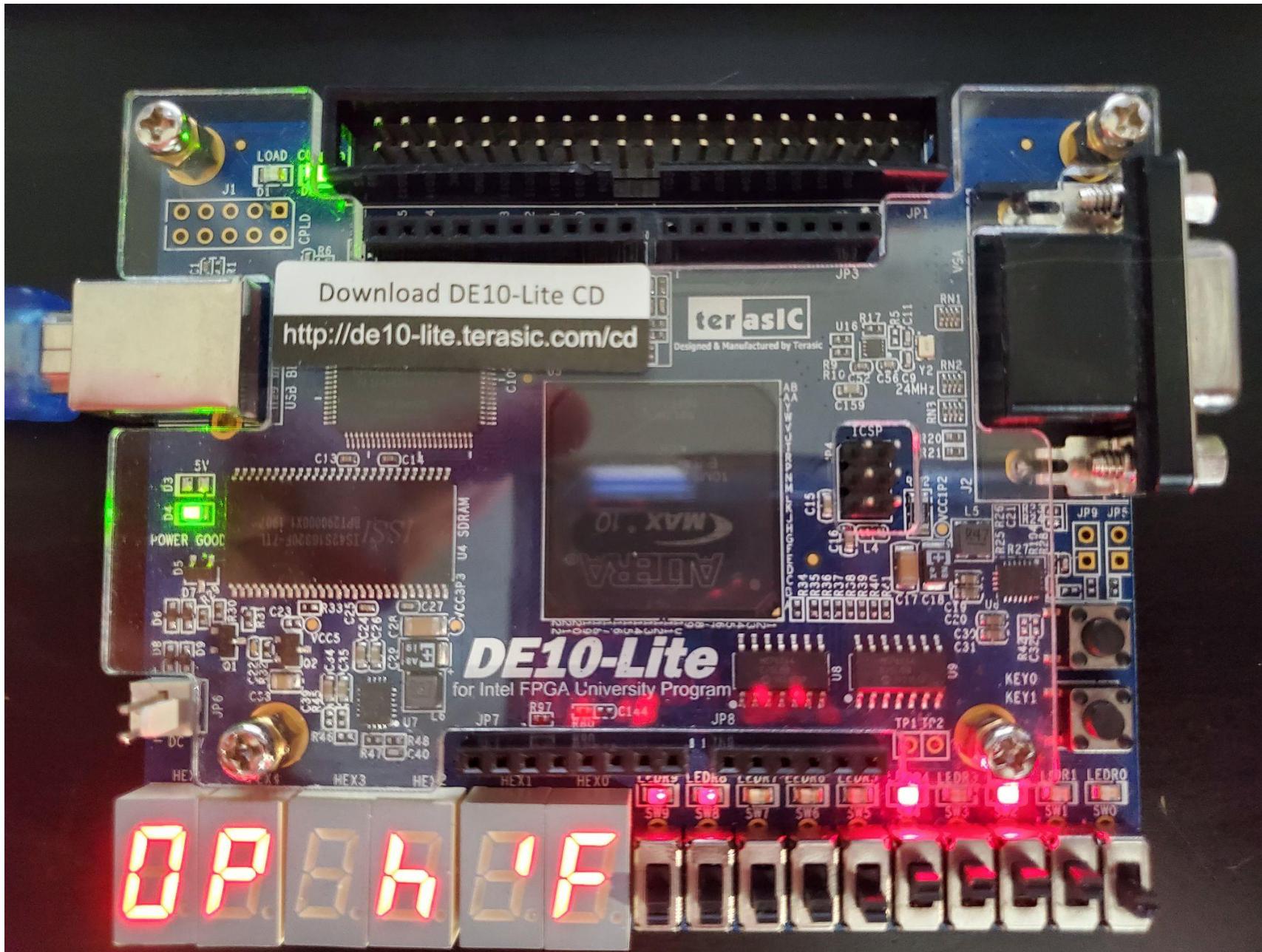
PC: h'13



PC: h'14



PC: h'14



PC: h'14

