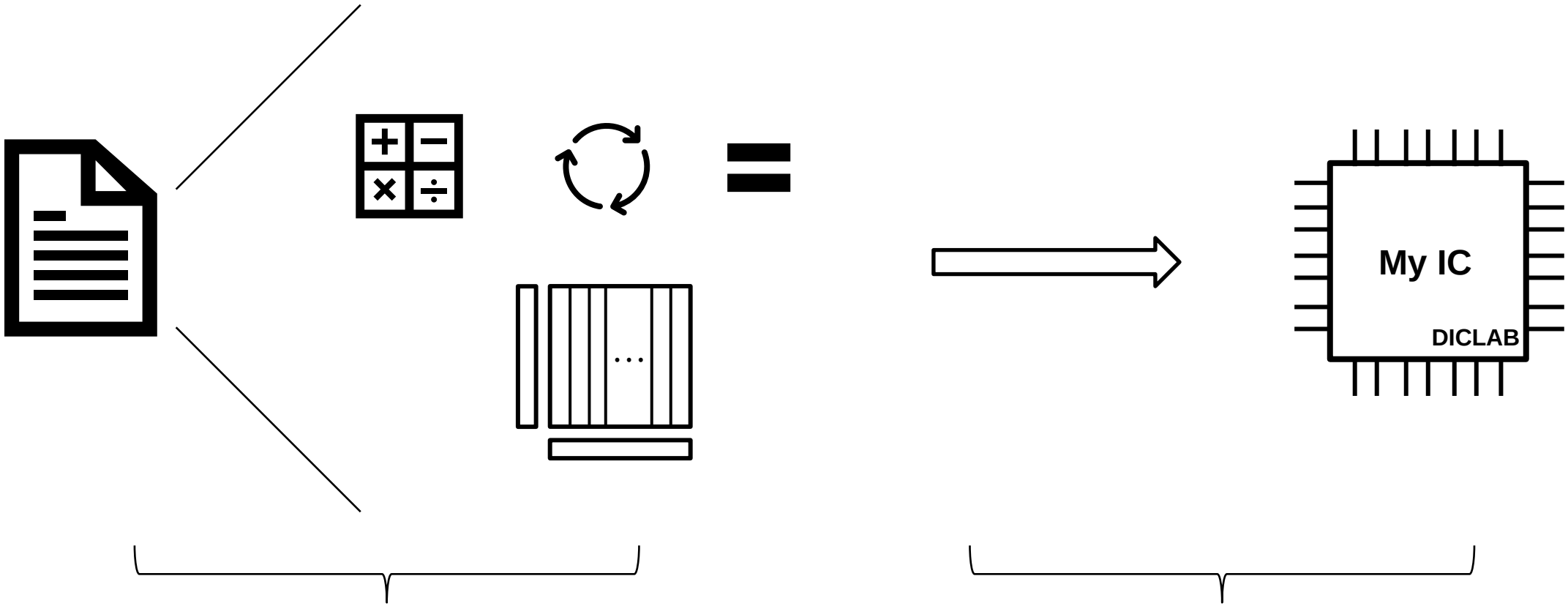
LAB - 05

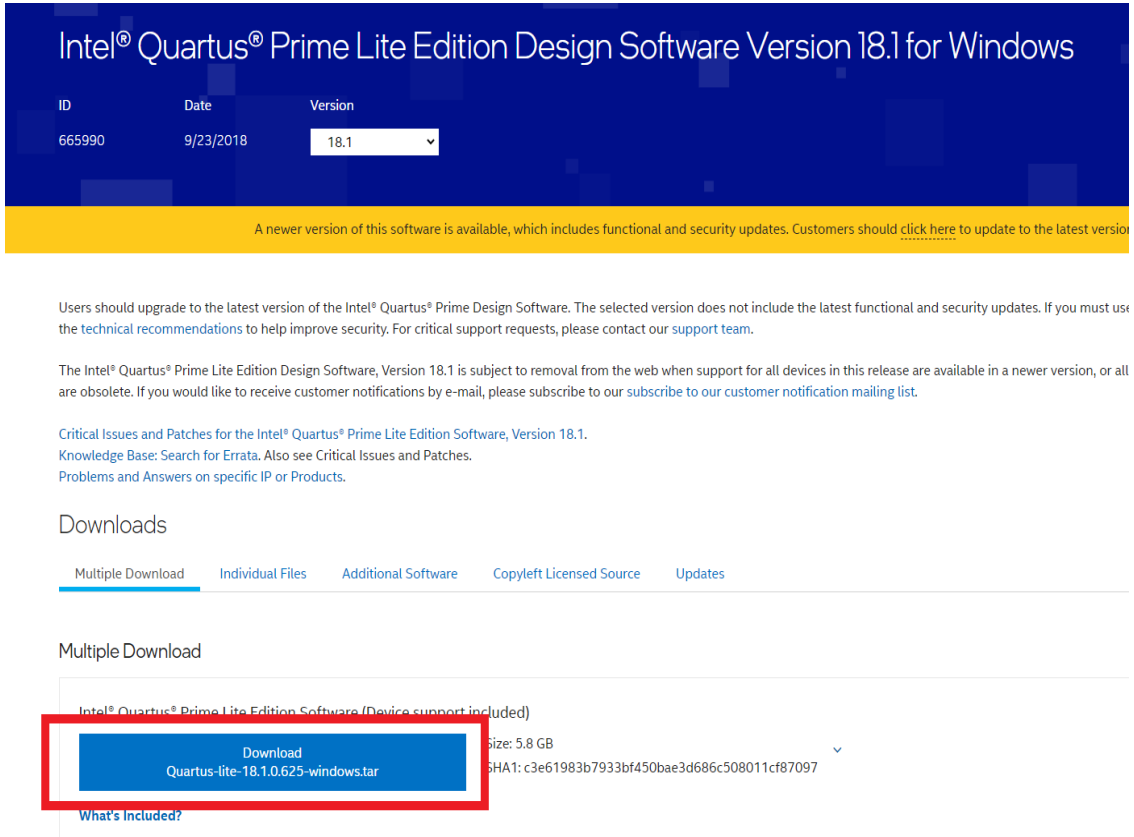
陳培殷老師
國立成功大學　資訊工程系

Introduction



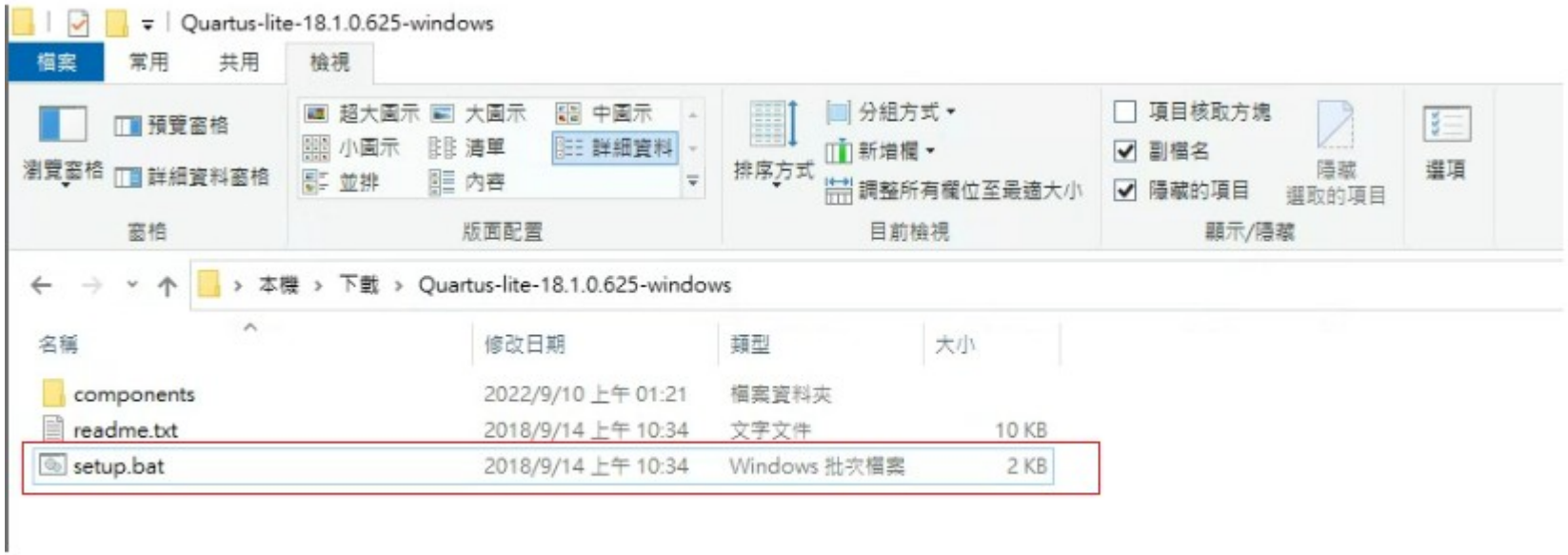
Install Quartus II

- 下載網址 - https://reurl.cc/eOQK7Q



Install Quartus II

- 解壓縮後打開 setup.bat

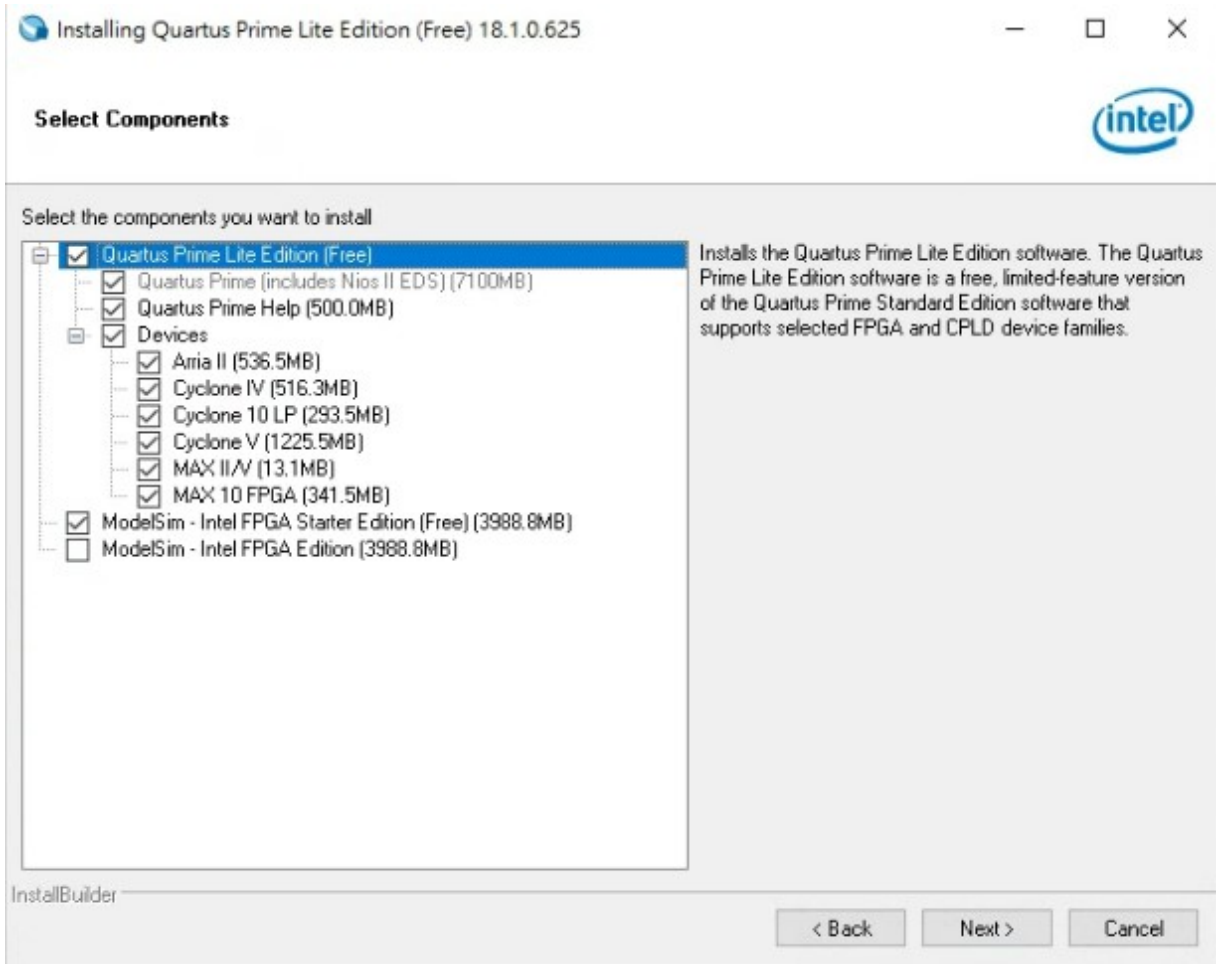


Install Quartus II

- **Next**

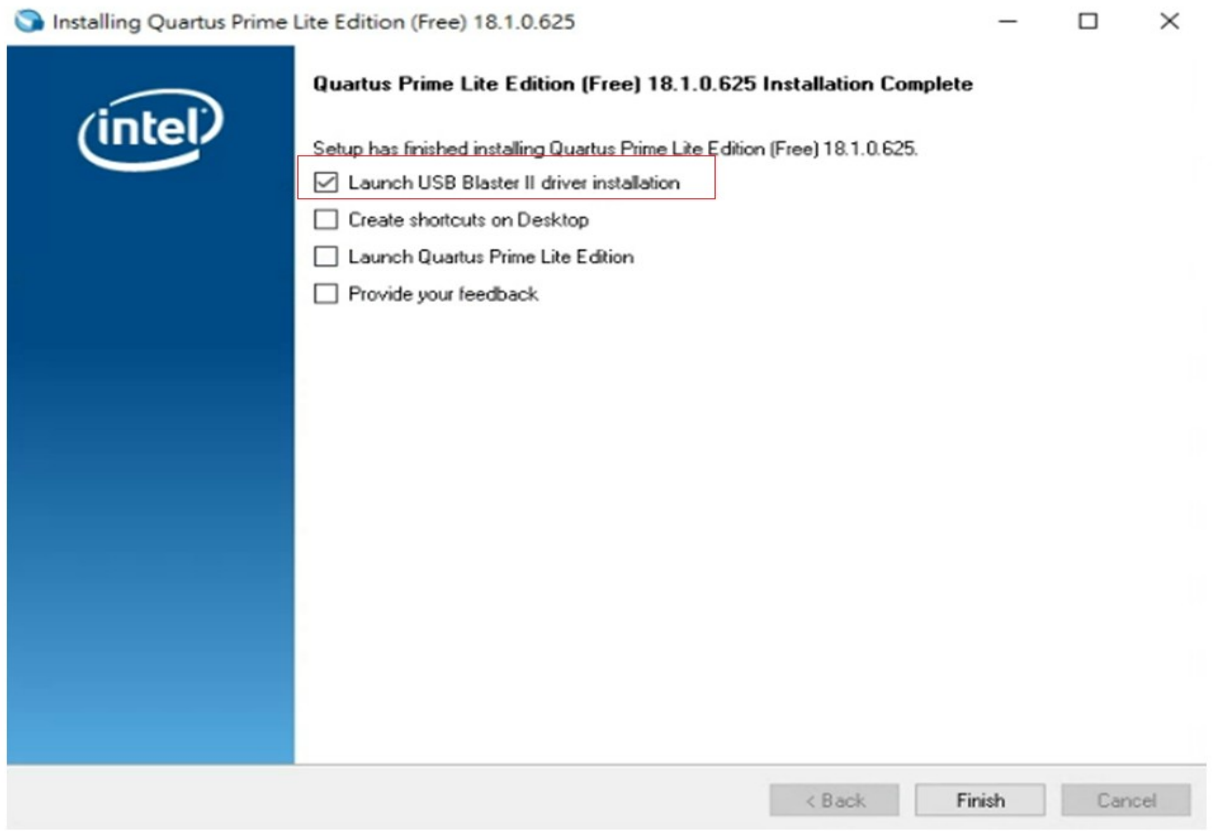
Install Quartus II

- 勾選選項



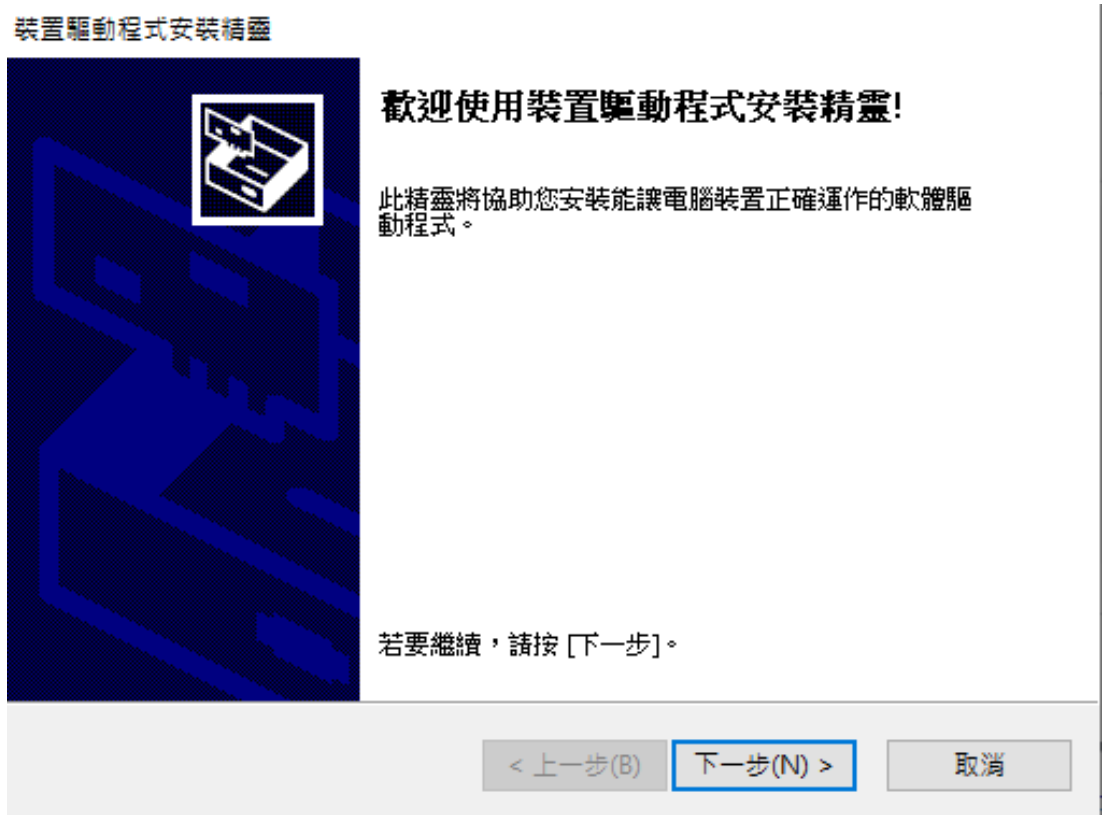
Install Quartus II

- 完成後勾選 Launch USB Blaster II driver installation



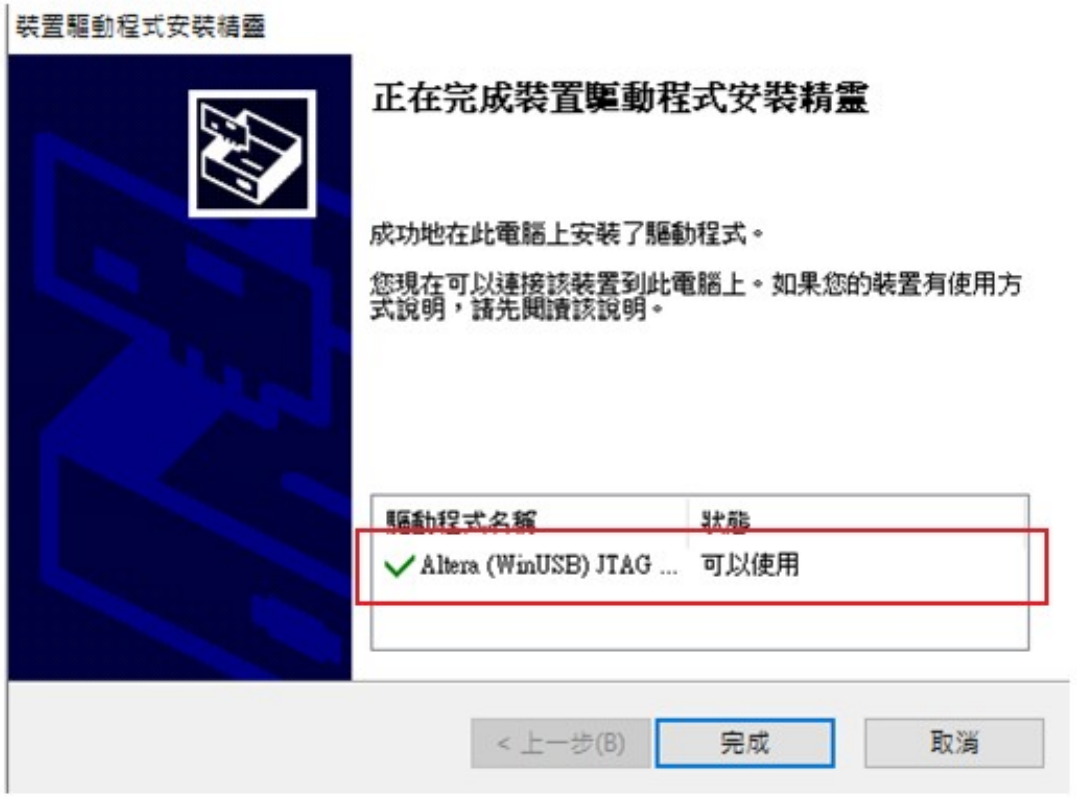
Install Quartus II

- 跳出裝置驅動程式安裝精靈後一直按下一步



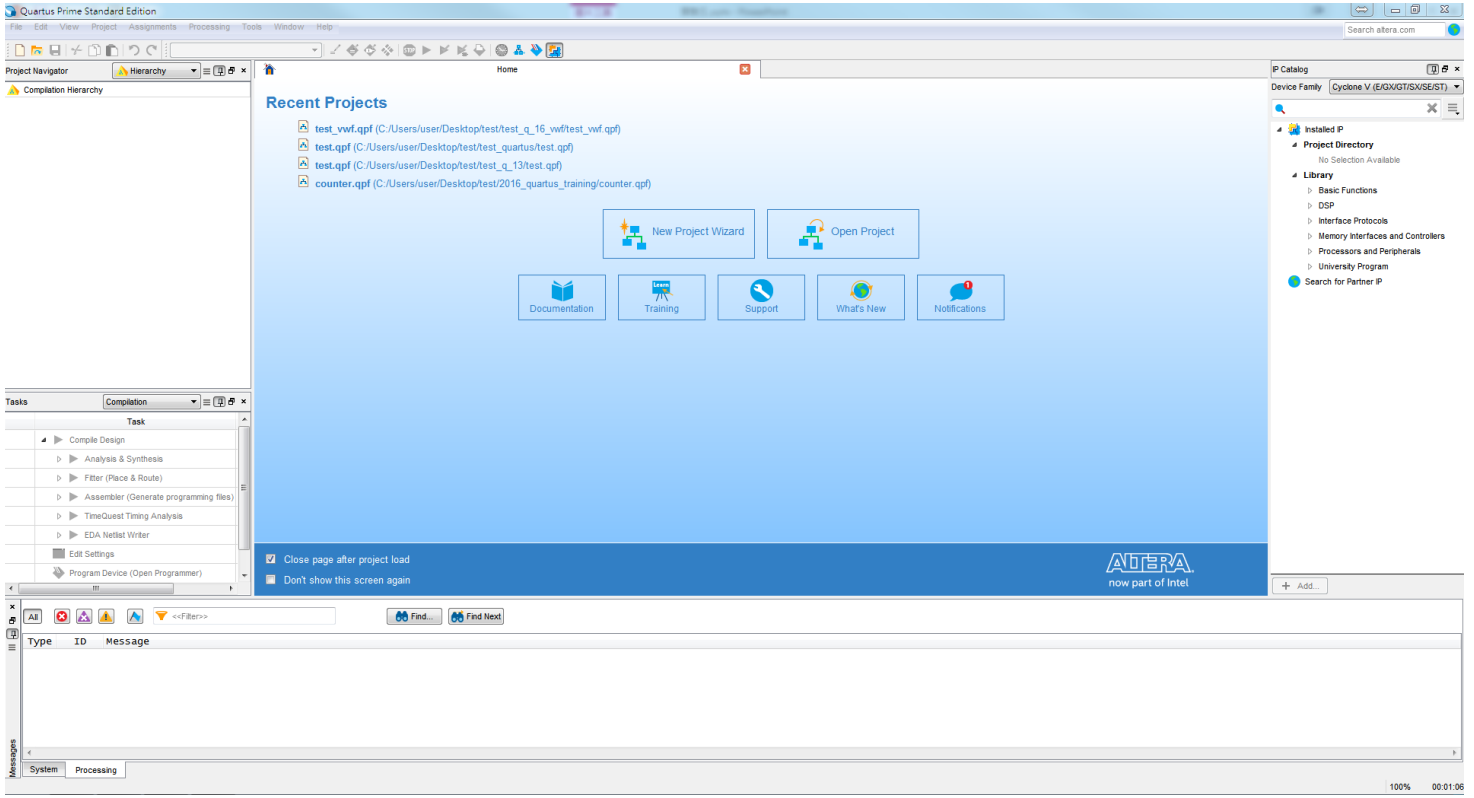
Install Quartus II

- 出現 “可以使用” 就完成安裝了



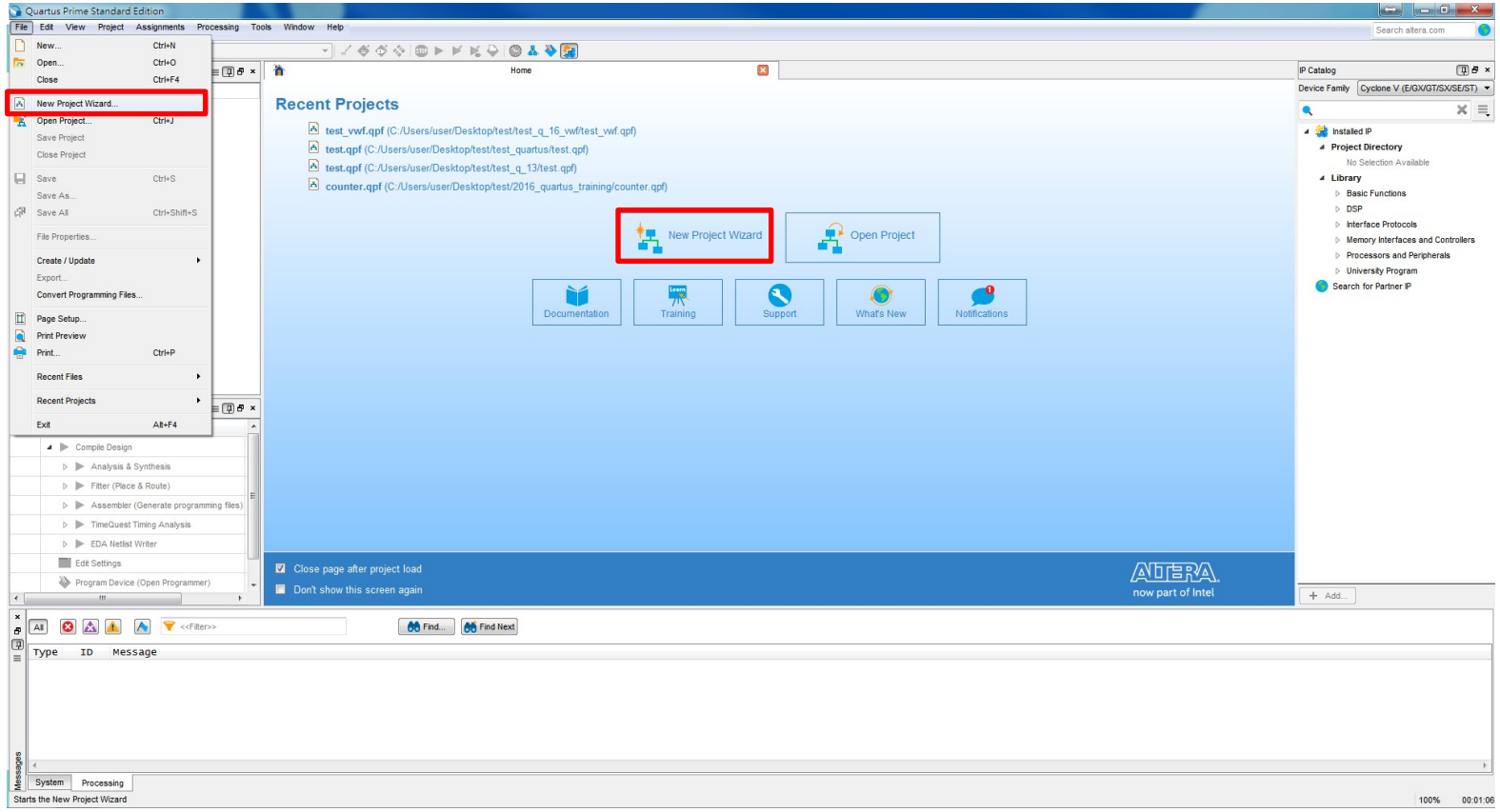
Quartus II Tutorial (1/19)

- **Getting Started –**
  - **Start the Quartus II software**



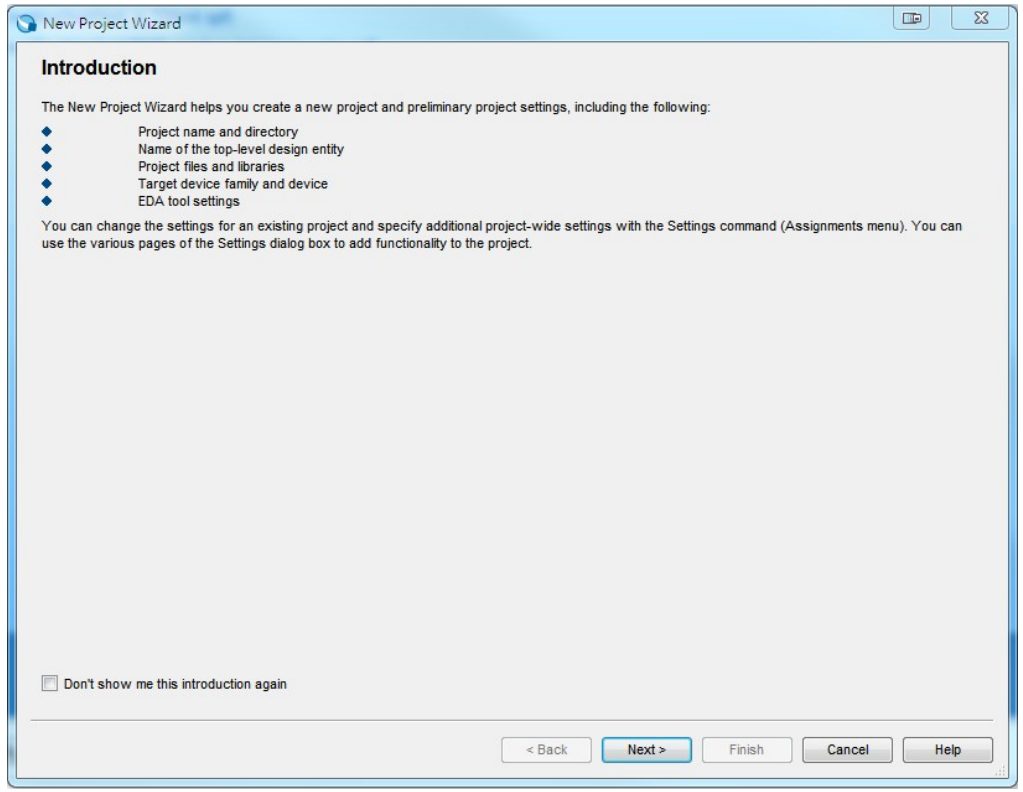
Quartus II Tutorial (2/19)

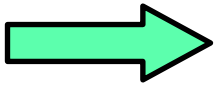
- **Create a New Project –**
  - **Open New Project Wizard (File → New Project Wizard…)**

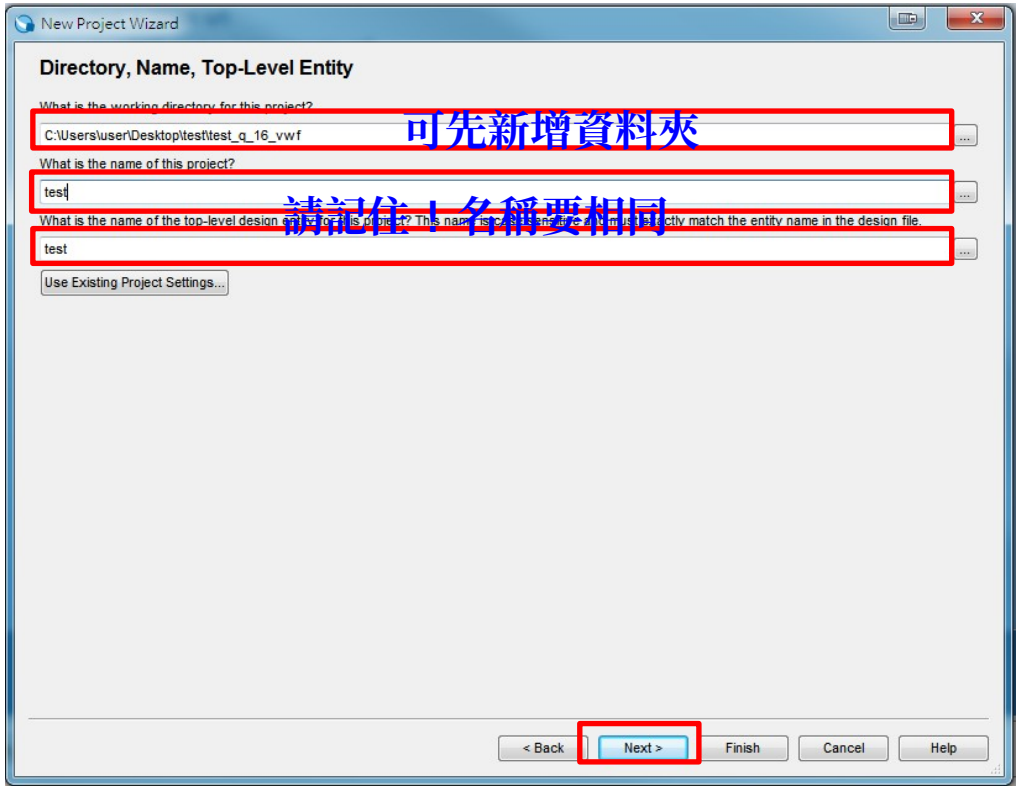


Quartus II Tutorial (3/19)

- **Specify the working directory and the name of the project**

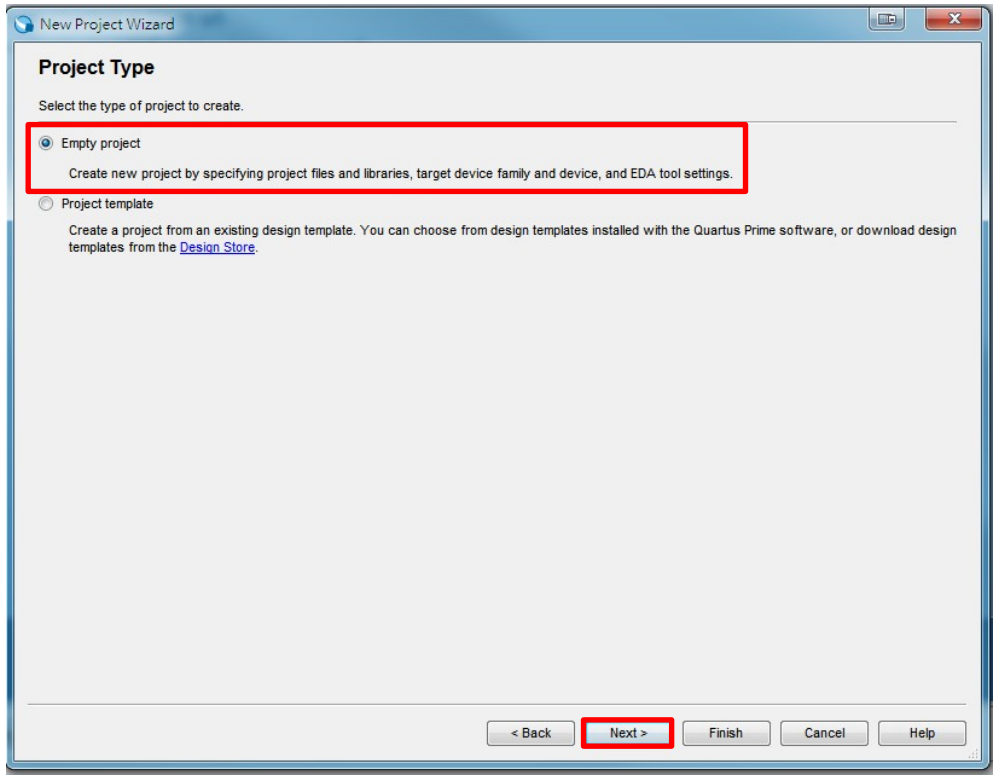


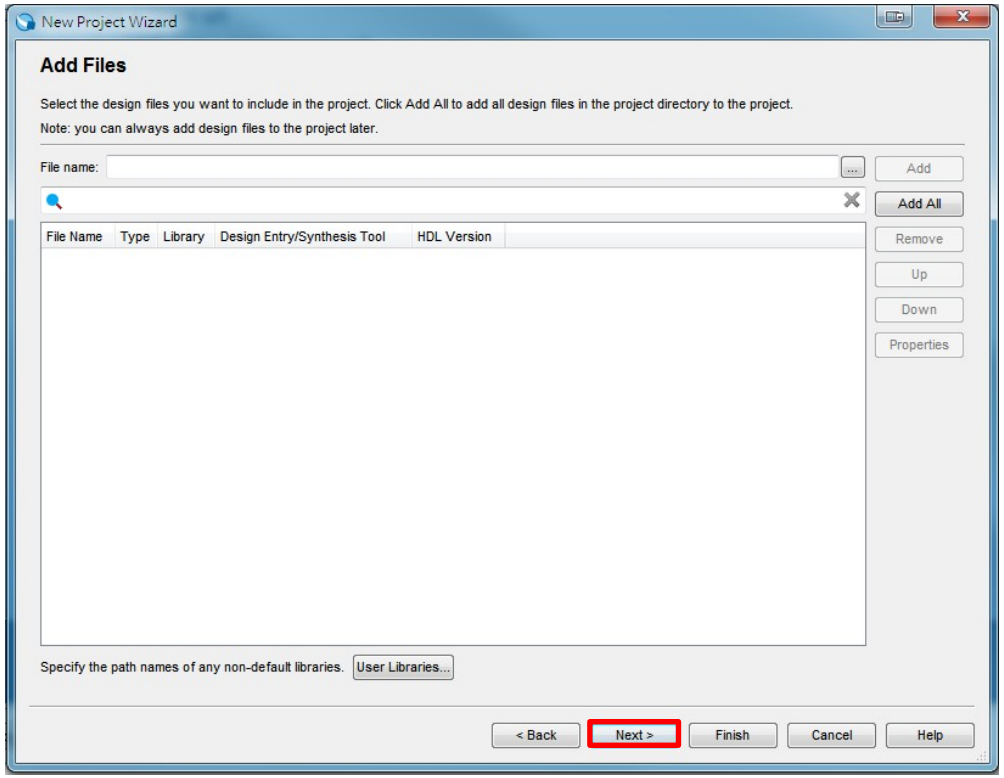




Quartus II Tutorial (4/19)

- Select “Empty project”. Then, click “Next”.
- Select design files. Or click “Next” to skip this step.



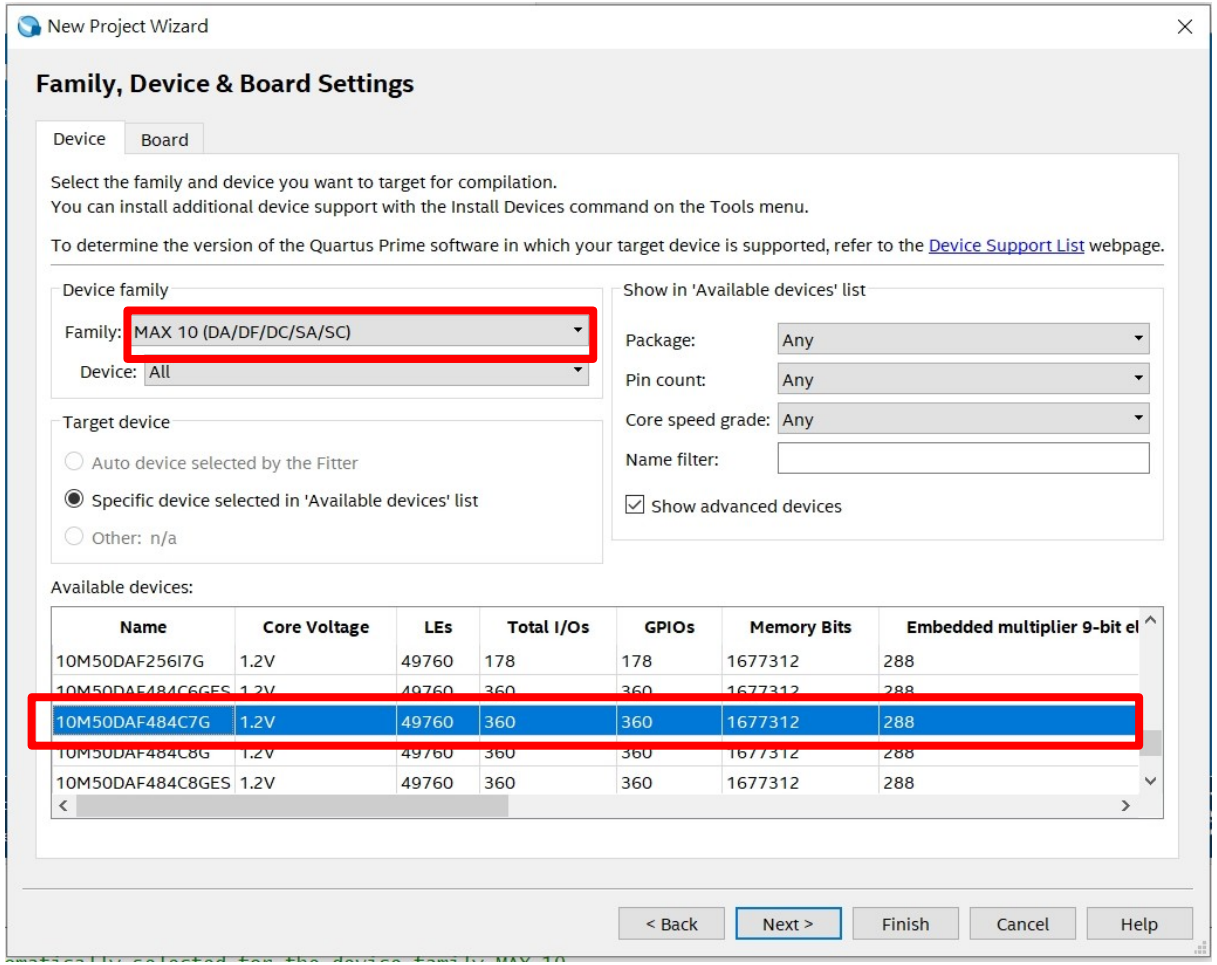


Quartus II Tutorial (5/19)

- Specify device settings - (DE10-Lite Device family are used). Click “Next.”

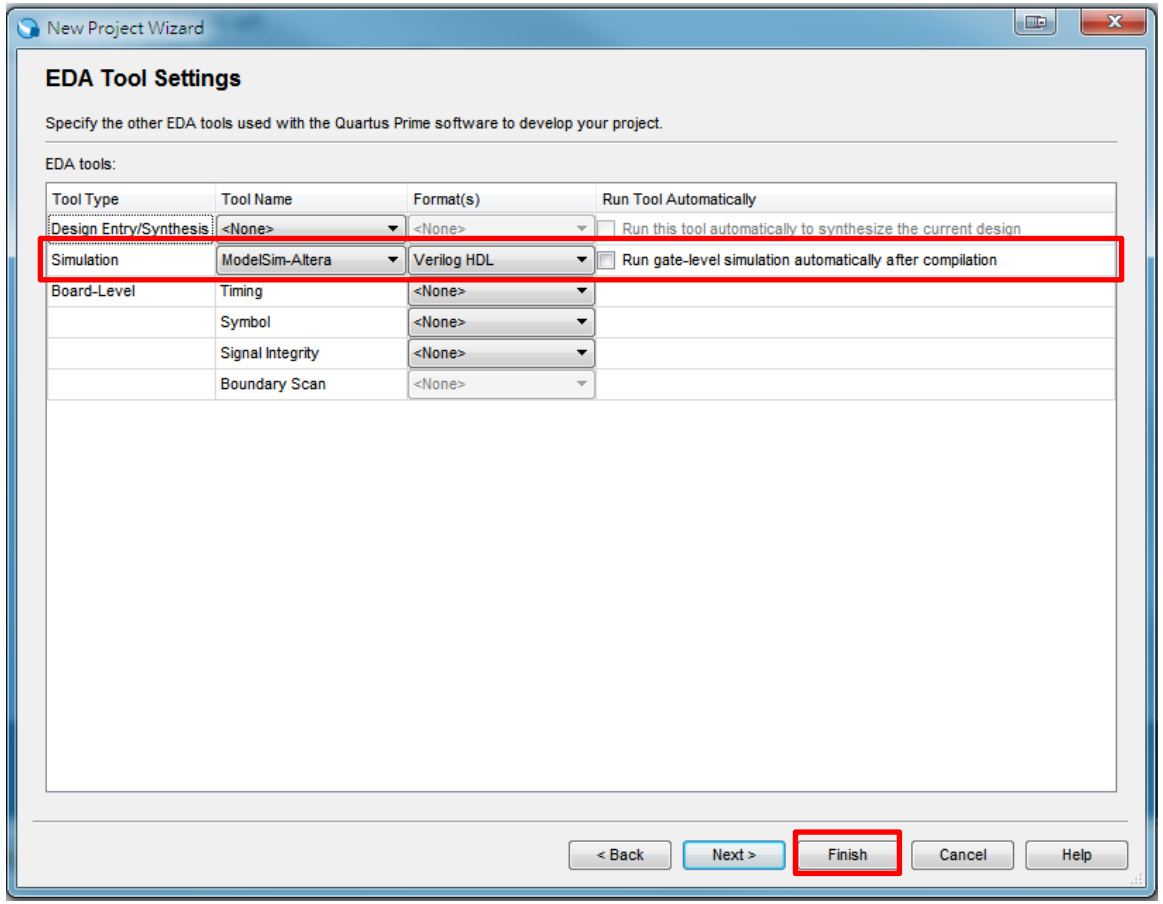
MAX 10(DA/DF/DC/SA/SC)

10M50DAF484C7G



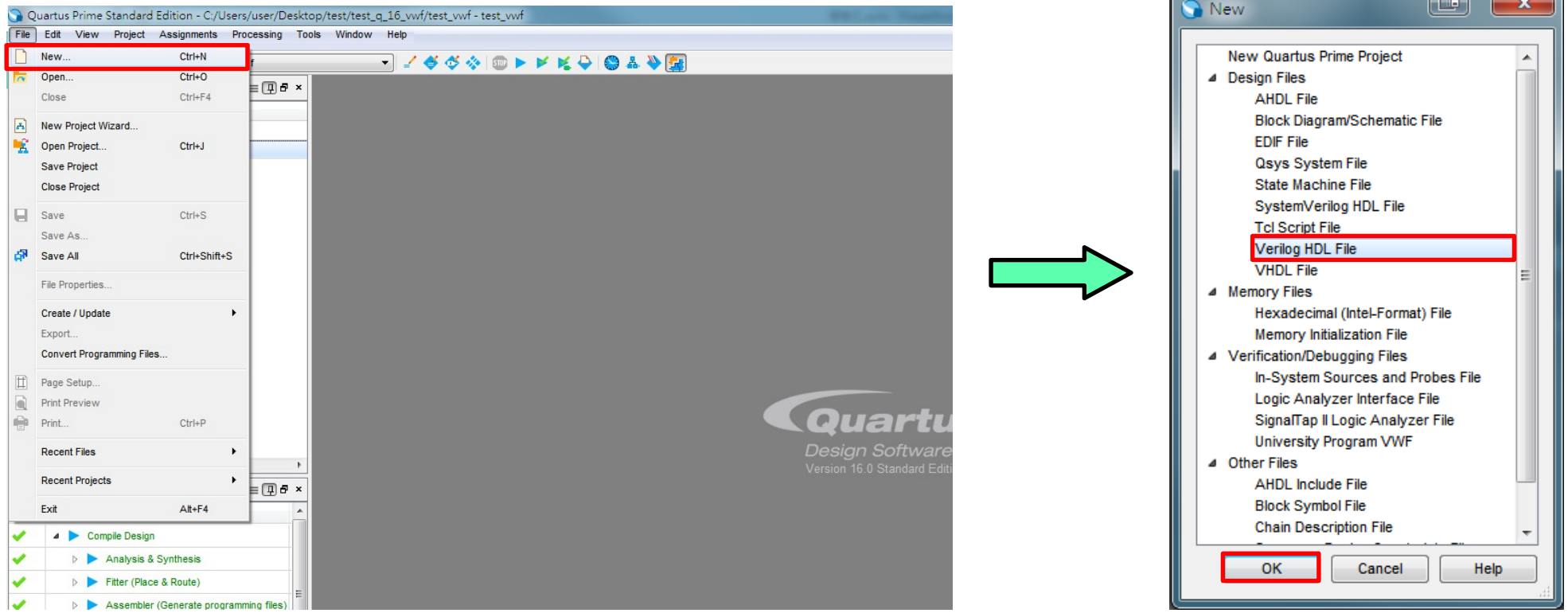
Quartus II Tutorial (6/19)

- **Specify EDA Tool – (Modelsim-Altera is selected for simulation). Click “Finish.”**



Quartus II Tutorial (7/19)

- **Edit a new file by opening a Verilog HDL file**
  - **(File → New → Verilog HDL File → OK)**

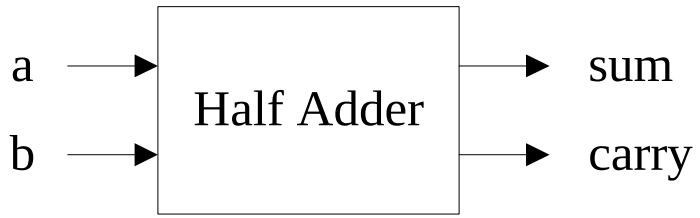


Quartus II Tutorial (8/19)

- **Write Verilog code**

Top module name 一定要跟 Project name 相同 !!

輸入 (input)		輸出 (output)	
被加數 (a)	加數 (b)	和 (sum)	進位 (carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



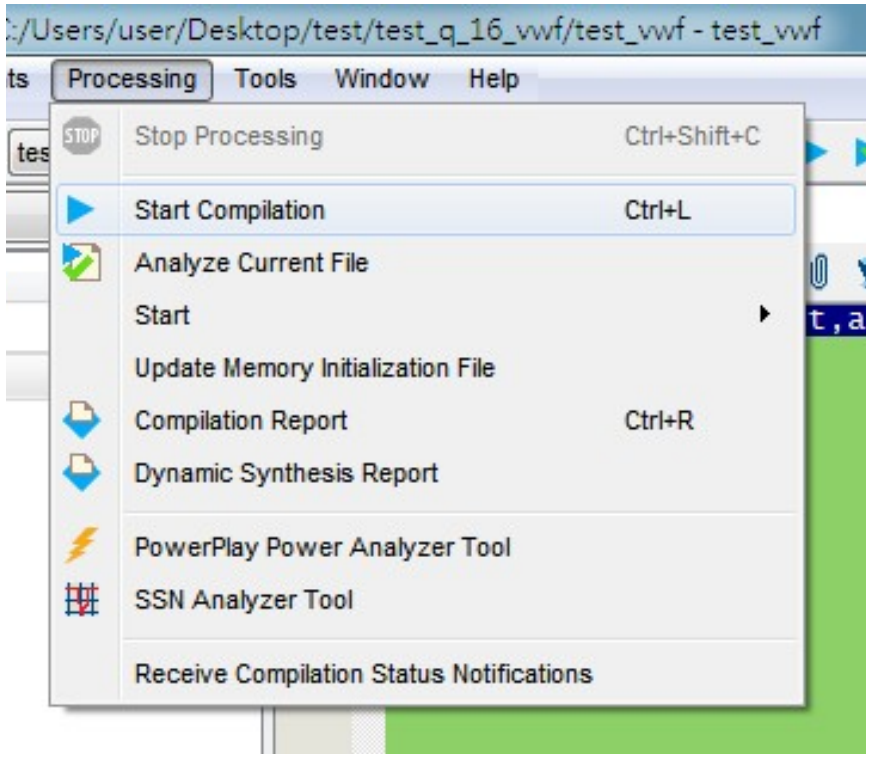

```
module test (
  input a,
  input b,
  output sum,
  output carry
);

/* Write your code here. */

endmodule
```

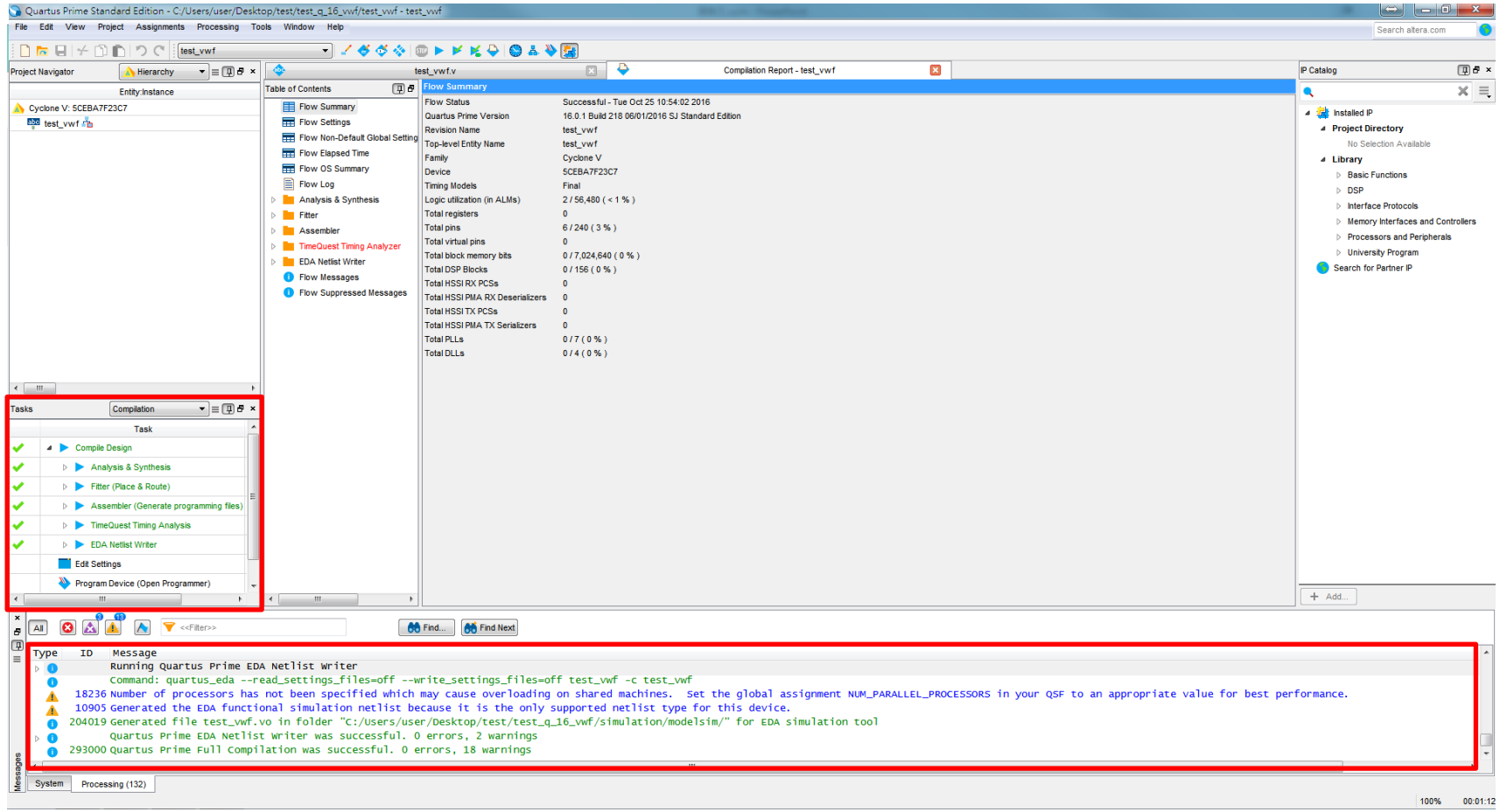
Quartus II Tutorial (9/19)

- **Compiling the Designed Circuit （synthesis 合成）**
  - **(Processing → Start Compilation)**



Quartus II Tutorial (10/19)

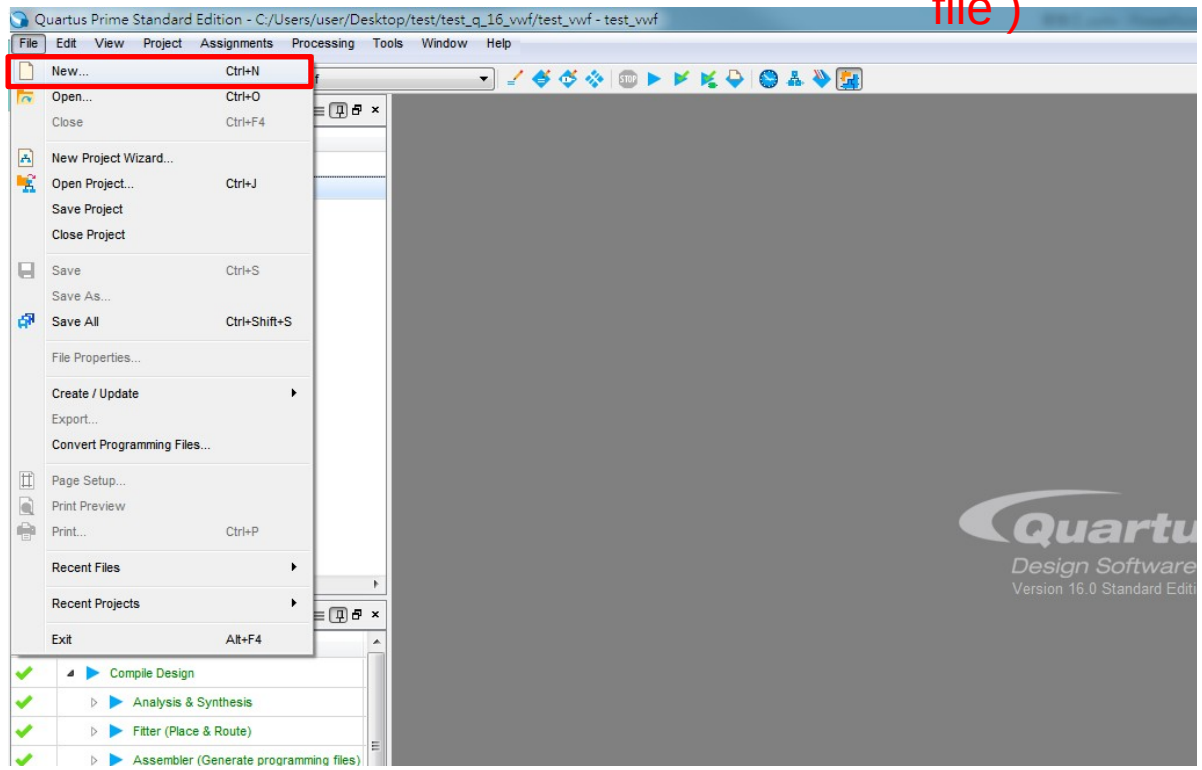
- **Successful compilation**

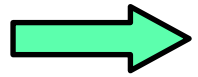


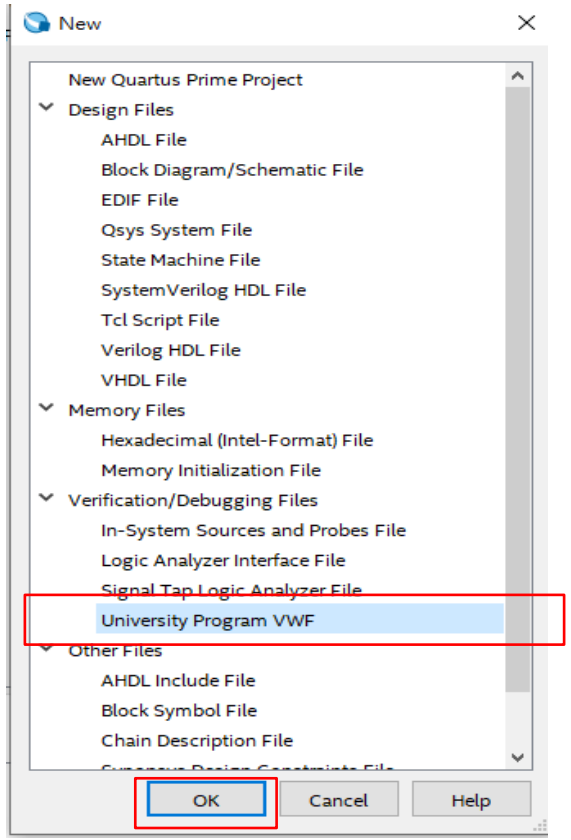
Quartus II Tutorial (11/19)

- **Edit a new file by opening a Verilog HDL file**
  - **(File → New → University Program VWF → OK)**

(vector waveform file)

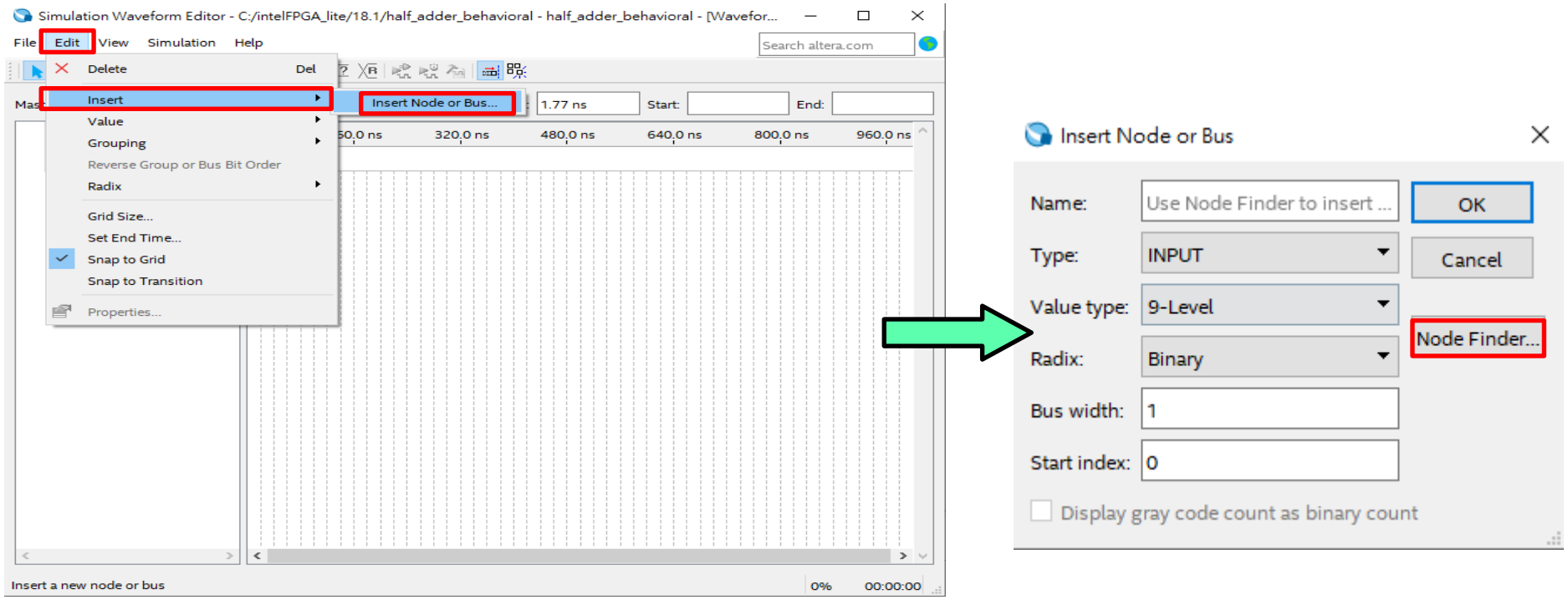






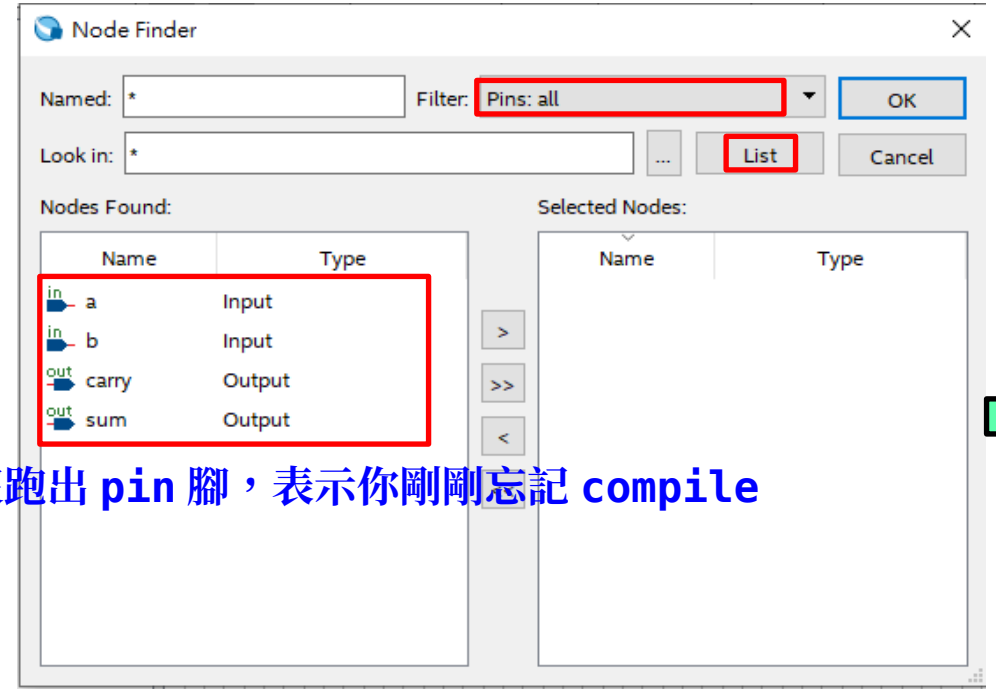
Quartus II Simulation (12/19)

- **Simulating the Designed Circuit**
  - **Use node finder to find all the I/O pins (Edit → Insert → Insert Node or Bus…)**

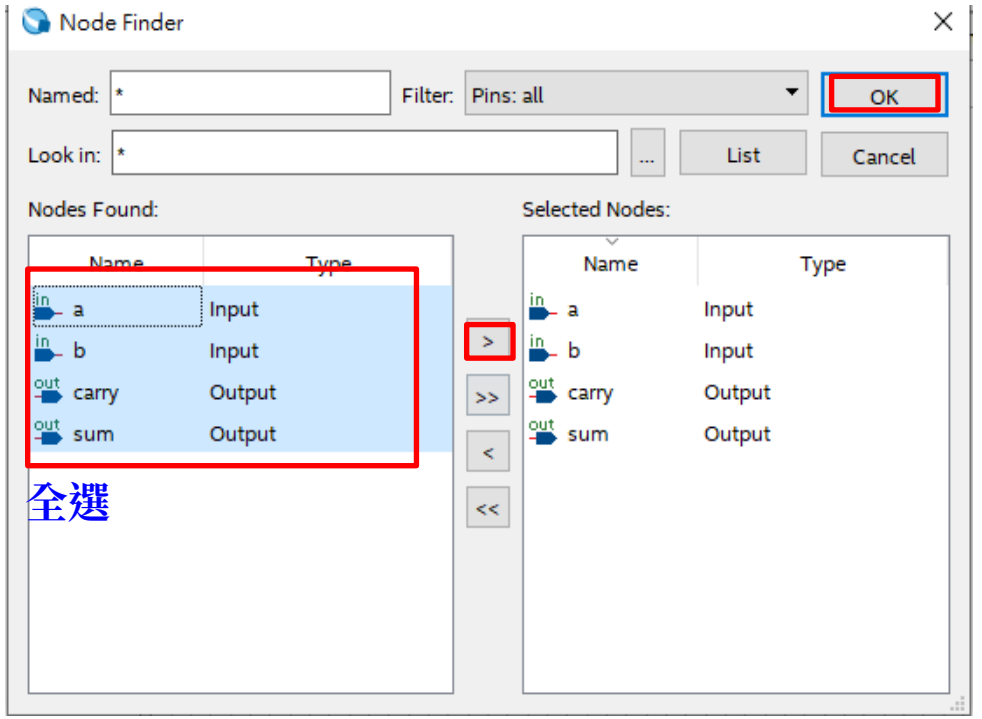


Quartus II Simulation (13/19)

- **Simulating the Designed Circuit**
  - **Selecting nodes to insert into the Waveform Editor**



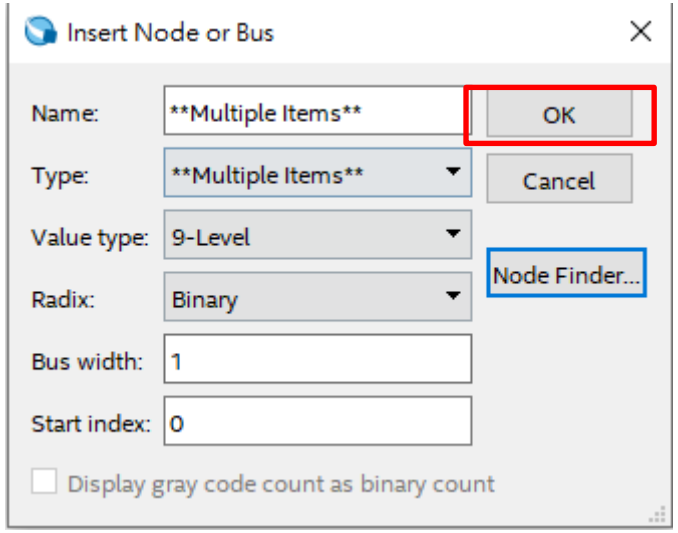
沒跑出 pin 腳，表示你剛剛忘記 compile

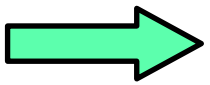


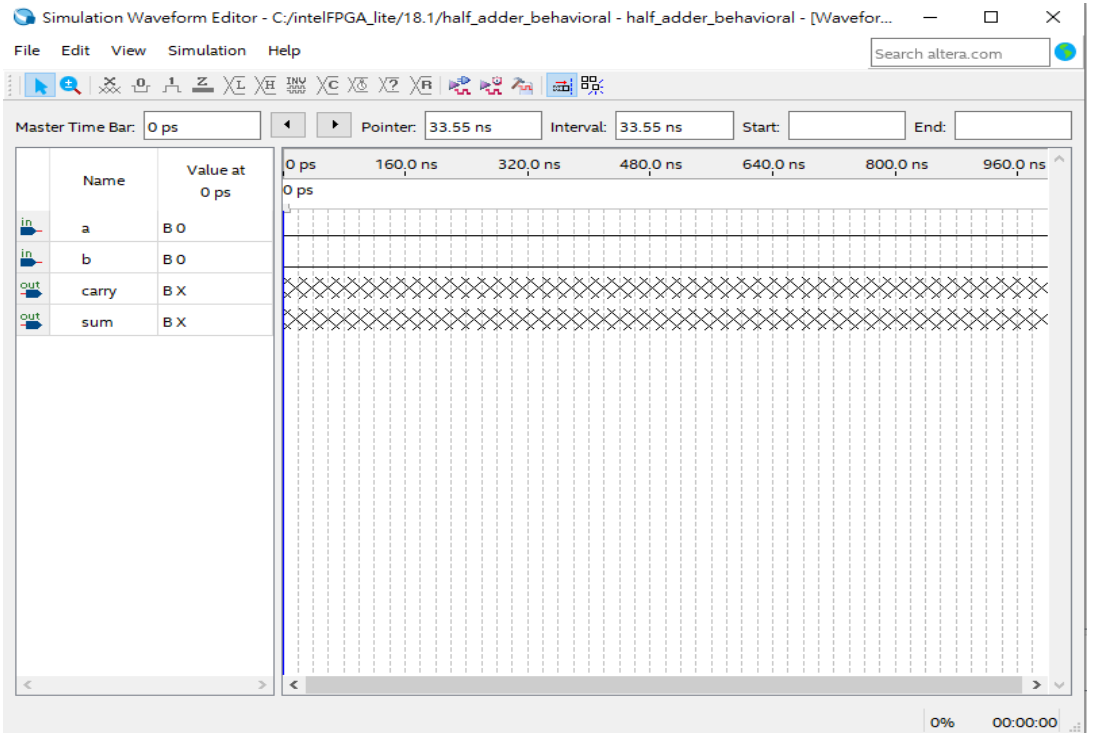
全選

Quartus II Simulation (14/19)

- **Simulating the Designed Circuit**
  - **Selecting nodes to insert into the Waveform Editor**

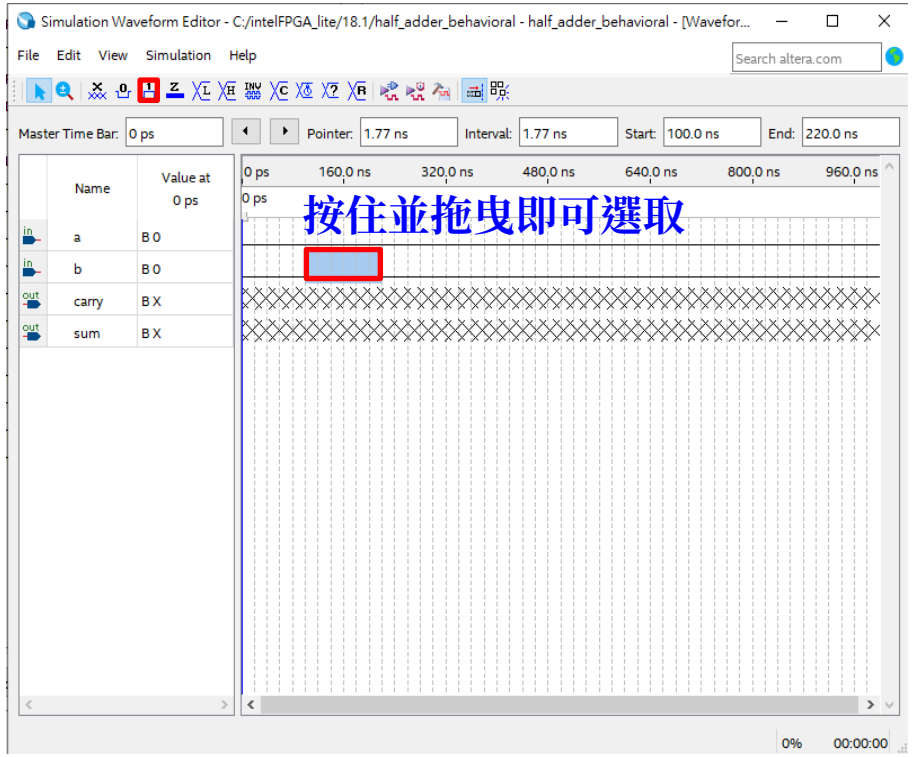


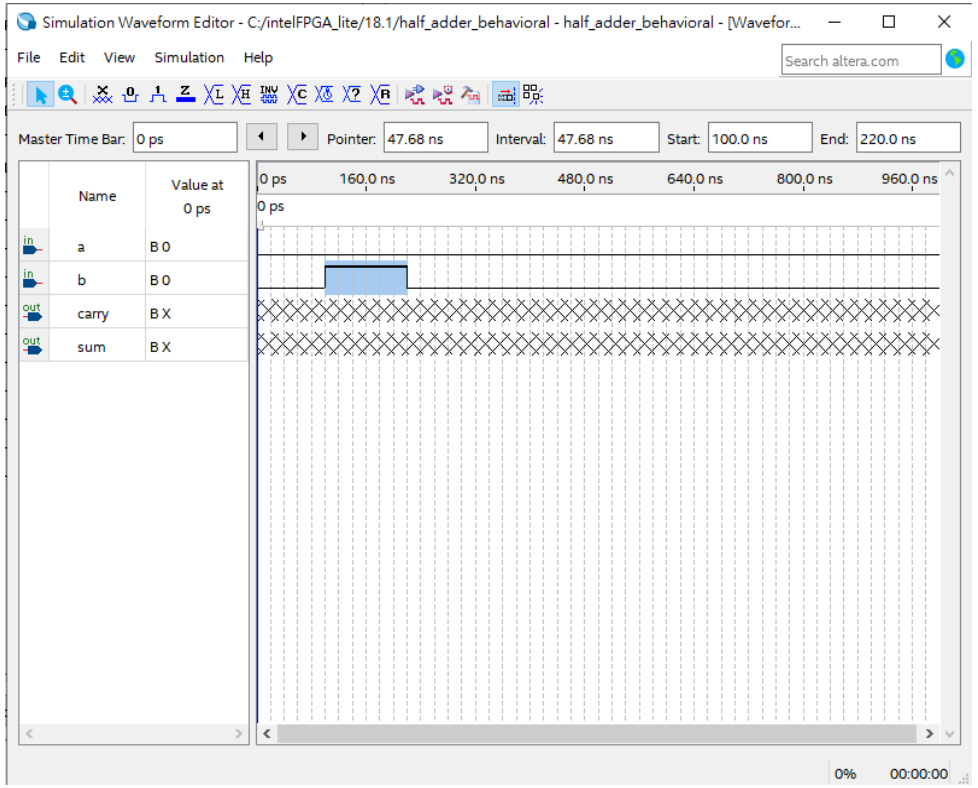




Quartus II Simulation (15/19)

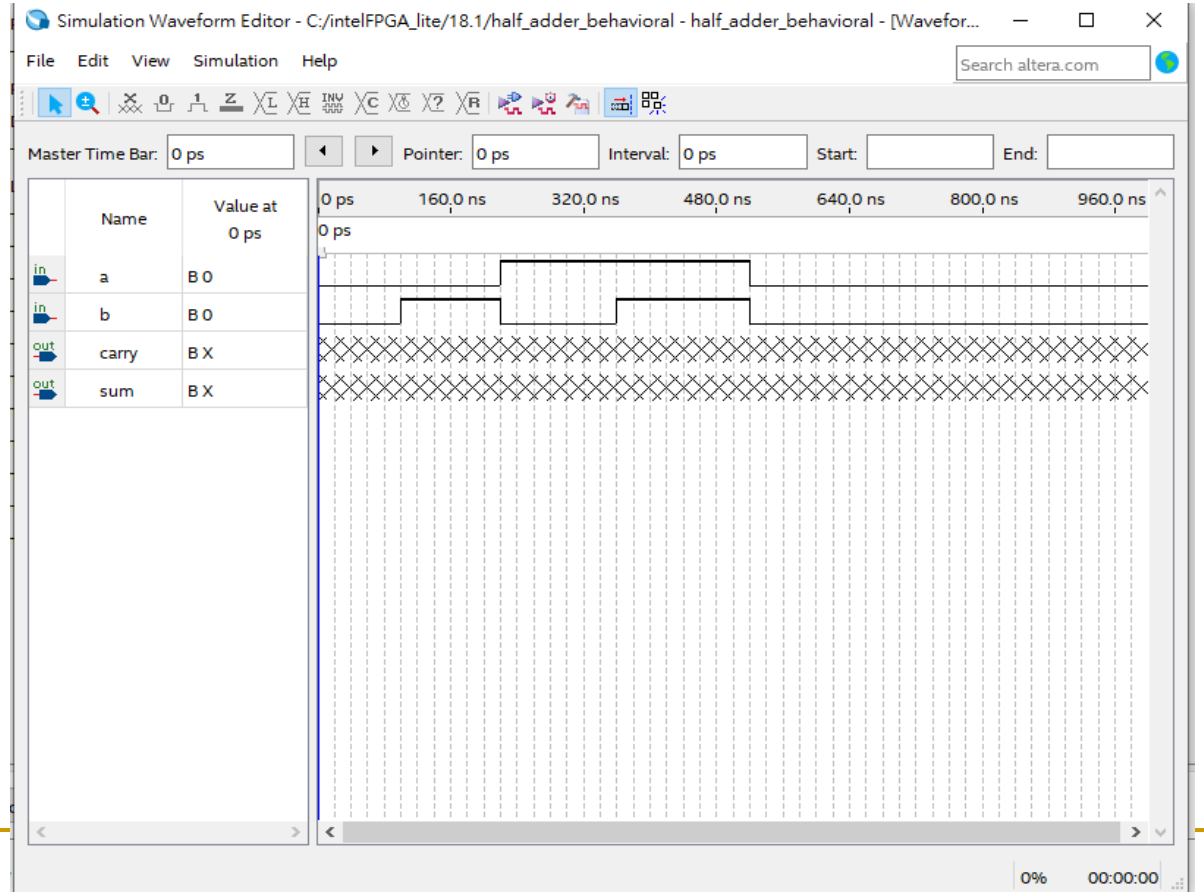
- **Simulating the Designed Circuit**
  - **Select and edit waveform**





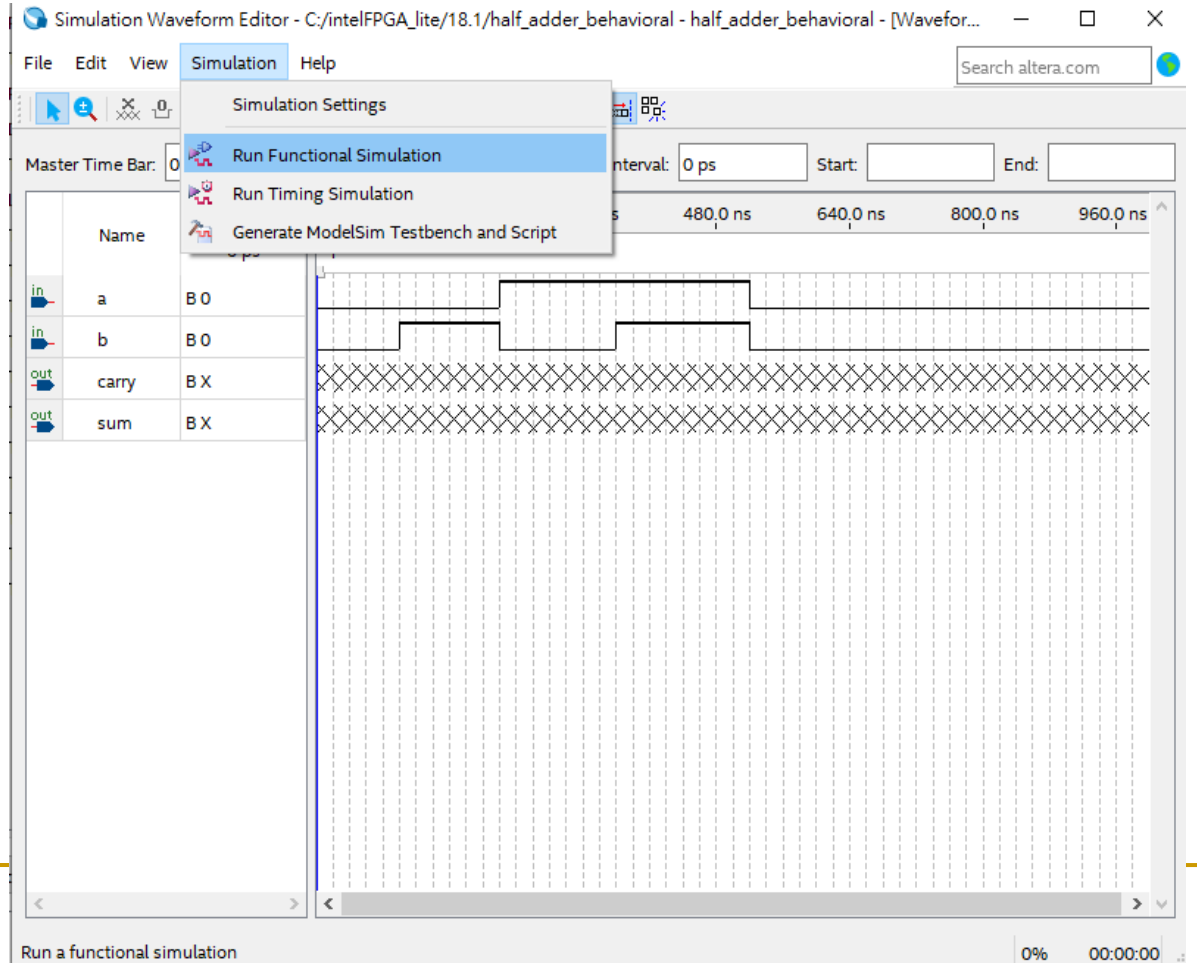
Quartus II Simulation (16/19)

- **Simulating the Designed Circuit**
  - **Setting of test values**



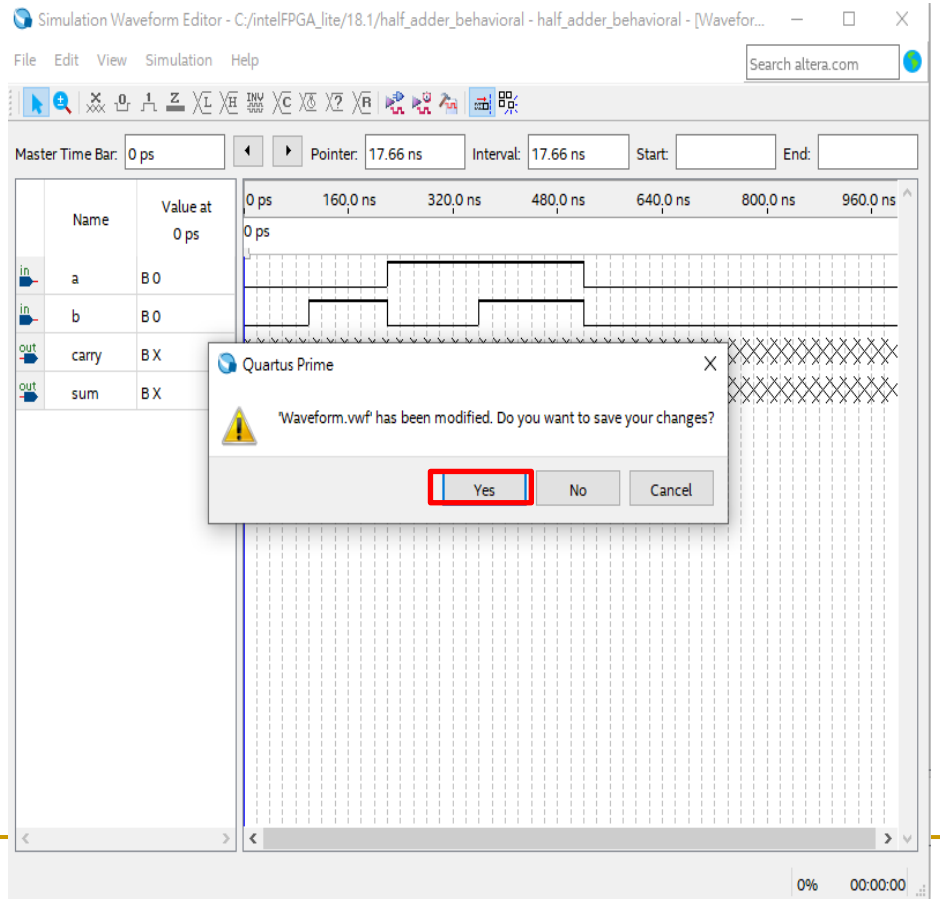
Quartus II Simulation (17/19)

- **Simulating the Designed Circuit**
  - **Run Functional Simulation**



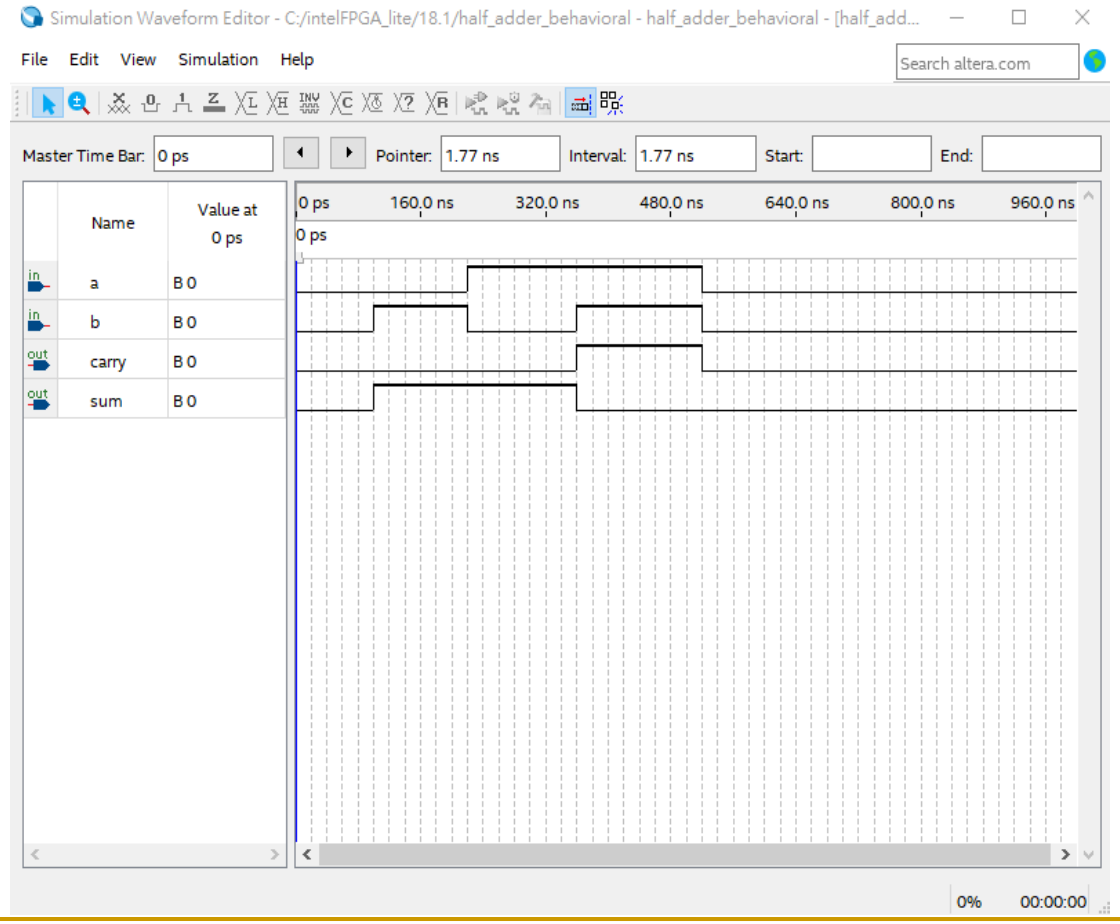
Quartus II Simulation (18/19)

- **Simulating the Designed Circuit**
  - **Save .vwf**



Quartus II Simulation (19/19)

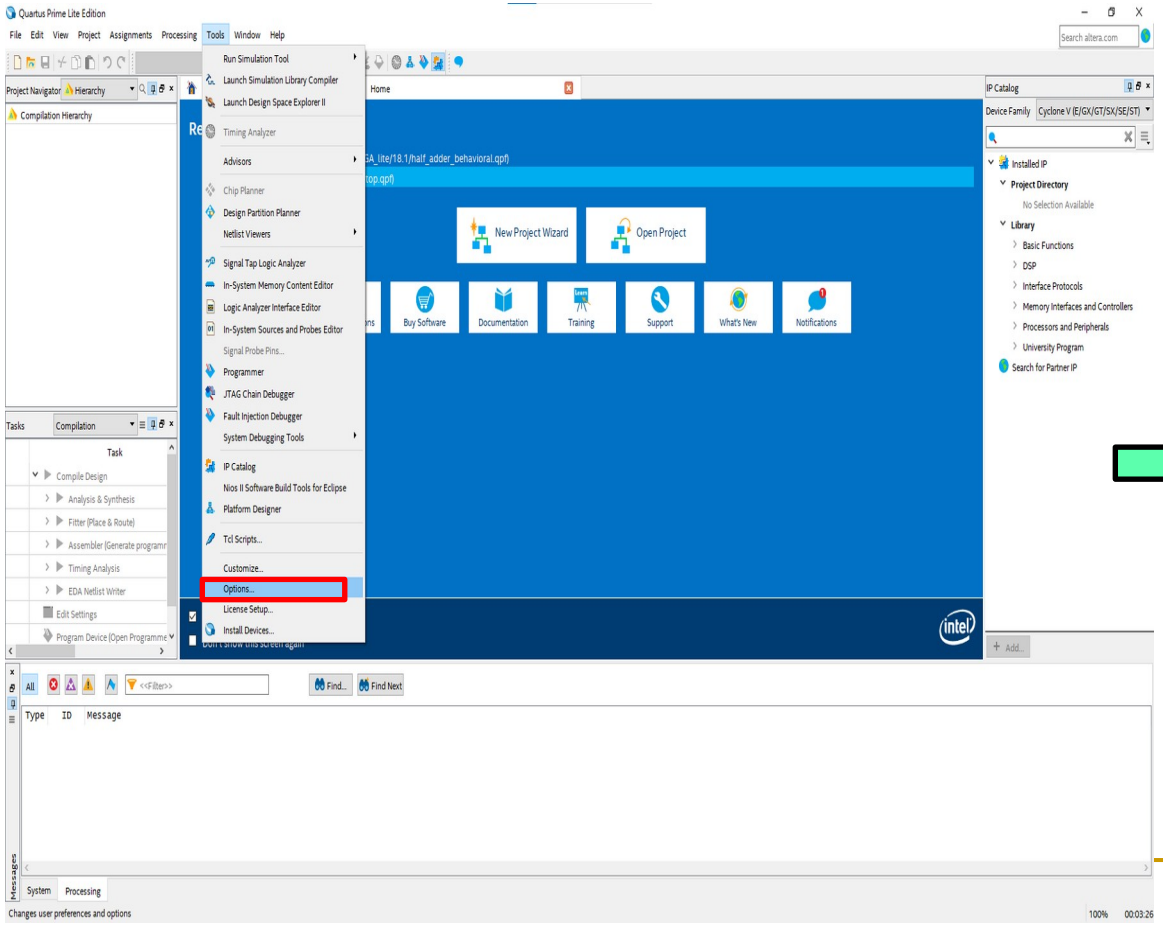
- **The result of functional simulation**

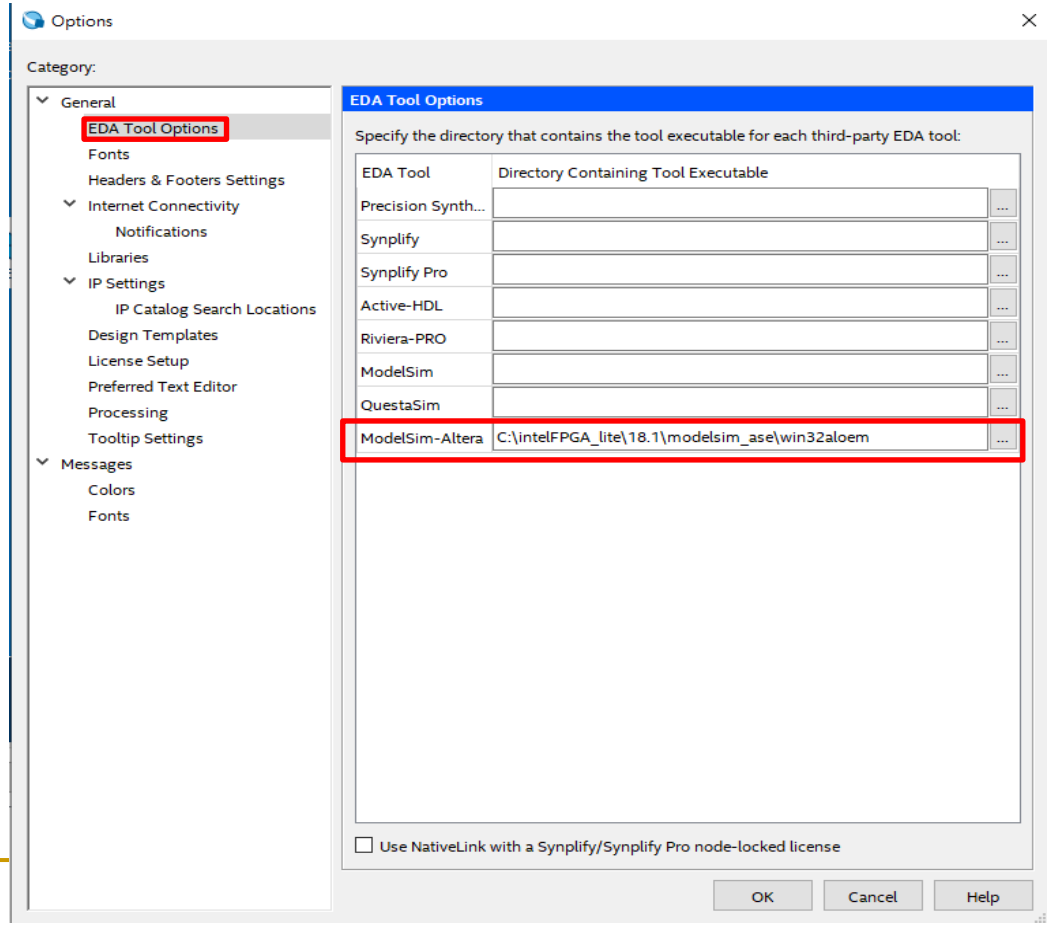


輸入 (input)		輸出 (output)	
被加數 (a)	加數 (b)	和 (sum)	進位 (carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Quartus II Simulation Notice

- 如果 simulation 時出現 error ，修改 ModelSim-Altera 路徑
  - 個人電腦 : (Tools → Options → EDA Tool Options → ModelSim-Altera → C:\intelFPGA_lite\18.1\modelsim_ase\win32aloem)
  - 實驗室電腦 : (Tools → Options → EDA Tool Options → ModelSim-Altera → C:\intelFPGA\16.1\modelsim_ase\win32aloem)





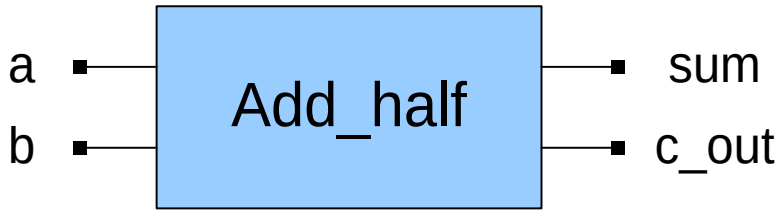
Lab I - Half Adder

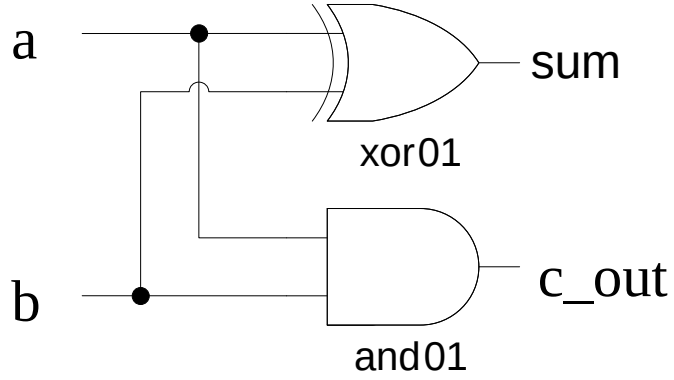
a\b	0	1
0	0	1
1	1	0

$sum = a \oplus b$

a\b	0	1
0	0	0
1	0	1

$c\_out = ab$





Lab I - Half Adder

- **(a) Using Verilog to implement a 1-bit Half Adder**

  Please implement with 3 methods

  1) **Structural description**
  2) **Data flow description**
  3) **Behavioral description**

- **(b) Simulation with waveform**

Lab I - Hint

Structural Description

Verilog allows three kinds of descriptions for circuits:

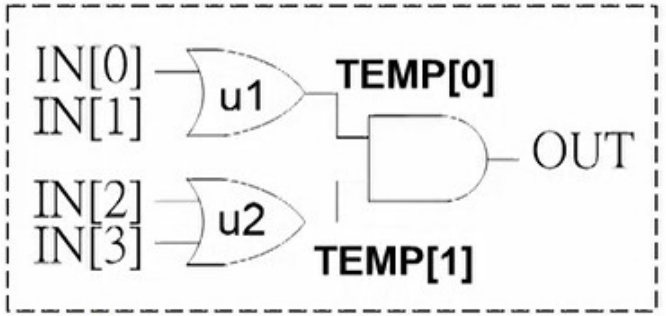
(1) Structural description (2) Data flow description (3) Behavioral description

Structural description:

```
1. module OR_AND_STRUCTURAL(IN,OUT);

2. input      [3:0]    IN;
3. output              OUT;
4. wire       [1:0]    TEMP;

5. or u1(TEMP[0], IN[0], IN[1]);
6. or u2(TEMP[1], IN[2], IN[3]);
7. and (OUT, TEMP[0], TEMP[1]);
8. endmodule
```



***Synthesized* (synthesis) +**
optimized by tools

Lab I - Hint

Data Flow Description

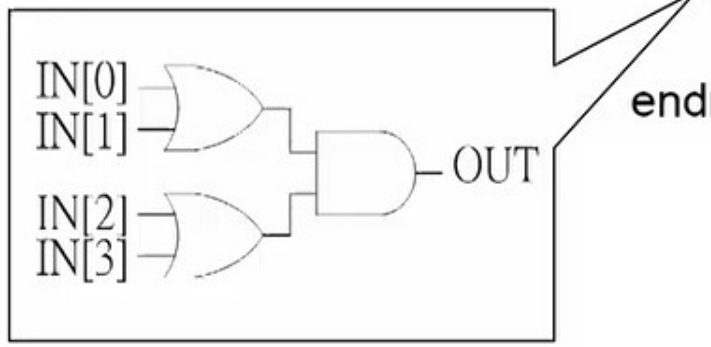
Data flow description

```
1.  module OR_AND_DATA_FLOW(IN, OUT);
2.  input       [3:0]       IN;
3.  output                  OUT;

4.  assign OUT = (IN[0] | IN[1]) & (IN[2] | IN[3]);

    endmodule
```

Synthesized and optimized by tools



Lab I - Hint

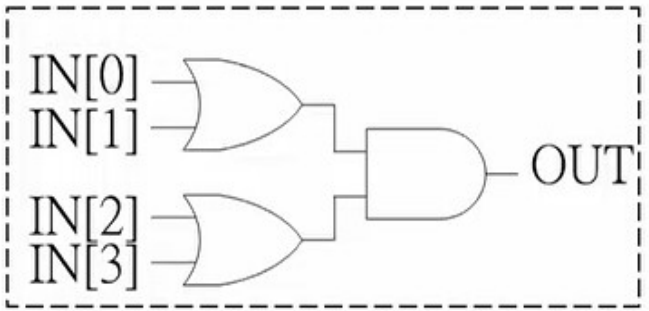
Behavioral (RTL) Description

Behavioral description

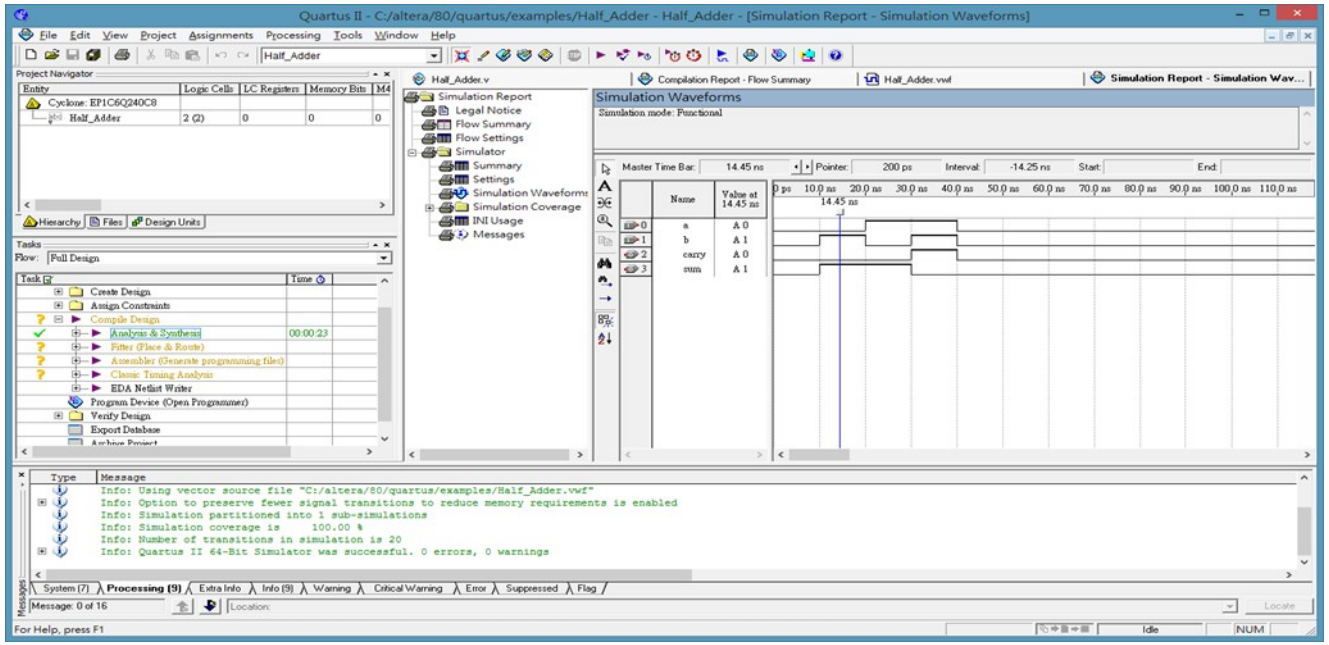
```
1.  module OR_AND_BEHAVIORAL(IN, OUT);

2.  input  [3:0]   IN;
3.  output         OUT;
4.  reg            OUT;

5.  always @(IN)
6.  begin
7.    OUT = (IN[0] | IN[1]) & (IN[2] | IN[3]);
8.  end
9.  endmodule
```



Lab I - Simulation with waveform



a	b	sum	carry
0	0	**0**	**0**
0	1	**1**	**0**
1	0	**1**	**0**
1	1	**0**	**1**

Lab II - Full Adder (1/2)

ab\c_in	0	1
00	0	1
01	1	0
11	0	1
10	1	0

ab\c_in	0	1
00	0	0
01	0	1
11	1	1
10	0	1

sum

$$= \bar{a}\bar{b}c\_in + a\bar{b}\bar{c}\_in + \bar{a}bc\_in + abc\_in$$

$$= (\bar{a}b + a\bar{b})\bar{c}\_in + (\bar{a}\bar{b} + ab)c\_in$$

$$= (a \oplus b)\bar{c}\_in + (\overline{a \oplus b})c\_in$$

$$= (a \oplus b) \oplus c\_in$$

c_out

$$= ab + \bar{a}bc\_in + a\bar{b}c\_in$$

$$= ab + (\bar{a}b + a\bar{b})c\_in$$

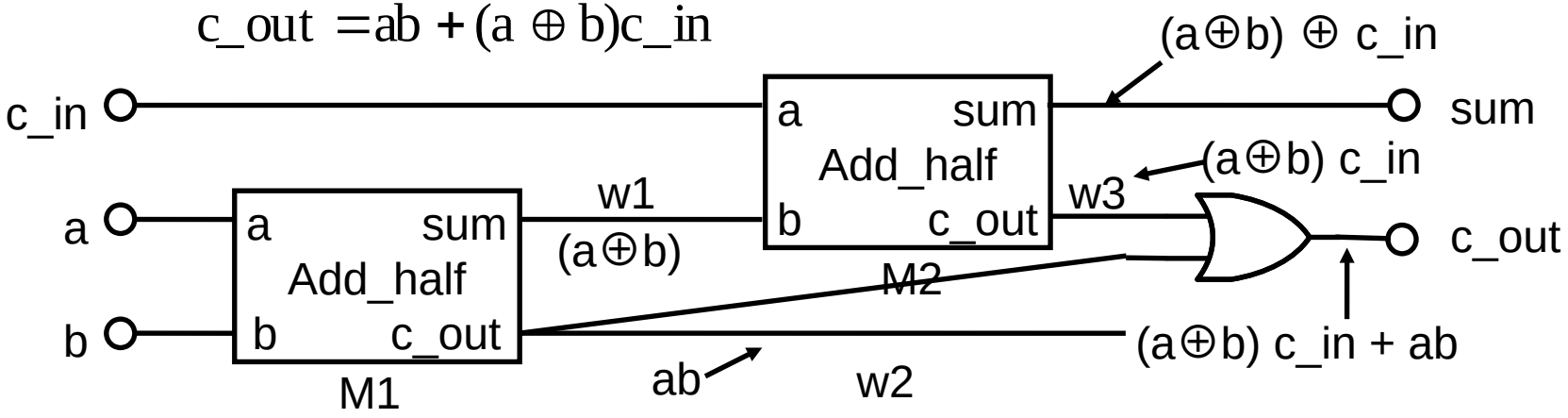
$$= ab + (a \oplus b)c\_in$$

Lab II - Full Adder (2/2)

You can implement a full adder with (2 half adder and 1 or gate).

$$sum = (a \oplus b) \oplus c\_in$$

$$c\_out = ab + (a \oplus b)c\_in$$



Lab II - Full Adder

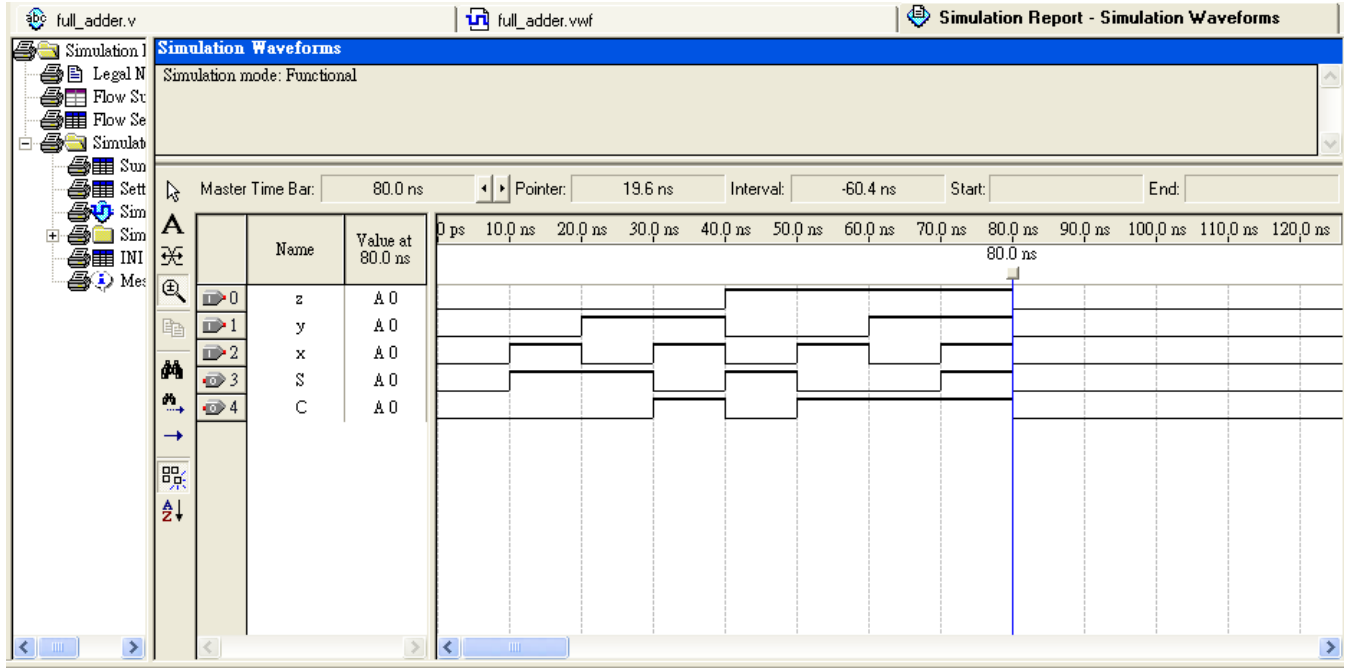
- **(a) Using Verilog to implement a 1-bit Full Adder**

  Please implement with 3 methods

  1) **Structural description(with 2 half adder + 1 or gate)**
  2) **Data flow description**
  3) **Behavioral description**

- **(b) Simulation with waveform**

Lab II - Simulation with waveform



z	y	x	S	C
0	0	0	**0**	**0**
0	0	1	**1**	**0**
0	1	0	**1**	**0**
0	1	1	**0**	**1**
1	0	0	**1**	**0**
1	0	1	**0**	**1**
1	1	0	**0**	**1**
1	1	1	**1**	**1**

Notice

- 請勿在桌面建立 Project 及請勿命名中文資料夾
- Device family 請確認與 FPGA Chip 符合 (10M50DAF484C7G)
- Top module name & Project name 需要一致
- 確認 module … endmodule 為 keyword 變成藍色字體