



## 1. Description

### 1.1. Project

Project Name	STM32H735G-DK
Board Name	custom
Generated with:	STM32CubeMX 6.11.0
Date	06/13/2024

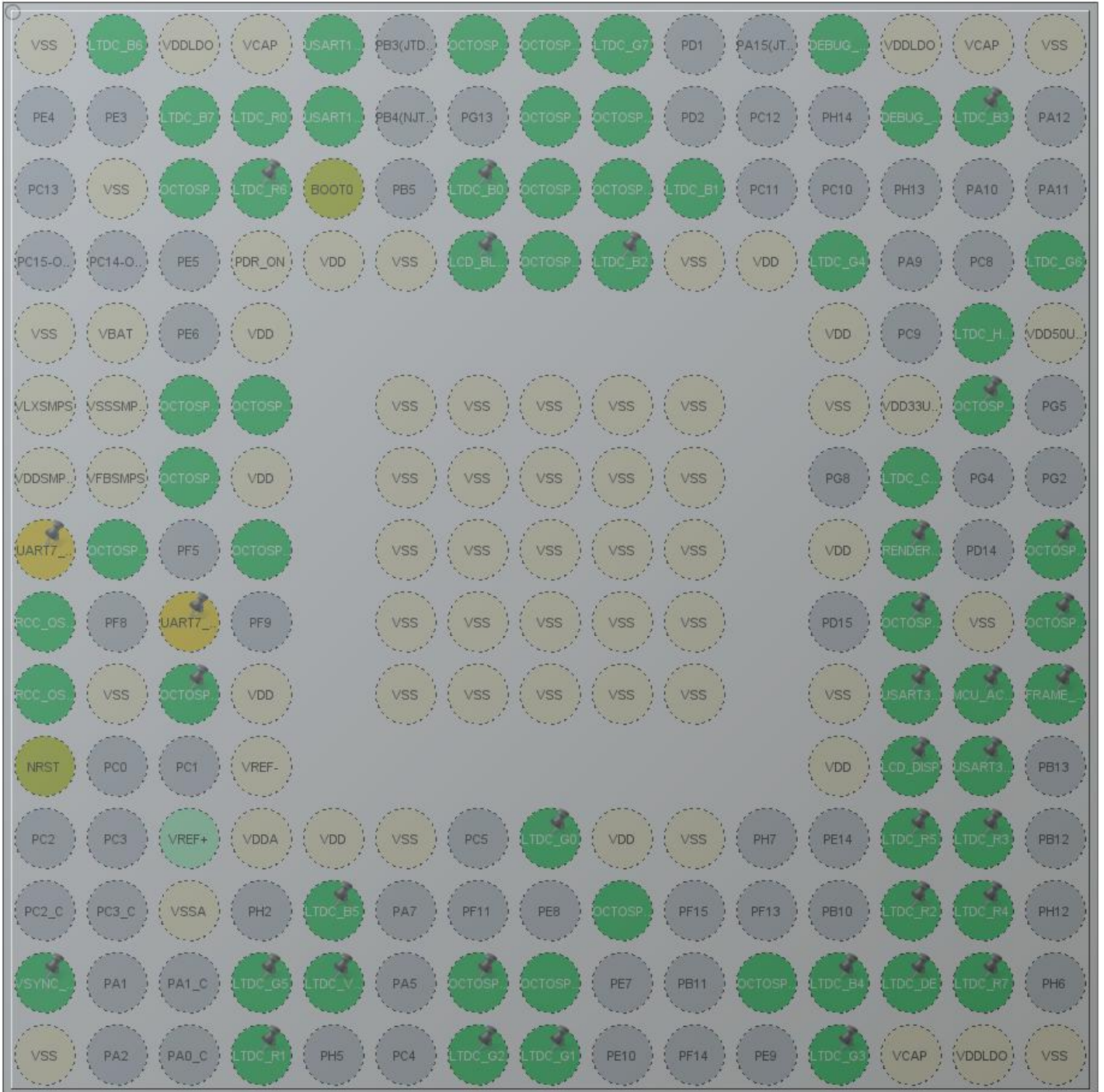
### 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H725/735
MCU name	STM32H735IGKx
MCU Package	UFBGA176
MCU Pin number	201

### 1.3. Core(s) information

Core(s)	Arm Cortex-M7
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## 2. Pinout Configuration



UFBGA176 +25 (Top view)

### 3. Pins Configuration

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PB8	I/O	LTDC_B6	
A3	VDDLDO	Power		
A4	VCAP	Power		
A5	PB6	I/O	USART1_TX	
A7	PG11	I/O	OCTOSPIM_P2_IO7	
A8	PG9	I/O	OCTOSPIM_P1_IO6	
A9	PD3	I/O	LTDC_G7	
A12	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
A13	VDDLDO	Power		
A14	VCAP	Power		
A15	VSS	Power		
B3	PB9	I/O	LTDC_B7	
B4	PE0	I/O	LTDC_R0	
B5	PB7	I/O	USART1_RX	
B8	PD7	I/O	OCTOSPIM_P1_IO7	
B9	PD5	I/O	OCTOSPIM_P1_IO5	
B13	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
B14	PA8	I/O	LTDC_B3	
C2	VSS	Power		
C3	PE2	I/O	OCTOSPIM_P1_IO2	
C4	PE1	I/O	LTDC_R6	
C5	BOOT0	Boot		
C7	PG14	I/O	LTDC_B0	
C8	PG10	I/O	OCTOSPIM_P2_IO6	
C9	PD4	I/O	OCTOSPIM_P1_IO4	
C10	PD0	I/O	LTDC_B1	
D4	PDR_ON	Power		
D5	VDD	Power		
D6	VSS	Power		
D7	PG15 *	I/O	GPIO_Output	LCD_BL_CTRL
D8	PG12	I/O	OCTOSPIM_P2_NCS	
D9	PD6	I/O	LTDC_B2	
D10	VSS	Power		
D11	VDD	Power		
D12	PH15	I/O	LTDC_G4	

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
D15	PC7	I/O	LTDC_G6	
E1	VSS	Power		
E2	VBAT	Power		
E4	VDD	Power		
E12	VDD	Power		
E14	PC6	I/O	LTDC_HSYNC	
E15	VDD50USB	Power		
F1	VLXSMPS	Power		
F2	VSSMPS	Power		
F3	PF1	I/O	OCTOSPIM_P2_IO1	
F4	PF0	I/O	OCTOSPIM_P2_IO0	
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F12	VSS	Power		
F13	VDD33USB	Power		
F14	PG6	I/O	OCTOSPIM_P1_NCS	
G1	VDDSMPS	Power		
G2	VFBSMPS	Power		
G3	PF2	I/O	OCTOSPIM_P2_IO2	
G4	VDD	Power		
G6	VSS	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G13	PG7	I/O	LTDC_CLK	
H1	PF6 **	I/O	UART7_RX	
H2	PF4	I/O	OCTOSPIM_P2_CLK	
H4	PF3	I/O	OCTOSPIM_P2_IO3	
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H12	VDD	Power		
H13	PG3 *	I/O	GPIO_Output	RENDER_TIME

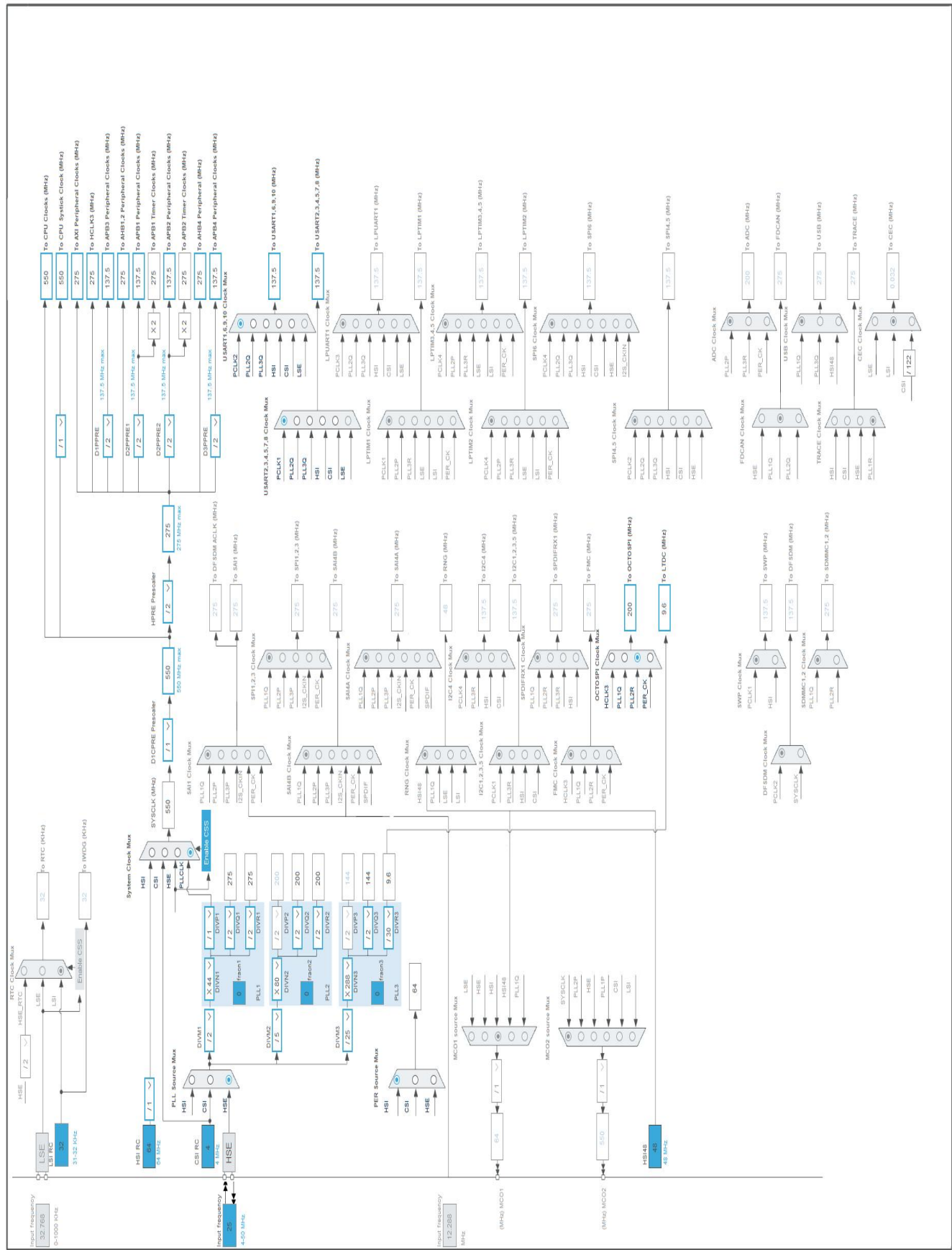
Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H15	PD13	I/O	OCTOSPIM_P1_IO3	
J1	PH0-OSC_IN	I/O	RCC_OSC_IN	
J3	PF7 **	I/O	UART7_TX	
J6	VSS	Power		
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J13	PD11	I/O	OCTOSPIM_P1_IO0	
J14	VSS	Power		
J15	PD12	I/O	OCTOSPIM_P1_IO1	
K1	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
K2	VSS	Power		
K3	PF10	I/O	OCTOSPIM_P1_CLK	
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K12	VSS	Power		
K13	PD9	I/O	USART3_RX	
K14	PB15 *	I/O	GPIO_Output	MCU_ACTIVE
K15	PB14 *	I/O	GPIO_Output	FRAME_RATE
L1	NRST	Reset		
L4	VREF-	Power		
L12	VDD	Power		
L13	PD10 *	I/O	GPIO_Output	LCD_DISP
L14	PD8	I/O	USART3_TX	
M4	VDDA	Power		
M5	VDD	Power		
M6	VSS	Power		
M8	PB1	I/O	LTDC_G0	
M9	VDD	Power		
M10	VSS	Power		
M13	PH11	I/O	LTDC_R5	
M14	PH9	I/O	LTDC_R3	
N3	VSSA	Power		
N5	PA3	I/O	LTDC_B5	

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N9	PG1	I/O	OCTOSPIM_P2_IO5	
N13	PH8	I/O	LTDC_R2	
N14	PH10	I/O	LTDC_R4	
P1	PA0 *	I/O	GPIO_Output	VSYNC_FREQ
P4	PH4	I/O	LTDC_G5	
P5	PA4	I/O	LTDC_VSYNC	
P7	PB2	I/O	OCTOSPIM_P1_DQS	
P8	PG0	I/O	OCTOSPIM_P2_IO4	
P11	PF12	I/O	OCTOSPIM_P2_DQS	
P12	PE12	I/O	LTDC_B4	
P13	PE13	I/O	LTDC_DE	
P14	PE15	I/O	LTDC_R7	
R1	VSS	Power		
R4	PH3	I/O	LTDC_R1	
R7	PA6	I/O	LTDC_G2	
R8	PB0	I/O	LTDC_G1	
R12	PE11	I/O	LTDC_G3	
R13	VCAP	Power		
R14	VDDLDO	Power		
R15	VSS	Power		

\* The pin is affected with an I/O function

\*\* The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration





## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	STM32H735G-DK
Project Folder	C:\TouchGFXProjects\stunning-parakeet
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x1000
Minimum Stack Size	0x1000

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_CRC_Init	CRC
4	MX_DMA2D_Init	DMA2D
5	MX_LTDC_Init	LTDC
6	MX_OCTOSPI1_Init	OCTOSPI1
7	MX_OCTOSPI2_Init	OCTOSPI2
8	MX_LIBJPEG_Init	LIBJPEG
9	MX_USART1_UART_Init	USART1
10	MX_USART3_UART_Init	USART3
12	MX_TouchGFX_Init	STMicroelectronics.X-CUBE-TOUCHGFX.4.23.2

Rank	Function Name	Peripheral Instance Name
13	MX_TouchGFX_Process	STMicroelectronics.X-CUBE-TOUCHGFX.4.23.2

## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H725/735
MCU	STM32H735IGKx
Datasheet	DS13312_Rev1

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

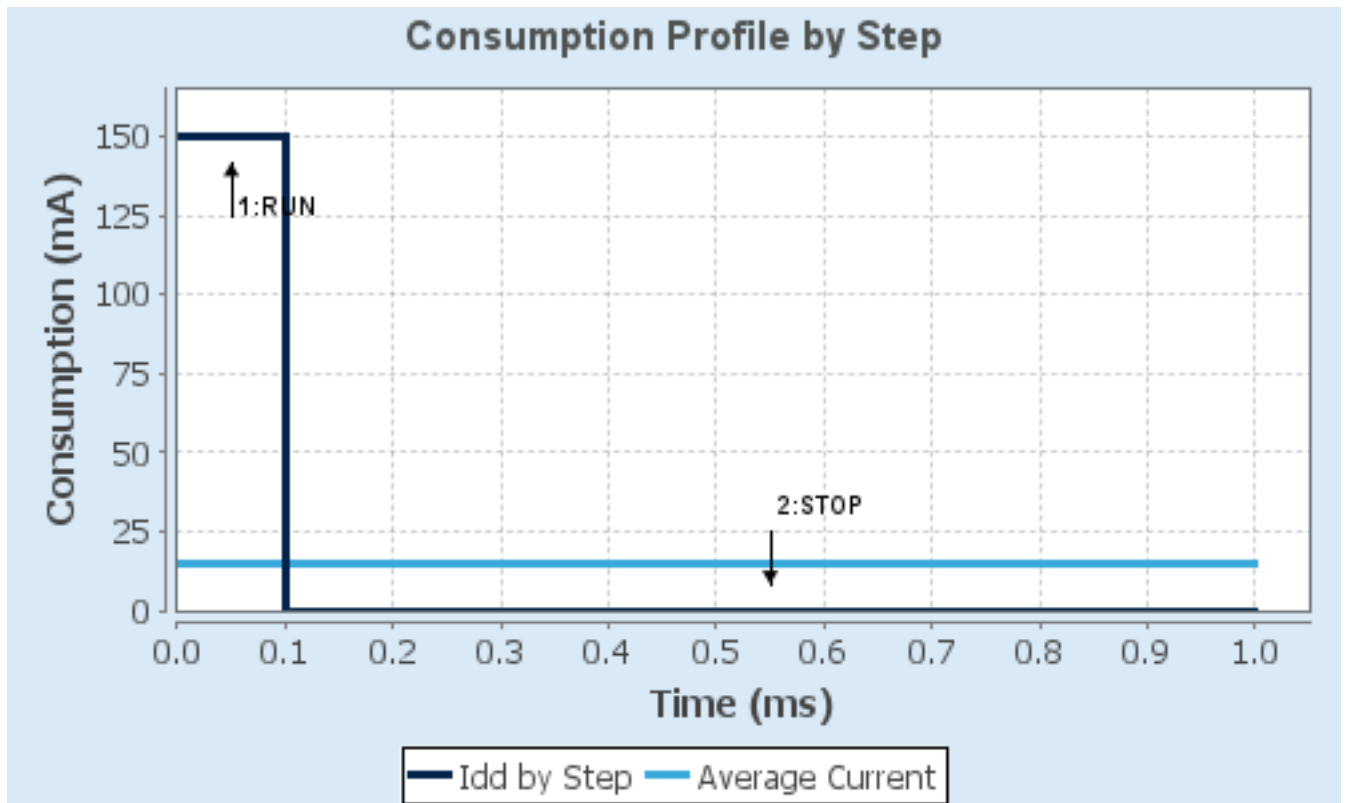
## 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0: Scale0/Boost	SVOS3: System-Scale3/SMPS-LDO
<b>D1 Mode</b>	DRUN	DSTANDBY
<b>D2 Mode</b>	DRUN	DSTANDBY
<b>D3 Mode</b>	DRUN	DSTOP
<b>Fetch Type</b>	SRAM1/FlashMode-ON/Cache	NA
<b>CPU Frequency</b>	550 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	LSE LowDrive RTC
<b>Clock Source Frequency</b>	8 MHz	32.768 kHz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	150 mA	2.5 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	1177.0	0.0
<b>Ta Max</b>	107.9	125
<b>Category</b>	In DS Table	In DS Table

## 1.5. Results

Sequence Time	1 ms	Average Current	15 mA
Battery Life	1 day, 17 hours	Average DMIPS	1177.0 DMIPS

## 1.6. Chart



## 2. Peripherals and Middlewares Configuration

### 2.1. CORTEX\_M7

#### 2.1.1. Parameter Settings:

##### Speculation default mode Settings:

Speculation default mode Disabled

##### Cortex Interface Settings:

CPU ICache Enabled \*

CPU DCache Enabled \*

##### Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers \*

##### Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled \*

MPU Region Base Address 0x24000000 \*

MPU Region Size 512KB \*

MPU SubRegion Disable 0x0 \*

MPU TEX field level level 0

MPU Access Permission ALL ACCESS PERMITTED \*

MPU Instruction Access DISABLE \*

MPU Shareability Permission DISABLE

MPU Cacheable Permission ENABLE \*

MPU Bufferable Permission ENABLE \*

##### Cortex Memory Protection Unit Region 1 Settings:

MPU Region Enabled \*

MPU Region Base Address 0x70000000 \*

MPU Region Size 512MB \*

MPU SubRegion Disable 0x0 \*

MPU TEX field level level 0

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access DISABLE \*

MPU Shareability Permission DISABLE

MPU Cacheable Permission DISABLE

MPU Bufferable Permission DISABLE

##### Cortex Memory Protection Unit Region 2 Settings:

MPU Region Enabled \*

MPU Region Base Address 0x70000000 \*

MPU Region Size	<b>8MB *</b>
MPU SubRegion Disable	<b>0x0 *</b>
MPU TEX field level	level 0
MPU Access Permission	<b>ALL ACCESS PERMITTED *</b>
MPU Instruction Access	<b>DISABLE *</b>
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	<b>ENABLE *</b>
MPU Bufferable Permission	<b>ENABLE *</b>

#### **Cortex Memory Protection Unit Region 3 Settings:**

MPU Region	<b>Enabled *</b>
MPU Region Base Address	<b>0x90000000 *</b>
MPU Region Size	<b>512MB *</b>
MPU SubRegion Disable	<b>0x0 *</b>
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS NOT PERMITTED
MPU Instruction Access	<b>DISABLE *</b>
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

#### **Cortex Memory Protection Unit Region 4 Settings:**

MPU Region	<b>Enabled *</b>
MPU Region Base Address	<b>0x90000000 *</b>
MPU Region Size	<b>64MB *</b>
MPU SubRegion Disable	<b>0x0 *</b>
MPU TEX field level	level 0
MPU Access Permission	<b>ALL ACCESS PERMITTED *</b>
MPU Instruction Access	<b>DISABLE *</b>
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	<b>ENABLE *</b>
MPU Bufferable Permission	DISABLE

#### **Cortex Memory Protection Unit Region 5 Settings:**

MPU Region	Disabled
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#### **Cortex Memory Protection Unit Region 6 Settings:**

MPU Region	Disabled
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#### **Cortex Memory Protection Unit Region 7 Settings:**

MPU Region	Disabled
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#### **Cortex Memory Protection Unit Region 8 Settings:**

MPU Region	Disabled
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**Cortex Memory Protection Unit Region 9 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 10 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 11 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 12 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 13 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 14 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 15 Settings:**

MPU Region Disabled

## 2.2. CRC

**mode: Activated**

### 2.2.1. Parameter Settings:

**Basic Parameters:**

Default Polynomial State Enable

Default Init Value State Enable

**Advanced Parameters:**

Input Data Inversion Mode None

Output Data Inversion Mode Disable

Input Data Format Bytes

## 2.3. DEBUG

**Debug: Serial Wire**

## 2.4. DMA2D

**mode: Activated**

### 2.4.1. Parameter Settings:

**Basic Parameters:**

Transfer Mode Register to Memory \*



Color Mode	<b>RGB888 *</b>
Output Offset	0

## 2.5. LTDC

### Display Type: RGB888 (24 bits)

#### 2.5.1. Parameter Settings:

##### **Synchronization for Width:**

Horizontal Synchronization Width	<b>41 *</b>
Horizontal Back Porch	<b>13 *</b>
Active Width	<b>480 *</b>
Horizontal Front Porch	<b>32 *</b>
HSync Width	40
Accumulated Horizontal Back Porch Width	53
Accumulated Active Width	533
Total Width	565

##### **Synchronization for Height:**

Vertical Synchronization Height	<b>10 *</b>
Vertical Back Porch	2
Active Height	<b>272 *</b>
Vertical Front Porch	2
VSyn Height	9
Accumulated Vertical Back Porch Height	11
Accumulated Active Height	283
Total Height	285

##### **Signal Polarity:**

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

##### **Layer Default Color:**

Red	0
Green	0
Blue	0

#### 2.5.2. Layer Settings:

##### **Layer Default Color:**

Layer 0 - Alpha	0
Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

#### Number of Layers:

Number of Layers	<b>1 layer *</b>
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#### Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	<b>480 *</b>
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	<b>272 *</b>

#### Pixel Parameters:

Layer 0 - Pixel Format	<b>RGB888 *</b>
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#### Blending:

Layer 0 - Alpha constant for blending	<b>255 *</b>
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant

#### Frame Buffer:

Layer 0 - Color Frame Buffer Start Address	<b>0x70000000 *</b>
Layer 0 - Color Frame Buffer Line Length (Image Width)	<b>480 *</b>
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	<b>272 *</b>

## 2.6. OCTOSPI1

**Mode: Octo SPI**

**Clock: Port1 CLK**

**Chip Select: Port1 NCS**

**Data Strobe: Port1 DQS (RWDS)**

**Data [3:0]: Port1 IO[3:0]**

**Data [7:4]: Port1 IO[7:4]**

### 2.6.1. Parameter Settings:

#### Generic:

Fifo Threshold	<b>4 *</b>
Dual Quad mode	Disable
Memory Type	<b>Macronix *</b>

Device Size	32
Device Type	Not defined
Chip Select High Time	<b>2 *</b>
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	<b>2 *</b>
Sample Shifting	None
Delay Hold Quarter Cycle	Disable
Chip Select Boundary	0
Delay Block	Disable
Maximum Transfer	0
Refresh Rate	0

## 2.7. OCTOSPI2

**Mode: HyperBus(TM)**

**Clock: Port2 CLK**

**Chip Select: Port2 NCS**

**Data Strobe: Port2 DQS (RWDS)**

**Data [3:0]: Port2 IO[3:0]**

**Data [7:4]: Port2 IO[7:4]**

### 2.7.1. Parameter Settings:

#### **Generic:**

Fifo Threshold	<b>4 *</b>
Dual Quad mode	Disable
Memory Type	HyperBus(TM)
Device Size	<b>24 *</b>
Device Type	Not defined
Chip Select High Time	<b>4 *</b>
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	<b>2 *</b>
Sample Shifting	None
Delay Hold Quarter Cycle	<b>Enable *</b>
Chip Select Boundary	<b>23 *</b>
Delay Block	<b>Enable *</b>

Maximum Transfer	0
Refresh Rate	<b>400 *</b>
<b>HyperBus(TM):</b>	
RW Recovery Time	<b>3 *</b>
Access Time	<b>6 *</b>
Write Access Latency	<b>Enable *</b>
Latency Mode	<b>Fixed *</b>

## 2.8. RCC

### High Speed Clock (HSE): Crystal/Ceramic Resonator

#### 2.8.1. Parameter Settings:

##### Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

##### RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	64

##### System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	3 WS (4 CPU cycle)

##### PLL range Parameters:

PLL1 input frequency range	Between 8 and 16 MHz
PLL2 input frequency range	Between 4 and 8 MHz
PLL3 input frequency range	Between 1 and 2 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range
PLL3 clock Output range	MEDIUM VCO range

## 2.9. SYS

### Timebase Source: TIM6

## 2.10. USART1

### Mode: Asynchronous

#### 2.10.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

##### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 2.11. USART3

### Mode: Asynchronous

#### 2.11.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## 2.12. FREERTOS

### Interface: CMSIS\_V2

#### 2.12.1. Config parameters:

##### API:

FreeRTOS API	CMSIS v2
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##### Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

##### MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

##### Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	<b>512 *</b>
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8

USE_APPLICATION_TASK_TAG	<b>Enabled *</b>
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

#### Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	<b>75000 *</b>
Memory Management scheme	heap_4

#### Hook function related definitions:

USE_IDLE_HOOK	<b>Enabled *</b>
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

#### Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

#### Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

#### Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	1024

#### Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

#### Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

#### CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

### 2.12.2. Include parameters:

#### **Include definitions:**

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

### 2.12.3. Advanced settings:

#### **Newlib settings (see parameter description first):**

USE\_NEWLIB\_REENTRANT                      **Enabled \***

#### **Project settings (see parameter description first):**

Use FW pack heap file                      Enabled

## **2.13. LIBJPEG**

**mode: Enabled**

### 2.13.1. Config parameters:

#### **Version:**

LIBJPEG version

8d



### MW configuration:

Data Stream management type	Stdio
FREERTOS	Enabled
HAVE_BOOLEAN	Undefined

### General Settings:

Use FREERTOS Memory Allocator	Enabled
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### RGB scanline format:

RGB_ORDERING	<b>BGR *</b>
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## 2.14. STMicroelectronics.X-CUBE-TOUCHGFX.4.23.2

### mode: GraphicsJjApplication

#### 2.14.1. TouchGFX Generator:

### Display:

Interface	<b>Parallel RGB (LTDC) *</b>
Framebuffer Pixel Format (LTDC)	RGB888
Width (LTDC)	480
Height (LTDC)	272
Framebuffer Strategy	<b>Double Buffer *</b>
Buffer Location	By Allocation

### Driver:

Application Tick Source	<b>LTDC *</b>
Use DMA2D Accelerator (ChromART)	<b>Yes *</b>
Real-Time Operating System	CMSIS_RTOS_V2

### Additional Features:

Vector Rendering	<b>Software *</b>
Vector Font Rendering	<b>Enabled *</b>

### Video Decoding:

Type	<b>Software *</b>
Concurrent videos	1
Strategy	<b>Single buffer *</b>
Decode Format	<b>RGB888 *</b>
Buffer Width	<b>480 *</b>
Buffer Height	<b>272 *</b>

\* User modified value

### 3. System Configuration

#### 3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
LTDC	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE0	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA8	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PG14	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD0	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD6	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PH15	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB1	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PH11	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH9	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PH8	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PH10	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PH4	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE13	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE15	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PH3	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB0	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE11	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
OCTOSPI1	PG9	OCTOSPIM_P1_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	OCTOSPIM_P1_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	OCTOSPIM_P1_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE2	OCTOSPIM_P1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	OCTOSPIM_P1_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG6	OCTOSPIM_P1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD13	OCTOSPIM_P1_	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
		IO3				
	PD11	OCTOSPIM_P1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD12	OCTOSPIM_P1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF10	OCTOSPIM_P1_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB2	OCTOSPIM_P1_DQS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
OCTOSPI2	PG11	OCTOSPIM_P2_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG10	OCTOSPIM_P2_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG12	OCTOSPIM_P2_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	OCTOSPIM_P2_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	OCTOSPIM_P2_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	OCTOSPIM_P2_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	OCTOSPIM_P2_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	OCTOSPIM_P2_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	OCTOSPIM_P2_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	OCTOSPIM_P2_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	OCTOSPIM_P2_DQS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PF6	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_BL_CTRL
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	RENDER_TIME

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Very High</b> *	MCU_ACTIVE
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Very High</b> *	FRAME_RATE
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_DISP
	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	<b>Very High</b> *	VSYNC_FREQ

### 3.2. DMA configuration

nothing configured in DMA service

### 3.3. BDMA configuration

nothing configured in DMA service

### 3.4. MDMA configuration

nothing configured in DMA service

### 3.5. NVIC configuration

#### 3.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
USART1 global interrupt	true	5	0
USART3 global interrupt	true	5	0
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	0	0
LTDC global interrupt	true	5	0
DMA2D global interrupt	true	5	0
PVD/AVD through EXTI Line detection Interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FPU global interrupt	unused		
LTDC Error global Interrupt	unused		
OCTOSPI1 global interrupt	unused		
HSEM1 global interrupt	unused		
OCTOSPI2 global interrupt	unused		

#### 3.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
USART1 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
USART3 global interrupt	false	true	true
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	false	true	true
LTDC global interrupt	false	true	true
DMA2D global interrupt	false	true	true

\* User modified value



## 4. System Views

### 4.1. Category view

#### 4.1.1. Current

## 5. Software Pack Report

### 5.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	X-CUBE-TOUCHGFX	4.23.2	Class : Graphics Group : Application Variant : TouchGFX Generator Version : 4.23.2

## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip">https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32h7-svd.zip">https://www.st.com/resource/en/svd/stm32h7-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
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Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/brstm32h7.pdf">https://www.st.com/resource/en/brochure/brstm32h7.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/brstm32h7vl.pdf">https://www.st.com/resource/en/brochure/brstm32h7vl.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf</a>
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the-dma-request-router-stmicroelectronics.pdf

- Application Notes [https://www.st.com/resource/en/application\\_note/an5281-how-to-use-otfdec-for-encryptiondecryption-in-trusted-environment-on-stm32h7bxxx-and-stm32h73xx-microcontrollers-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an5281-how-to-use-otfdec-for-encryptiondecryption-in-trusted-environment-on-stm32h7bxxx-and-stm32h73xx-microcontrollers-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an5337-stm32h7-series-lifetime-estimates-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an5337-stm32h7-series-lifetime-estimates-stmicroelectronics.pdf)
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User Manuals	<a href="https://www.st.com/resource/en/user_manual/um2331-stm32h7-singlecore-series-safety-manual-stmicroelectronics.pdf">https://www.st.com/resource/en/user_manual/um2331-stm32h7-singlecore-series-safety-manual-stmicroelectronics.pdf</a>