Lab 4

Subtractor

4.1 Introduction

In the next several labs, we are going to compare various implementations of a two-bit adder/subtractor. This is a relatively simple circuit that has sufficient complexity to highlight some important aspects of digital circuit design. (By comparison, a TI-89 calculator uses a 16-bit processor, your cell phone and computer are 32 or 64-bit, and all of these do *vastly* more than add and subtract.)

4.2 Objectives

After completing this lab, you should be able to:

- Describe the operation of a two-bit adder/subtractor
- Develop a moderately complex circuit on a breadboard using standard electrical parts
- Develop your own test procedure and verify operation of the circuit
- Recognize that digital circuits quickly become complex and difficult to implement in hardware

4.3 Background

You should understand the operation of half, full, and ripple adders from the previous lab. If not, see this tutorial or seek help from your classmates, instructor, textbook, etc.

4.4 Pre-Lab

1. Draw a schematic of the two-bit adder from the previous lab.
   - Group gates together in half adders and full adders
   - Draw dashed lines around these and indicate “HA” or ”FA”
   - Arrange the full adders and wires in the correct order, i.e. the MSB on the top/left and LSB on the bottom/right
   - Use a full page. Leave space to write next to your wires and also around the outside of your drawing to add other components

   Submit a copy of your drawing to Canvas. Bring the original with you to lab.

2. On the back of your schematic page or a separate page, copy this table and fill in the decimal equivalents of the two’s complement binary numbers. One hint is provided for you. This will be a useful reference during lab.

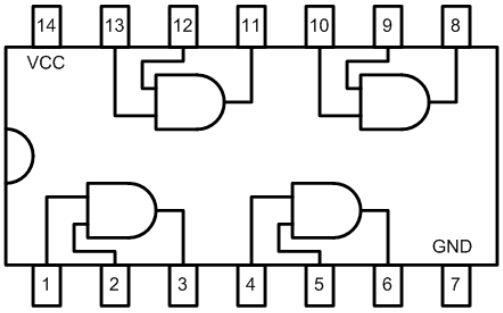
2-bit	3-bit	Dec
00	000	
01	001	
	010	
	011	
	100	
	101	
10	110	
11	111	-1

4.5 Materials

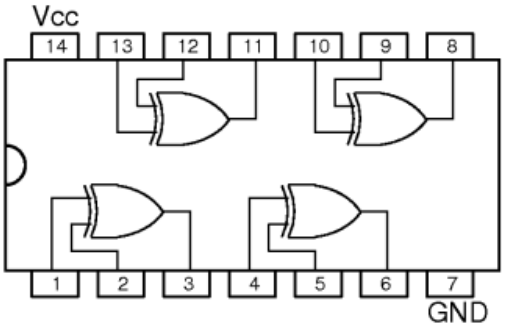
You will need:

- three 7486 Xor ICs
- two 7408 And ICs
- breadboard
- wires

Note that this lab could be done with one 7408 And chip, but using two will make it easier to build and



7408 Quad 2 Input AND



7486 Quad 2 Input XOR

Figure 4.1: Pin diagrams for 7408 and 7486

troubleshoot. The pinout diagrams for these chips are shown in Figure 4.1.

4.6 Lab Procedures

Remember to:

- Draw a schematic/wiring diagram (done as the Pre-lab and first step in the Experiment)
- Order your inputs and outputs according to bit significance
- Color code your wires
- Space your components
- Minimize wire lengths
- Carefully remove chips

4.7 Experiment

4.7.1 Subtraction

Subtraction is just adding a negative number. If you think of it this way, we only need a way to make the second number negative. We do negative numbers by two's compliment. That means flip every bit and add one. The add one part is easy, we just make the carry input to the first full adder 1 instead of 0 to subtract. We can handle this by connecting the carry input to a switch or button, often called the mode (M): 0 means add, 1 means subtract.

Now, how do we flip a bit by some control signal? Consider for a second the truth table for XOR:

A	B	Xor
0	0	0
0	1	1
1	0	1
1	1	0

I put in an extra line to separate when A = 0 from A = 1. Compare B and XOR when A is zero then when it is one. What do you notice? How can we use this to flip the bits when we set our mode switch (M) to 1?

Before building your circuit, fill out the expected results table (ERT) on the circuit demonstration page at the end of this document.

4.7.2 Adder/Subtractor

Choose one of your schematics (from the pre-lab) and add the components necessary to allow for subtraction.

Instead of drawing a wiring diagram, we are going to use another common industry practice and label the pins of each gate with their pin numbers. For example, one of your XOR gates might use pins 1 and 2 as the inputs and pin 3 as the output. Write these numbers next to those pins on your schematic.

Since we have multiple ICs of each type, we also need to label these. The typical way to do this is by giving each chip a designator and writing that designator next to the part on the schematic. Use a naming scheme of 'A' for AND (7408) chips and 'X' for XOR (7486) chips, followed by a number. With two AND chips, you'll have A1 and A2. With three XOR chips, you'll have X1, X2, and X3. List power and ground connections at the bottom of your schematic.

Figure 4.2 provides an example of all of the labeling that you need. The XOR gate is from chip X1, pins

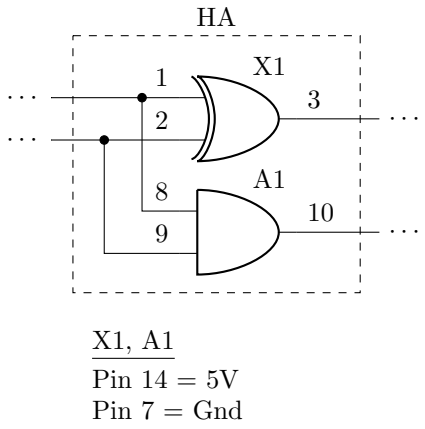


Figure 4.2: Example schematic drawing with labels

1, 2, and 3. The AND gate is from chip A1, pins 8, 9, and 10.

Construct your circuit and test it using the combinations from your ERT.

4.7.3 Overflow

Do your test results match what you expect? Did you notice that the carry output doesn't indicate the sign of the result like we would expect? That is, the result isn't in two's complement. This is because carry for addition and "borrow" for subtraction are slightly different. We might also refer to this as the "overflow" of a *signed* number operation, as opposed to the carry of an *unsigned* operation.

Compare the results of the two operations shown in Table 4.1. On the left is "regular" subtraction of two binary numbers. In decimal, this is equivalent to $2 - 1 = 1$. On the right is the *addition* of A with the two's complement of B, or -B. Notice that the MSB is different. The left result indicates positive 1 as we expect, while the result on the right would be -3 if we interpret it as a two's complement number.

Table 4.1: Subtraction vs. adder/subtractor

Subtraction		Adding 2's Comp	
$\curvearrowright$	*borrow*	$\curvearrowleft$	*carry*
1 0	A	1 0	A
− 0 1	B	+ 1 1	-B
0 0 1	(+1)	1 0 1	(-3)

We can fix this by inverting the MSB when we are using our adder as a subtractor. As before, how can we flip the carry/borrow output bit when our circuit is operating as a subtractor?

Make this modification to your schematic and your actual circuit, and then test it again. Demonstrate it to your instructor. Take a picture of your completed circuit.

4.8 Deliverables

Submit a report using the provided template and include:

1. A picture of your assembled circuit
2. Complete two-bit adder/subtractor schematic with:
   (a) IC and pin labels
   (b) Boxes around HAs and FAs
   (c) Components added for subtraction
3. The Circuit Demonstration Page with your completed ERT and all circuits approved by your instructor

Answer the following questions:

1. Why did we use two full adders instead of a half adder and a full adder?
2. How many input combinations would it take to exhaustively test the adder/subtractor?
3. Why were the combinations given in the truth table chosen?
4. Do the results from your adder/subtractor match what you would expect from theory? Explain any discrepancies.

Circuit Demonstration Page

Student names: _____

_____ _____

Instructor Signatures

Separate Full Adders _____

Two-Bit Adder _____

Adder/Subtractor _____

Inputs		Expected Results			Actual Results
A	B	B 2's comp	Sub	Dec	Sub
00	01				
00	10				
00	11				
01	01				
10	01				
10	00				