

ELC 2137 Lab 04: Subtractor

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Summary

In this lab we modified our full adder from the last lab, to make the two bit adder/subtractor in this lab. The only adjustment we had to make to our previous adder was to add two additional XOR gates with new inputs and a mode input (previously Cin).

Q&A

1) Why did we use two full adders instead of a half adder and a full adder?

We used the 2 full adders we built in the last lab instead of a half adder and full adder, because it was a simple modification.

2) How many input combinations would it take to exhaustively test the adder/subtractor?

4069

3) Why were the combinations given in the truth table chosen?

These values test all the possible combinations in one test.

4) Do the results from your adder/subtractor match what you would expect from theory? Explain any discrepancies.

Yes, the results match what I would expect from theory. When you look at the truth table you can see that the last two bits of the subtracted answer match the last two bits of the B inputs 2 compliment. The first bit of the answer is the only different bit, which makes sense because the first bit in the 2 compliment is a sign bit.

Results

ELC 2137

Lab 4. Subtractor


Circuit Demonstration Page

Student names: Kyra Rose

Instructor Signatures

Separate Full Adders

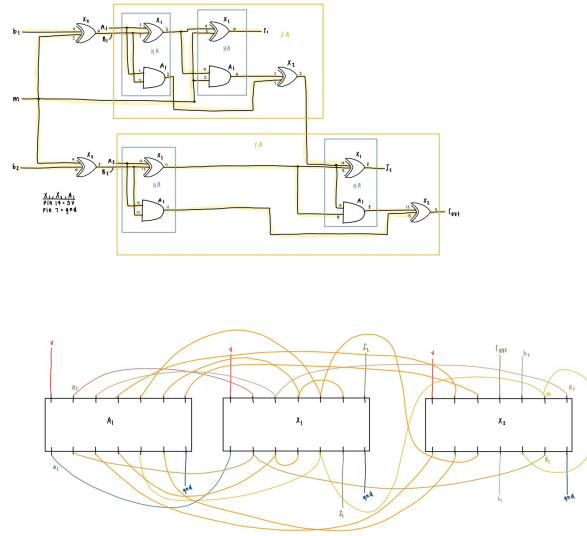
Two-Bit Adder

Adder/Subtractor 

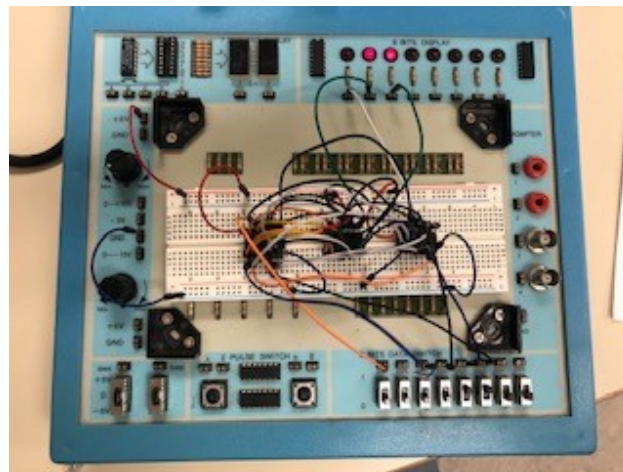
Inputs		Expected Results			Actual Results
A	B	B 2's comp	Sub	Dec	Sub
000	001	111	111	- 7	011
000	010	110	110	- 6	010
000	011	101	101	- 5	001
001	001	111	000	0	100
010	001	111	001	1	101
010	000	000	010	2	110

4

Circuit Demonstration Page



Subtractor Wiring Diagram and Schematic



Subtractor

Code

Listing 1: Direct Verilog code example

```
\begin{center}

\includegraphics[width=0.5\textwidth]{circuit demo page 4}

\caption{Circuit Demonstration Page}
```

```
\includegraphics[width=0.5\textwidth]{schematic}  
\caption{Subtractor Wiring Diagram and Schematic}  
\includegraphics[width=0.5\textwidth]{subtractor}  
\caption{Subtractor}  
\end{center}
```
