

V-by-One[®] HS Standard
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1. Introduction

1.1. Objectives

- V-by-One® HS targets a high speed data transmission of video signals based on internal connection of the equipment.
- V-by-One® HS pursues easier usage and lower power consumption compared with the current internal connection.
- V-by-One® HS supports up to 4Gbps data rate (effective data rate 3.2Gbps).
- V-by-One® HS supports scrambling and Clock Data Recovery (CDR) to reduce EMI.
- V-by-One® HS supports CDR to solve the skew problem between clock and data at conventional transfer system.

1.2. Technical Overview

With V-by-One® HS proprietary encoding scheme and CDR architecture, V-by-One® HS technology enables transmission up to 40bit video data, up to 24bit CTL data, Hsync, Vsync and Data Enable (DE) by some differential pair cables with minimal external components.

As shown in Figure 1, V-by-One® HS link includes data lanes, Hot Plug Detect signal (HTPDN), and CDR Lock signal (LOCKN). Number of data lanes is decided with the pixel rate and color depth (see Table 1). HTPDN connection between transmitter and receiver can be omitted as an application option.

As optional functions, it is possible to implement transmitter pre-emphasis and receiver equalizer.

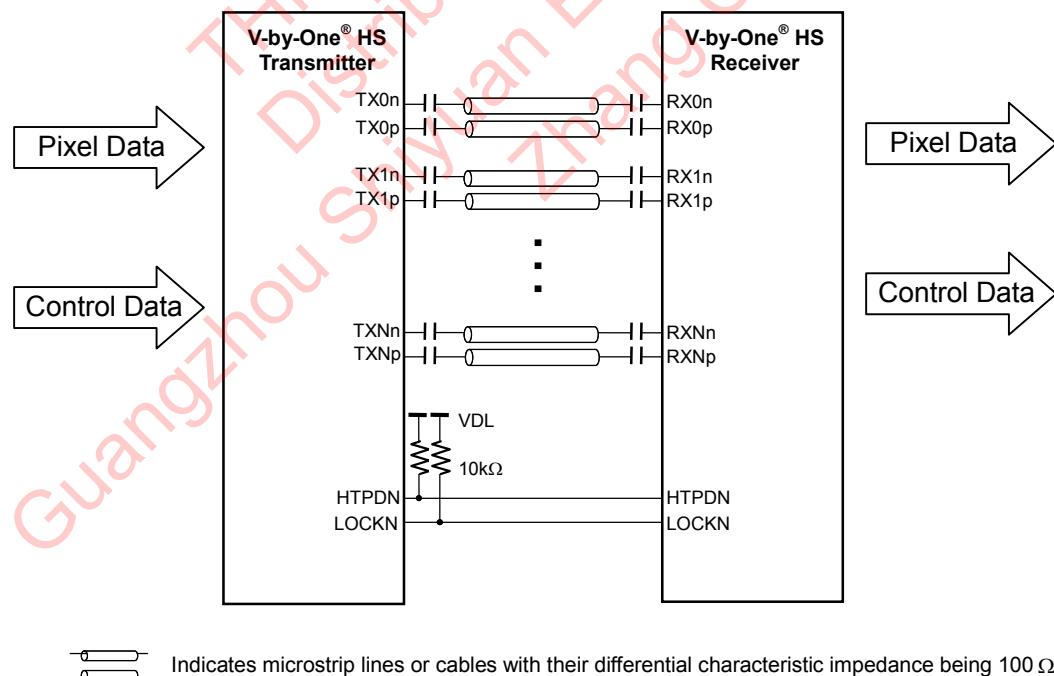


Figure 1 V-by-One® HS Link System Diagram

1.2.1. Transmitter

V-by-One® HS transmitter consists of packer, scrambler, encoder, serializer, and transmitter link monitor (Figure 3). Transmitter link monitor constantly monitor LOCKN and HTPDN signals. If the LOCKN signal is high, transmitter executes the CDR training. Transmitter sends the CDR training pattern on the CDR training mode. When CDR locked, transmitter shifts from CDR training mode to the normal mode, and then it starts to transmit input data from user logic.

1.2.2. Receiver

V-by-One® HS receiver consists of unpacker, descrambler, decoder, deserializer and receiver link monitor. The receiver synchronizes the pixel clock while referring to the CDR training pattern on the CDR training mode. After shifting from the CDR training mode to the normal mode, the receiver aligns byte and bit position using ALN training pattern. About ALN training, please refer to 2.2.5.2 in page 25).

1.2.3. Data Lane

Data lane is AC-coupled differential pairs with termination.

Transmission rate is able to be set up to 4Gbps depend on video pixel clock rate and bit depth.

1.2.3.1. Recommended Data Lane

Table 1 Video Data Format vs. Number of Lane Example

Resolution	Refresh Rate (Pixel clock)	Color Depth	Number of Data Lane*
HD e.g. 1280 x 720p	60Hz(74.25MHz)	18/24/30/36 bit	1
	120Hz(148.5MHz)	18/24/30/36 bit	2
	240Hz(297MHz)	18/24/30/36 bit	4
Full HD e.g. 1920 x 1080p	60Hz(148.5MHz)	18/24/30/36 bit	2
	120Hz(297MHz)	18/24/30/36 bit	4
	240Hz(594MHz)	18/24/30/36 bit	8
	480Hz(1188MHz)	18/24/30/36 bit	16
Cinema Full HD e.g. 2560 x 1080p	60Hz(185MHz)	18/24/30 bit	2
	120Hz(370MHz)	18/24/30 bit	4
	240Hz(740MHz)	18/24/30 bit	8
4K x 2K e.g. 3840 x 2160p	60Hz(594MHz)	18/24/30/36 bit	8
	120Hz(1188MHz)	18/24/30/36 bit	16
	240Hz(2376MHz)	18/24/30/36 bit	32

* Another lane number could be chosen; however, for the interoperability, those are STRONGLY recommended.

1.2.3.2. Data Lane Consideration

This chapter is informative only. It shows the procedure to select the minimum and maximum number of lanes necessary for the target application.

As a 1st step, [byte mode] (please refer to 2.1.1.4) is chosen from 3, 4, or 5 depending upon color depth. Literally 3, 4, or 5 byte mode conveys nominal 3, 4, or 5byte data. For example, 10bit per color RGB image requires 30 bit data per pixel; therefore, 4 byte mode which conveys 4 byte (32 bit) is enough to carry the data.

As a 2nd step, total bit rate which is physically transmitted on V-by-One[®] HS line should be estimated. Because V-by-One[®] HS uses 8b10b encoding scheme, encoded data amount which is physically transmitted is 10bit per nominal decoded 8bit (1 byte) of original data. Multiplying [pixel clock] of the target application by encoded data amount per pixel results into [encoded total bit-rate] of V-by-One[®] HS transmission.

$$[\text{encoded total bit-rate}] (\text{bps}) = [\text{byte mode}] (\text{byte}) \times 8 \times \frac{10}{8} \times [\text{pixel clock}] (\text{Hz})$$

[encoded bit-rate per lane] can be calculated as [total bit rate] over [number of lanes]. [number of lanes] should be chosen properly so that [encoded bit-rate per lane] is above 600Mbps and below 4Gbps.

$$600\text{Mbps} \leq [\text{encoded bit-rate per lane}] (\text{bps}) = \frac{[\text{encoded total bit-rate}] (\text{bps})}{[\text{number of lanes}]} \leq 4\text{Gbps}$$

[number of lanes] should be selected appropriate to signal handling in applications. For example, in case of video signal transmission, [number of lanes] is recommended to be divisor of Hactive, Hblank, and Htotal pixel number like 1, 2, 4, 8, etc. in order to help signal processing.

1.2.4. HTPDN Signal

HTPDN indicates connecting condition between the transmitter and the receiver. HTPDN of the transmitter side is high when the receiver is not active or not connected. Then transmitter can enter into the power down mode. HTPDN is set to low by the receiver when receiver is active and connects to the transmitter, and then transmitter must start up and transmit CDR training pattern for link training. HTPDN is open drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

HTPDN connection between the transmitter and the receiver can be omitted as an application option. In this case, HTPDN at the transmitter side should always be taken as low.

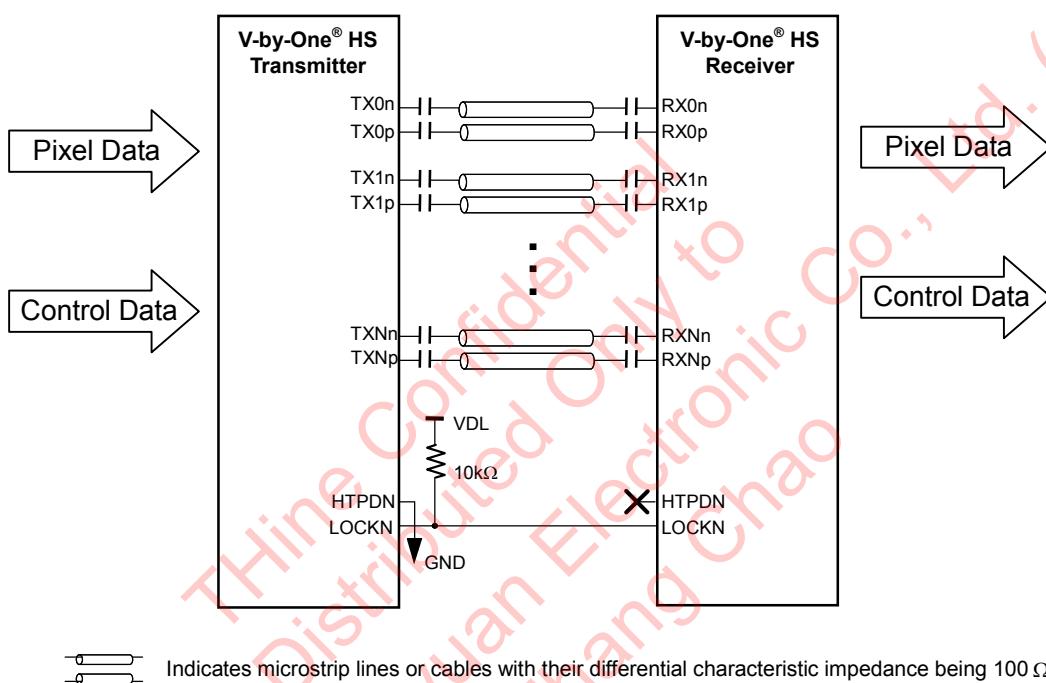


Figure 2 V-by-One® HS Link System without HTPDN Connection Schematic Diagram

1.2.5. LOCKN Signal

LOCKN indicates whether the CDR PLL is in the lock state or not. LOCKN at the transmitter input is set to high by pull-up resistor when receiver is not active or at the CDR PLL training state. LOCKN is set to low by the Receiver when CDR lock is done. Then the CDR training mode finishes and transmitter shifts to the normal mode. LOCKN is open drain output at the receiver side. Pull-up resistor is needed at the transmitter side. When HTPDN is included in an application, the LOCKN signal should only be considered when the HTPDN is pulled low by the receiver.

2. Link Specification

V-by-One® HS link configuration is shown in Figure 3.

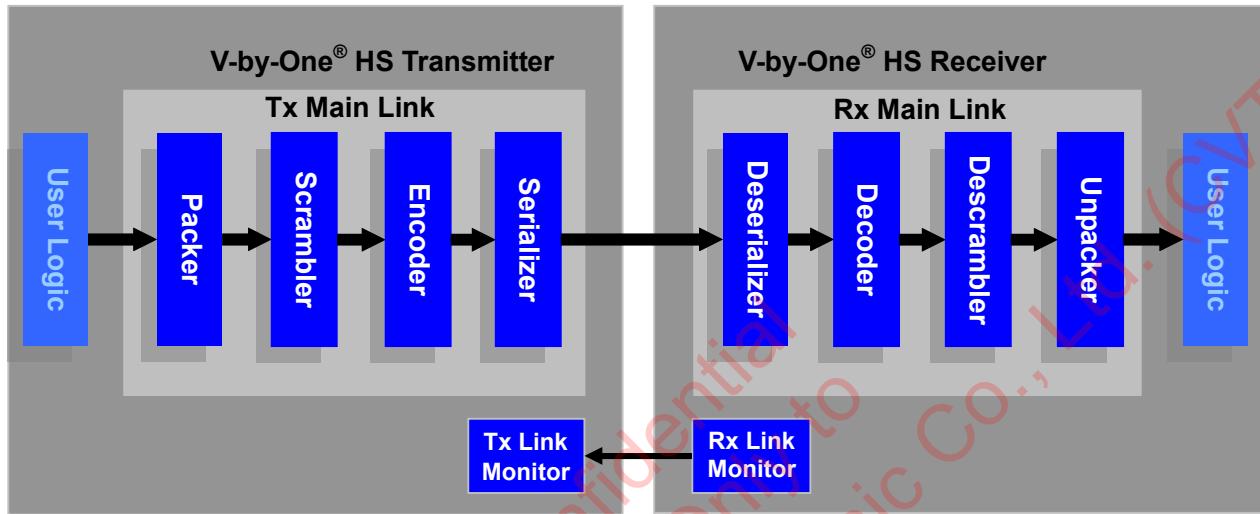


Figure 3 Link Configuration

The link connection is established as follows.

At first, the link training for CDR is performed. After link training finished, the transmitter starts the normal mode operation.

In the packer, the input data from user logic are packed to the packet include 8bit data character. After the packing, packets are scrambled with pseudo random numbers in the scrambler. On encoder, the scrambled 8bit packet data is encoded to 10bit character for an approximate DC balance as well as sufficient 0-1 and 1-0 transitions for the CDR. At last, 10bit data character is serialized to 1bit stream by the serializer.

The receiver performs the inverse process to convert the serial data from the transmitter to the pixel data for user logic.

2.1. Functional Specification

2.1.1. Packer and Unpacker

2.1.1.1. Interface

Packer generates the packet that consists of every 8bits. The packet includes pixel data (D), control data (CTL) and timing data (Hsync, Vsync, DE). The data mapping of a packet is determined by the framing byte size. The order of packer output is that the least significant byte (byte0) is the first and most significant byte is the last. Regarding the framing byte size and byte order, refer to the Table 2 in chapter 2.1.1.4. The D/K signal is used for the selection of D code and K code at the 8b/10b encoder/decoder block. Regarding the 8b/10b encoder/decoder, refer to chapter 2.1.3.

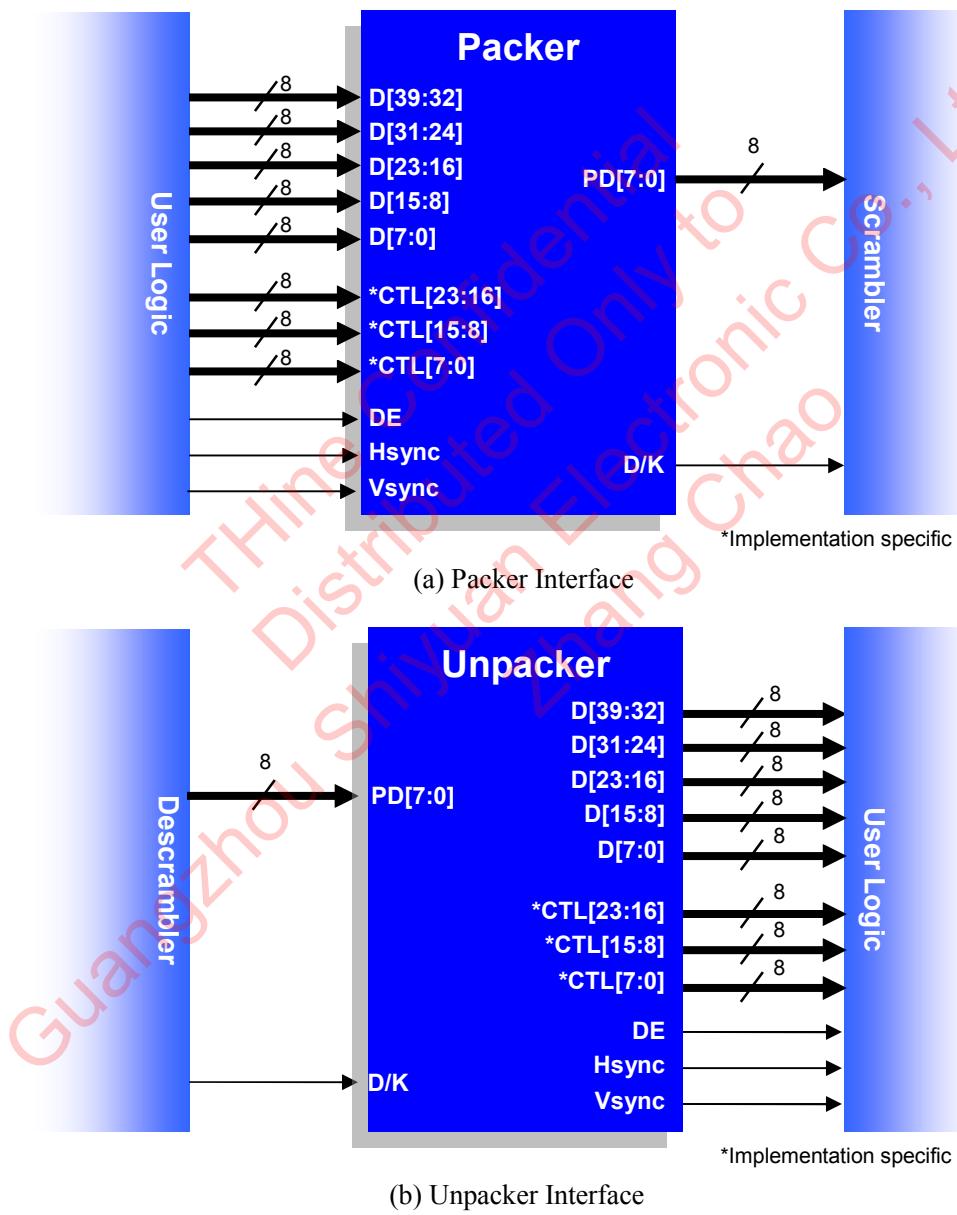


Figure 4 Packer and Unpacker Interface

2.1.1.2. Mapping Symbols for Framing

The following five control symbols are used for framing symbols (FS).

- **FSACTIVE**

Pixel data is packed during the DE active (DE = high) period. All bytes in this period are D codes. ‘DE high active’ is defined polarity.

- **FSBS (Blanking Start)**

Inserted right after the last active pixel. Vsync and Hsync data is packed into byte0 and byte1. All bytes in this FSBS are K code **.

- **FSBP (Blanking Payload)**

Inserted between BS and BE period. In this term, Vsync and Hsync data are packed into byte0 and byte1, it is permitted to pack CTL data into byte 2~4. All bytes in this period are D codes. The duration of FSBP is calculated as ;

$$[\text{Duration of FSBP}] = [\text{Duration of Blanking Period}] - 2 \text{ pixel}$$

- **FSBE (Blanking End)**

Inserted right before the first active pixel. Vsync, Hsync data and BE code is packed into byte0 and byte1. All bytes in this FSBE are K code.

- **FSBE_SR (Blanking End and Scrambler Reset)**

The first FSBE just after Vsync active period must be replaced with FSBE_SR for resetting the Linear Feedback Shift Register (LFSR) of the scrambler and descrambler. In addition, the input interval of FSBE_SR must be less than or equal to 512 times of FSBE input. The count of FSBE should be reset each time FSBE_SR is sent (See Figure 5). The data in FSBE_SR contains Vsync, Hsync, and BE_SR code of the K code.

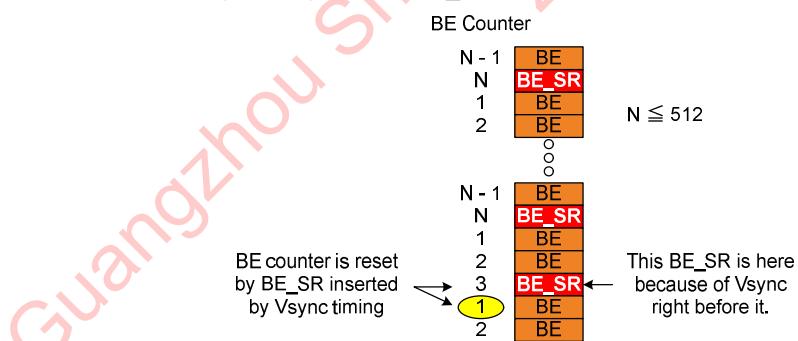


Figure 5 BE_SR Counter

Polarity of Vsync and Hsync can be both ‘high active’ and ’low active’, implementation specific as usage. ‘DE high active’ is V-by-One® HS default and all suppliers have to support this polarity.

** Note: see Table 4 about the definition of K code.

2.1.1.3. Mapping Diagram from Video Timing Chart

The relationship between the video timing and framing symbols are shown in Figure 6.

About the packed data for each framing symbols, refer to chapter 2.1.1.4.

The red arrow in the Figure 6 indicates the replacement of FSBE with FSBE_SR.

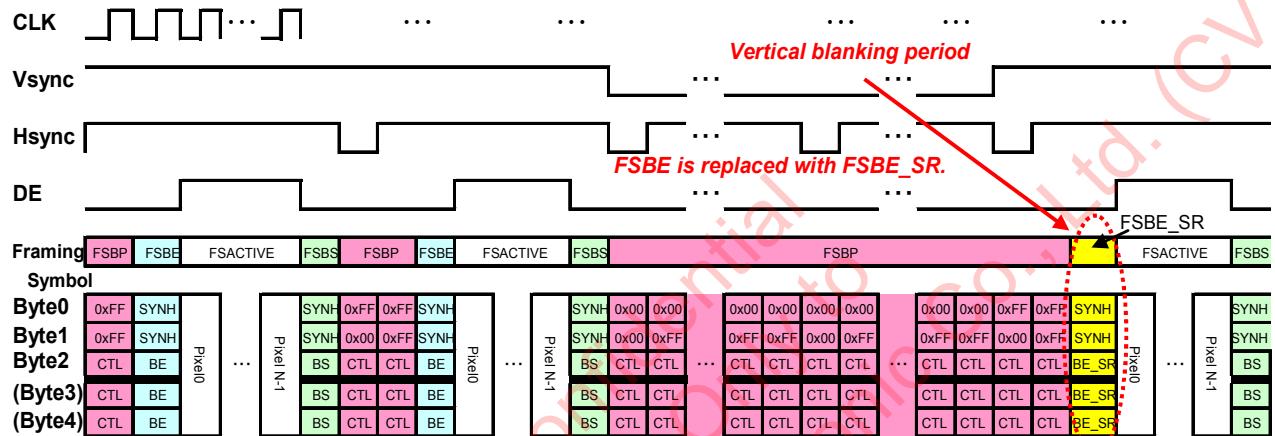


Figure 6 Relationships between Video Timing and Framing Symbols

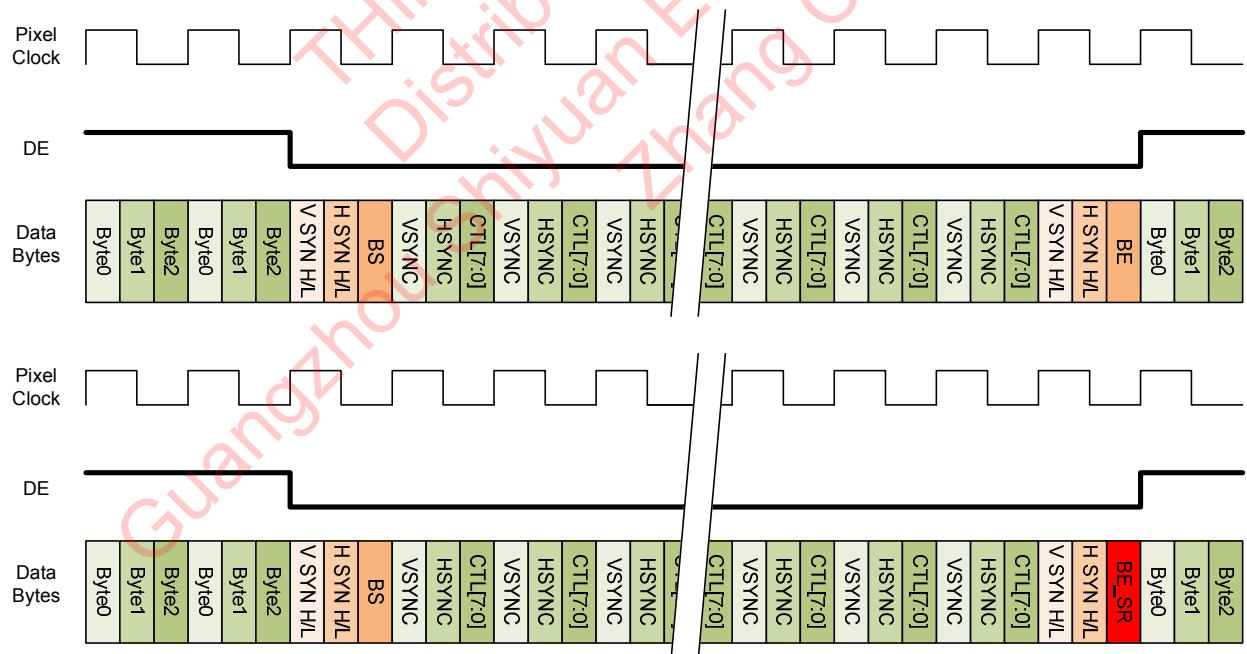


Figure 7 Packer Output Sequence with Framing Symbols (3byte mode)

2.1.1.4. Packet Data Mapping

The packer and unpacker data mapping is shown in Table 2 and Table 3. It is allowable to select 3~5byte modes depending on the video data bit width. Support of all byte modes from 3 to 5 is not required in the V-by-One® HS standard because most devices are designed for a particular data bit width in embedded applications. In addition, it is permissible to use 4 or 5 byte mode, even when only 3 byte mode is needed. It is permissible to use 5 byte mode, even when only 4 byte mode is needed.

The first and the last pixels of DE disable period are replaced with the special characters of K code on 8b/10b encoder to indicate byte boundary.

Table 2 Packer Mapping

Byte Mode	Framing Symbol	Condition			Packer Output
		DE	Enable	Disable	
3byte Mode	Byte 0	D[0]	Vsync: H \Rightarrow SYNH L \Rightarrow SYNL	Vsync: H \Rightarrow 0xFF L \Rightarrow 0x00	PD[0] PD[1] PD[2] PD[3] PD[4] PD[5] PD[6] PD[7]
		D[1]			
		D[2]			
		D[3]			
		D[4]			
		D[5]			
		D[6]			
		D[7]			
	Byte 1	D[8]	Hsync: H \Rightarrow SYNH L \Rightarrow SYNL	Hsync: H \Rightarrow 0xFF L \Rightarrow 0x00	PD[0] PD[1] PD[2] PD[3] PD[4] PD[5] PD[6] PD[7]
		D[9]			
		D[10]			
		D[11]			
		D[12]			
		D[13]			
		D[14]			
		D[15]			
4byte Mode	Byte 2	D[16]	BS	CTL[0]	PD[0] PD[1] PD[2] PD[3] PD[4] PD[5] PD[6] PD[7]
		D[17]		CTL[1]	
		D[18]		CTL[2]	
		D[19]		CTL[3]	
		D[20]		CTL[4]	
		D[21]		CTL[5]	
		D[22]		CTL[6]	
		D[23]		CTL[7]	
	Byte 3	D[24]	BS	CTL[8]	PD[0] PD[1] PD[2] PD[3] PD[4] PD[5] PD[6] PD[7]
		D[25]		CTL[9]	
		D[26]		CTL[10]	
		D[27]		CTL[11] *	
		D[28]		CTL[12]	
		D[29]		CTL[13]	
		D[30]		CTL[14]	
		D[31]		CTL[15]	
5byte Mode	Byte 4	D[32]	BS	CTL[16]	PD[0] PD[1] PD[2] PD[3] PD[4] PD[5] PD[6] PD[7]
		D[33]		CTL[17]	
		D[34]		CTL[18]	
		D[35]		CTL[19]	
		D[36]		CTL[20]	
		D[37]		CTL[21]	
		D[38]		CTL[22]	
		D[39]		CTL[23]	
	-	-	D	K	D/K

*Implementation specific

From PD data and D/K identification signal from 8b/10b decoder, the unpacker generates the D data, CTL data, and sync signal.

Table 3 Unpacker Mapping

Byte Mode	Framing Symbol	Unpacker Input		Condition		
		-	D/K	FSACTIVE	FSBS	FSBP
3byte Mode	Byte 0	PD[0]	D[0]	Vsync: SYNH → H SYNL → L	D	K
		PD[1]	D[1]			
		PD[2]	D[2]			
		PD[3]	D[3]			
		PD[4]	D[4]			
		PD[5]	D[5]			
		PD[6]	D[6]			
		PD[7]	D[7]			
	Byte 1	PD[0]	D[8]	Hsync: SYNH → H SYNL → L	Vsync: 0xFF → H 0x00 → L	Hsync: SYNH → H SYNL → L
		PD[1]	D[9]			
		PD[2]	D[10]			
		PD[3]	D[11]			
		PD[4]	D[12]			
		PD[5]	D[13]			
		PD[6]	D[14]			
		PD[7]	D[15]			
4byte Mode	Byte 2	PD[0]	D[16]	(BS)**	CTL[0]	
		PD[1]	D[17]		CTL[1]	
		PD[2]	D[18]		CTL[2]	
		PD[3]	D[19]		CTL[3]	
		PD[4]	D[20]		CTL[4]	
		PD[5]	D[21]		CTL[5]	
		PD[6]	D[22]		CTL[6]	
		PD[7]	D[23]		CTL[7]	
	Byte 3	PD[0]	D[24]	(BS)**	CTL[8]	
		PD[1]	D[25]		CTL[9]	
		PD[2]	D[26]		CTL[10]	
		PD[3]	D[27]		CTL[11]	*
		PD[4]	D[28]		CTL[12]	
		PD[5]	D[29]		CTL[13]	
		PD[6]	D[30]		CTL[14]	
		PD[7]	D[31]		CTL[15]	
5byte Mode	Byte 4	PD[0]	D[32]	(BS)**	CTL[16]	
		PD[1]	D[33]		CTL[17]	
		PD[2]	D[34]		CTL[18]	
		PD[3]	D[35]		CTL[19]	
		PD[4]	D[36]		CTL[20]	
		PD[5]	D[37]		CTL[21]	
		PD[6]	D[38]		CTL[22]	
		PD[7]	D[39]		CTL[23]	
	DE	-	Enable		Disable	

* Implementation specific

** Implementation specific

The FSACTIVE symbol period includes D[39:0]. FSBP is able to include CTL[23:0].

2.1.2. Scrambler and Descrambler

The data scrambling is adopted for EMI reduction prior to ANSI 8b/10b encoding on the transmitter.

Each of main link data are scrambled and descrambled independently, with a 16-bit LFSR as follows:

$$\text{LFSR : } G(X) = X^{16} + X^5 + X^4 + X^3 + 1$$

LFSR shifts 8bits for 1 byte character (both D-code and K-code). The BE_SR character is used to reset the LFSR to FFFFh. The data scrambling rules is as follows:

- Special characters (BS, BE, BE_SR, SYNL, and SYNH) are not scrambled.
- All data inside FSACTIVE and FSBP symbols are scrambled

Note that the scrambling must be disabled during the CDR training.

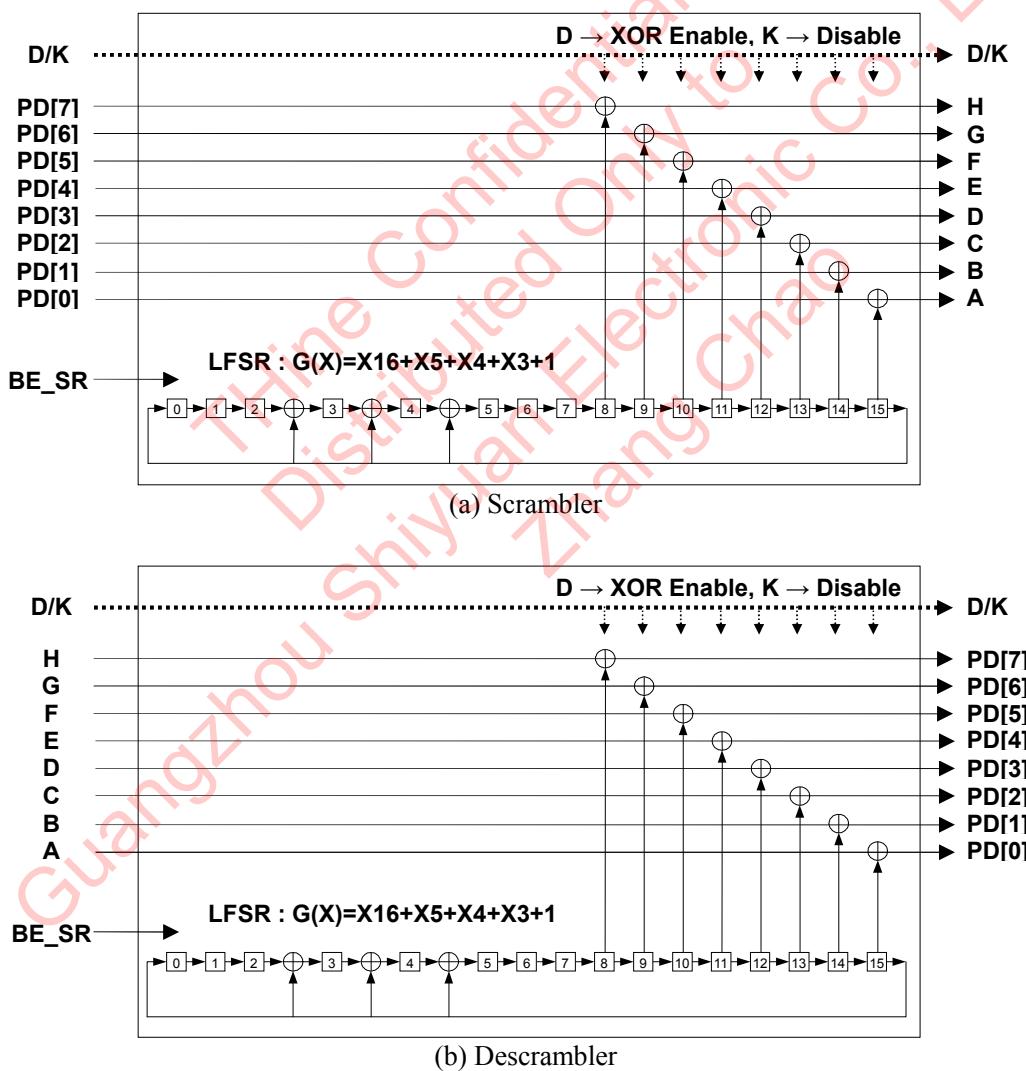


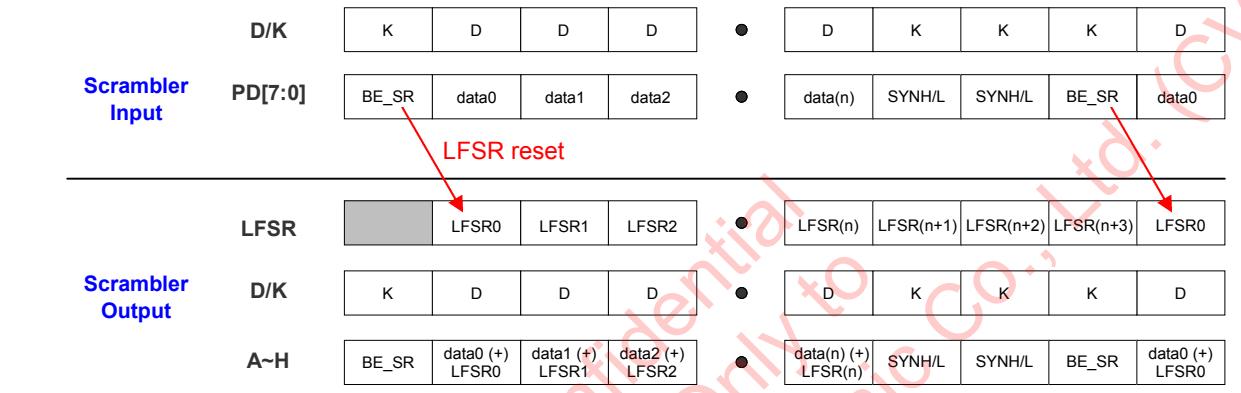
Figure 8 Scrambler and Descrambler

2.1.2.1. Time Chart

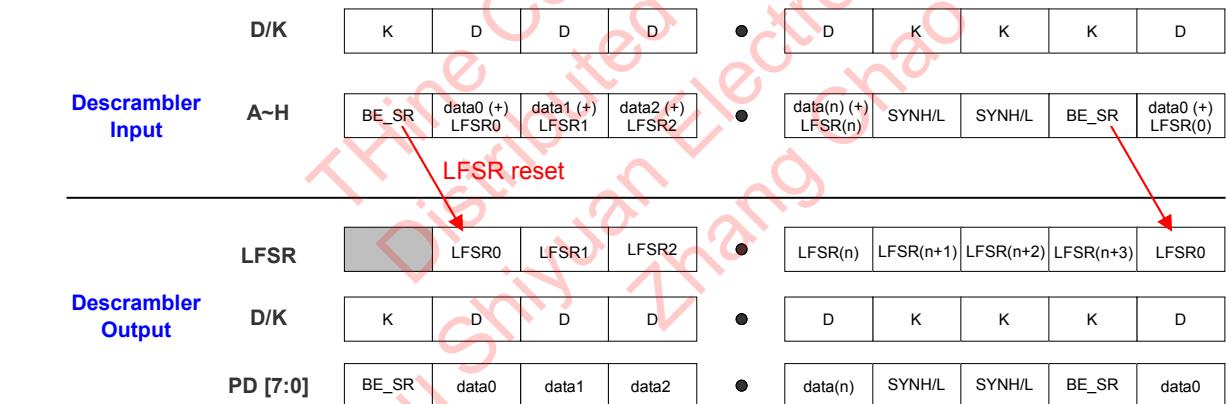
The LFSR reset timing is shown in Figure 9. The LFSR is reset to FFFFh by BE_SR character, and the reset data is applied from the next data.

Figure 9 shows the timing diagram of the LFSR operation including reset.

Tx



Rx

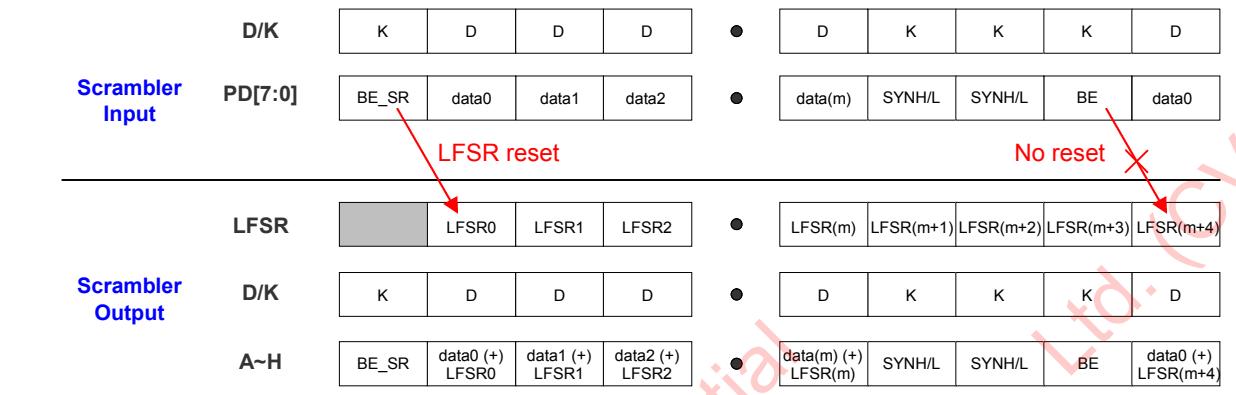


(+) means XOR operation

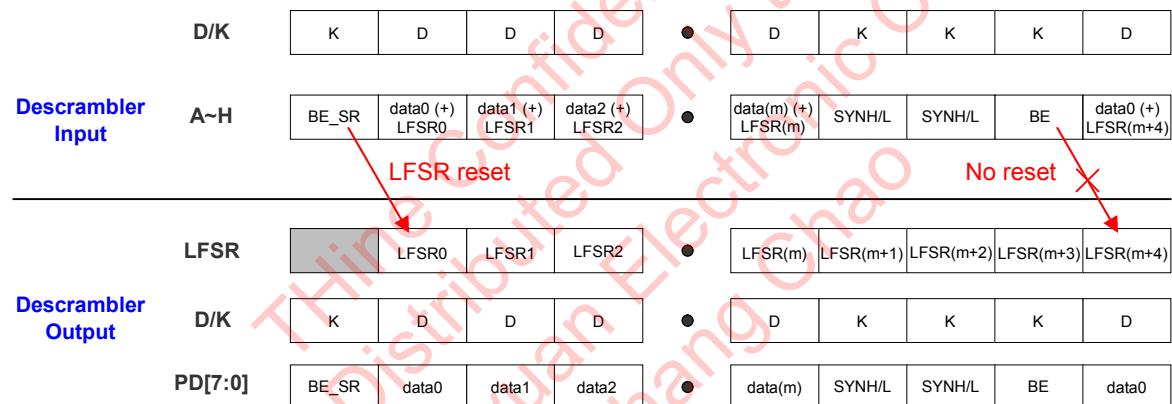
Figure 9 Scrambler and Descrambler Timing Chart with BE_SR (3byte mode)

Please be careful that LFSR does not reset a counter with BE character. See below figure.

Tx



Rx



(+) means XOR operation

Figure 10 Scrambler and Descrambler Timing Chart with BE (3byte mode)

2.1.3. Encoder and Decoder

The encoder and decoder are ANSI standard 8b/10b compatible. On normal mode operation, each 10bit character represents 8bit of pixel data (Figure 11). Encoded characters provide DC balance and sufficient 0-1 and 1-0 transitions in V-by-One® HS stream, which enable the receiver to recover link clock with CDR technology.

FSBS, FSBE, and FSBE_SR framing symbols consist of K codes, while FSBP framing symbol consists of scrambled D codes. FSBS framing symbol consists of BS, SYNH, or SYNL character, while FSBE symbol contains BE or BE_SR character in addition to SYNH or SYNL character. Special characters such as SYNH, SYNL, BS, BE and BE_SR are described in the table below. BS and SYNL are assigned the same code. BS, SYNH, and SYNL codes are so-called COMMA. They are used for detecting the byte boundary.

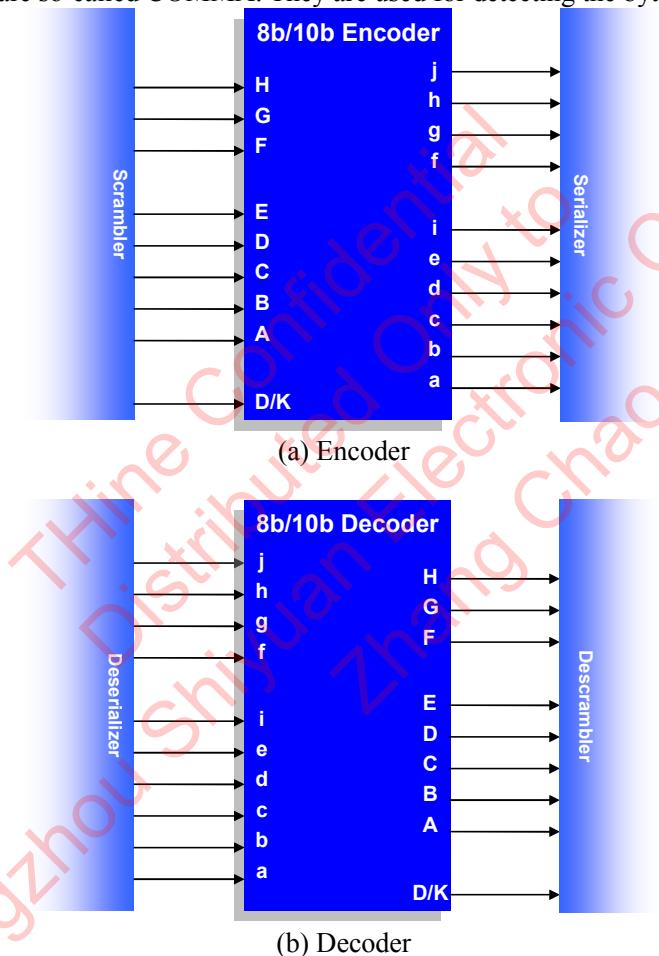


Figure 11 8b/10b Encoder and Decoder

Table 4 ANSI 8b/10b Special Characters for V-by-One® HS

Character	Code Name
BE_SR	K28.0
BS/SYNL	K28.1
BE	K28.2
SYNH	K28.5

2.1.4. Serializer and Deserializer

After 8b/10b encode, 10bit data is serialized (Figure 12).

The order of the data is shown in Figure 13.

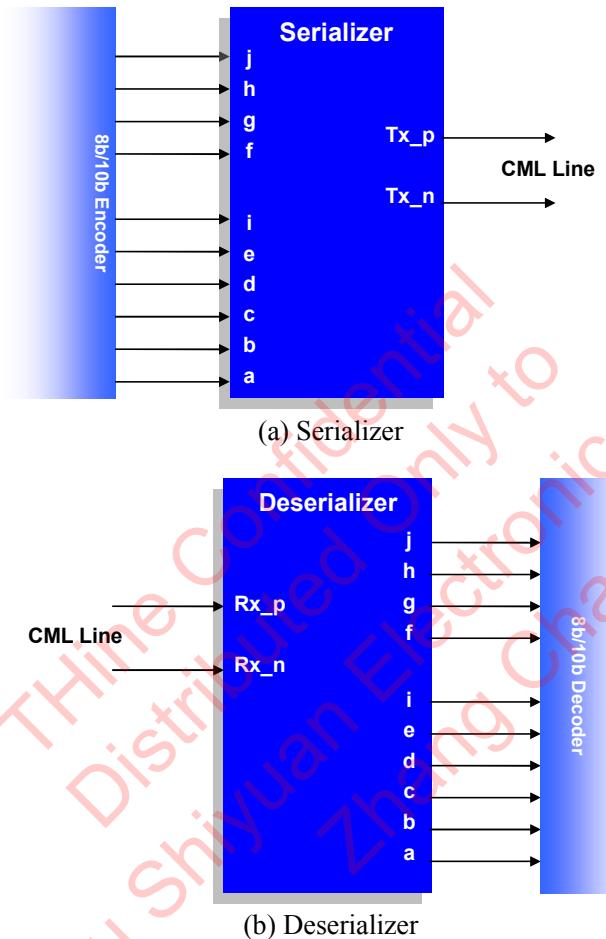


Figure 12 Serializer and Deserializer Interface

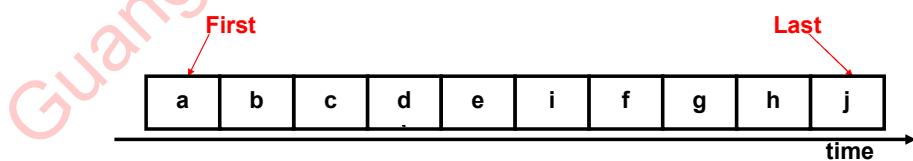


Figure 13 Timing Diagram of the Serializer

2.1.5. Link Status Monitor

Both LOCKN and HTPDN are open drain outputs from the receiver. Pull-up resistors are needed at the transmitter side. The value of the pull-up resistors is 10kΩ.

If the receiver is not active (e.g. power down mode or power off), HTPDN is open. Otherwise, HTPDN is pulled down to low by the receiver. HTPDN of the transmitter side is high when the receiver is not active or the receiver board is not connected. Then transmitter enters into the power down mode. When HTPDN transits from high to low, transmitter starts transmitting the training pattern for the link training.

HTPDN connection between the transmitter and the receiver can be omitted as an application option. In this case, HTPDN at the transmitter side is supposed be taken as low; therefore, the transmitter always start training pattern when the transmitter is active and LOCKN is high.

LOCKN indicates whether the receiver is at the lock state on the CDR sequence. If the receiver is in the unlock state, LOCKN is open. Otherwise (in the lock state), it's pulled down to low by the receiver. The transmitter keeps transmitting the training pattern until LOCKN becomes low. After training is done, the receiver drives LOCKN to low. Then transmitter starts transmitting ALN training pattern and normal video pattern.

2.2. Operating Specification

2.2.1. Transmitter State Diagram

Figure 14 shows the state machine of the transmitter's behavior.

The output from transmitter is listed in Table 5.

The diagram in this chapter is informative. Actual state machine of the transmitter may be not the same as this figure strictly.

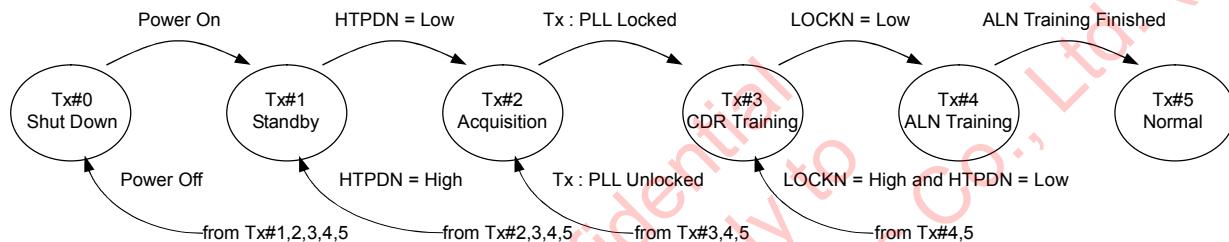


Figure 14 Transmitter State Diagram

Table 5 Detail of Each State

State	Comment	Tx Output
Tx#0 : Shut Down	Power Off	*
Tx#1 : Standby	Power On	**
Tx#2 : Acquisition	Acquisition of the Input Pixel Clock from User Logic	**
Tx#3 : Transmit CDR Training	Output CDR Training Pattern	CDR Training Pattern
Tx#4 : Transmit ALN Training	Output Alignment Training Pattern	ALN Training Pattern
Tx#5 : Transmit Normal	Output Normal Pattern	Normal Pattern

*The output from transmitter at the state of Tx#0 is implementation specific.

**The output from transmitter at the state of Tx#1, 2 should be fixed to some voltage level in order to avoid undesired output under transmitter PLL unstable condition.

2.2.2. Receiver State Diagram

The diagram in this chapter is informative. Actual state machine of the receiver may not be the same as this figure strictly.

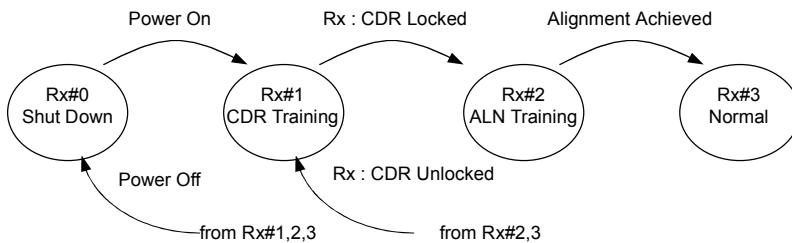


Figure 15 Receiver State Diagram

Table 6 Detail of Receiver State

State	Comment	Rx Output	HTPDN	LOCKN
Rx#0 : Shut Down	Shut Down	Invalid	High	High
Rx#1 : CDR Training	CDR Locking Process	Invalid	Low	High
Rx#2 : ALN Training	Training by Alignment Logic	Invalid	Low	Low
Rx#3 : Normal	Normal Operation	Valid	Low	Low

2.2.3. Link Start up Flow

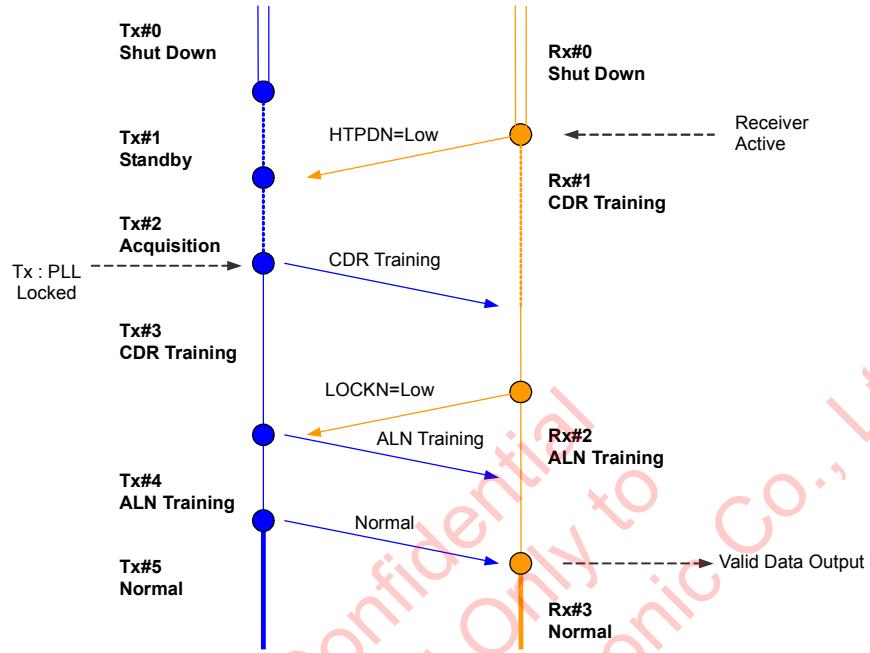


Figure 16 V-by-One[®] HS Link Start up Flow

2.2.4. Link Disable Flow

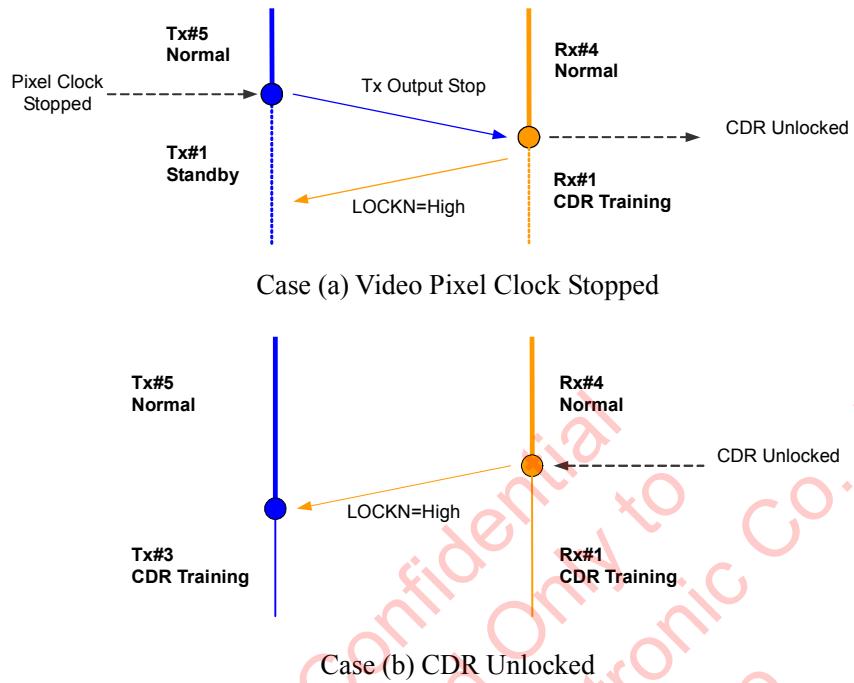


Figure 17 V-by-One® HS Link Disable Flow

2.2.5. Trainings

2.2.5.1. CDR Training

CDR training is performed for frequency acquisition of CDR PLL. CDR training conditions are as follows;

- CDR training is performed when the transmitter side HTPDN=low, and LOCKN=high.
- Transmitter transmits repetition of D10.2 (0101010101) code until frequency lock of CDR PLL.
- Training pattern (D10.2) frequency is equal to half of the V-by-One[®] HS link bit rate.
- D10.2 code must not be scrambled.
- When receiver loses CDR lock, it can indicate the status to transmitter by LOCKN=high.

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2.2.5.2. ALN Training

“ALN” stands for alignment. ALN training is performed for both byte alignment and pixel alignment. For these purpose, ALN pattern includes BS and BE character.

Byte boundary is detected with COMMA pattern embedded in BS and BE characters. Symbol boundary is detected from K boundaries.

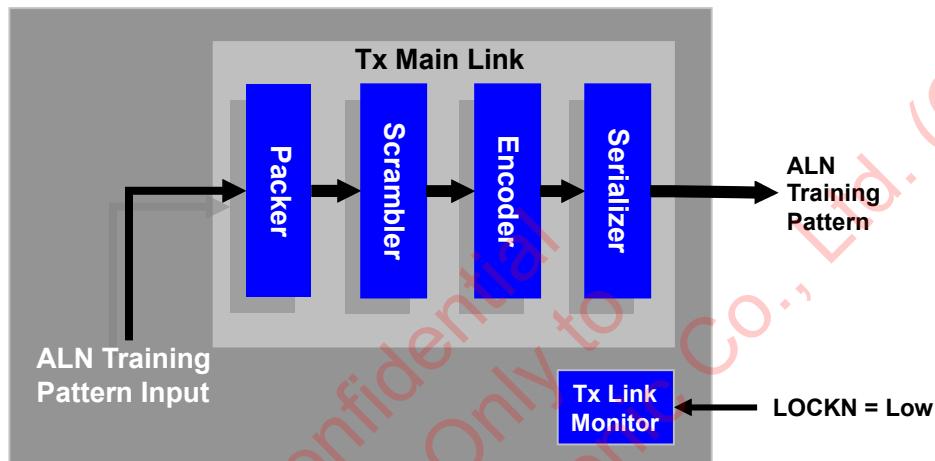


Figure 18 ALN Training Overview

ALN training conditions are as follows;

- ALN training starts when HTPDN and LOCKN at the transmitter input are low.
- One DE cycle consists of 64 pixels. The first 32 pixels are high and the last 32 pixels are low.
- DE cycle is repeated 16 times within ALN training.
- D[39:0], Hsync, and CTL[23:0] packets are kept to “0” during ALN training after LOCKN is set to “0”.
- DE at the last one pixel is set to “1”.
- In order to replace the BE character with BE_SR, 1 pixel cycle of Vsync should be set to “1”, the other pixels should be set to “0”.
- This 1 pixel cycle of Vsync should be set within the last 32 pixel counts of ALN training except for the 1st, 30th, 31st and 32nd pixel cycle. The detail of Vsync = “1” timing is shown in Figure 20.
- The ALN training pattern is scrambled by the scrambler.

ALN training timing details are shown in Figure 19.

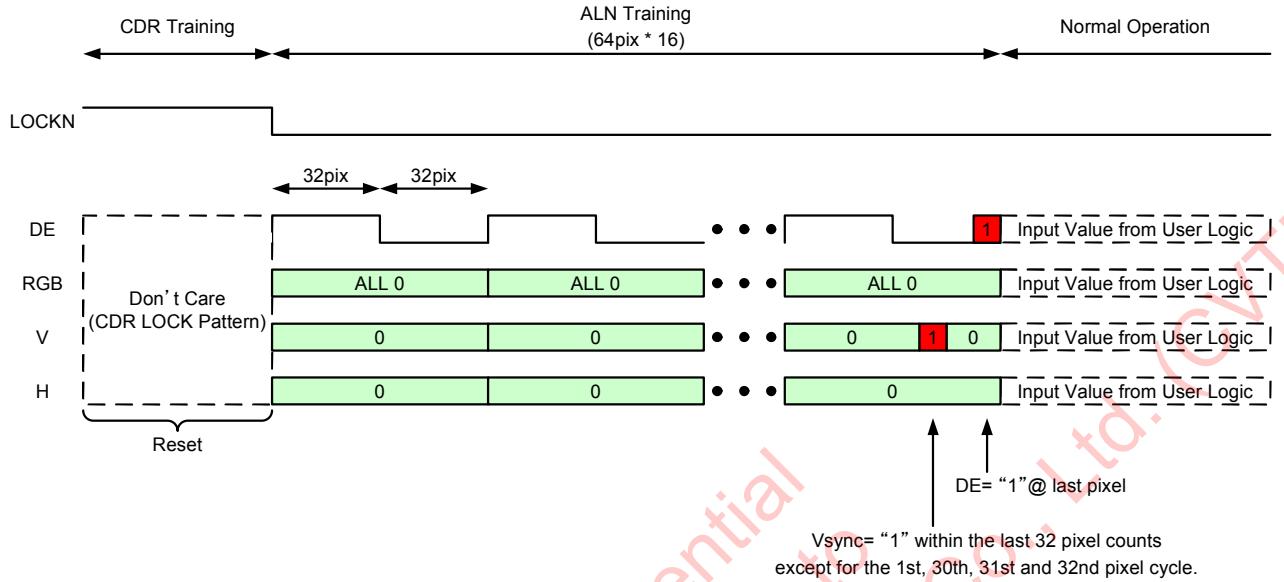


Figure 19 ALN Training Timing

The last ALN training cycle has different pattern that includes BE_SR character for scrambler reset.

Total ALN training period is always 64*16 pixels per lane that is independent of lane count of application.

ALN training example of packer output at 3byte mode is shown in Figure 20.

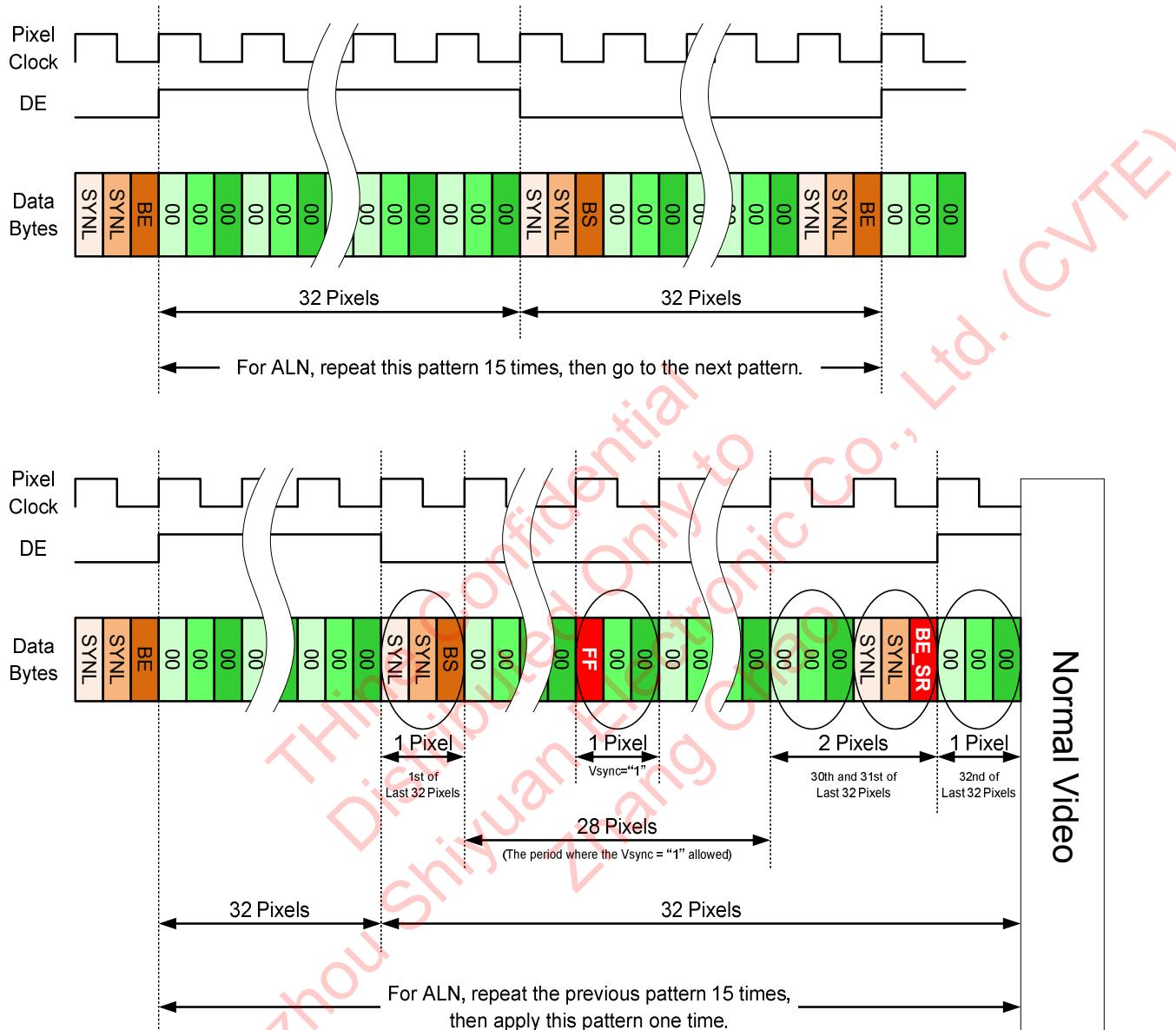


Figure 20 Packer Output Sequence of ALN Training (3byte mode)

2.2.5.3. Re-entry to Training Mode

In case that transmitter changes the data rate, transmitter should stop outputting signal firstly in order to make the receiver enter the training mode. After the receiver enter the training mode (LOCKN becomes high), then transmitter starts the transmission of the training signals (Figure 17(a)).

When receiver loses the link connection by some reasons (CDR failure etc.), receiver indicate the situation to the transmitter by setting LOCKN as high (Figure 17(b)).

3. Electrical Specification

3.1. Overview

Figure 21 shows the V-by-One® HS CML connection. Transmitter and receiver are connected by AC-coupled differential transmission line.

By the AC-coupling capacitor, transmitter and receiver can choose the supply and bias voltage suitable for their design and process technology.

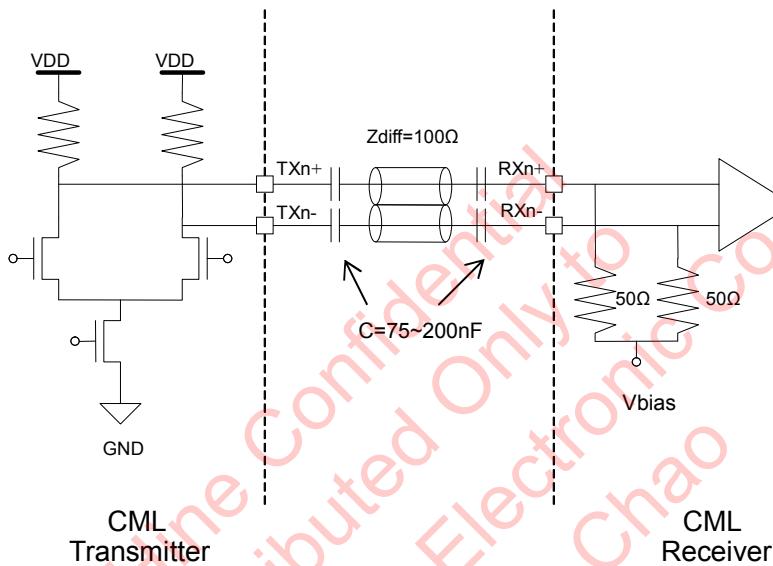


Figure 21 CML Transmitter and Receiver Configuration

The AC-coupling capacitor is placed on both ends of CML line in Figure 21. To use on both ends or on one side is implementation specific. When it is used only at one side, the transmitter side capacitor must be used.

3.2. Transmitter Electrical Specifications

The data link of the V-by-One® HS interface requires an AC-coupled link. The electrical test of the transmitter is performed using the test load shown in Figure 22.

Table 7 is the DC specifications of the transmitter. The VTOD parameter identifies the minimum and maximum single-ended peak-to-peak signal amplitude that may be delivered by transmitter into the test load. The VTOC parameter identifies common mode voltage.

Table 7 Transmitter DC Characteristics at TP

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VTOD	CML Differential Mode Output Voltage	*w/o Pre-emphasis	200	300	400	mV
*PRE	CML Pre-emphasis Level	-		Implementation Specific		%
VTOC	CML Common Mode Output Voltage	-		Implementation Specific		mV
VDL	Pull-up Voltage	For LOCKN and HTPDN Pin	1.08	-	3.6	V
VIH	High Level Input Voltage		0.7VDL	-	VDL	V
VIL	Low Level Input Voltage		0	-	0.35	V
IIH	Input Leak Current at Input = VDL		-10	-	10	uA
IIL	Input Leak Current at Input = 0		-10	-	10	uA

*Pre-emphasis is optional function. Pre-emphasis level and time is implementation specific.

Table 8 is the AC specifications of the transmitter. Rise and fall times are defined as the signal transition time between 20% and 80% of the nominal swing voltage (VTOD) of the device under test.

The intra-pair skew is the time difference between the true and complementary single-ended signals as shown in Figure 22 (b). The inter-pair skew is the time difference of the differential voltage between any two lanes in Figure 22 (c). These characteristics are measured at TP in Figure 22 (a) on both Low-to-High and High-to-Low transitions.

For all lanes, the differential voltage from the transmitter must be complied with the Eye diagram of Figure 23 at the TP point of Figure 22.

For the spread spectrum tolerance with lower jitter level, transmitter must have the upper limitation of its PLL loop bandwidth as shown in Figure 24. The maximum amplitude of Spread Spectrum(SS) is limited to 0.5% center spread at the 30kHz modulation frequency.

Eye diagram measurement of Figure 23 is supposed to be held by using constant frequency which is an averaged frequency in one acquisition time. Specific memory depth for one acquisition is supposed to be set so that one acquisition time around trigger is the period length of transmitter PLL bandwidth defined in Figure 24. For example, 3MHz bandwidth requires 333ns acquisition time length because transmitter PLL allows slower frequency shift than 3MHz; therefore, those slow frequency shift phenomena under long acquisition condition has no need to be focused on.

Table 8 Transmitter AC Characteristics at TP

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
tTBIT *	Unit Interval	3byte mode	266	tTCIP/30 **	1667	ps
		4byte mode	266	tTCIP/40	1667	ps
		5byte mode	266	tTCIP/50	1667	ps
tTRF	CML Output Rise and Fall Time (20-80%)	-	50	-	150	ps
tTOSK_INTRA	CML Output Intra-pair Skew	tTBIT= 333ps	-	20	60	ps
		tTBIT= 266ps	-	20	40	ps
tTOSK_INTER	CML Output Inter-pair Skew	-	-	-	2	UI
-	CML Jitter	-	-	-	0.3	UIp-p
-	Spread Spectrum Amplitude	30kHz modulation	-0.5	-	0.5	%

* The specification of tTBIT is defined only as the operation limitation. The transmitter only required its operation range inside this specification. Full frequency range support is not required in the V-by-One® HS standard because most devices are used at the fixed data rate in the embedded applications. Also full byte mode support does not have to be required with the similar reason.

** tTCIP is the pixel data unit time per lane

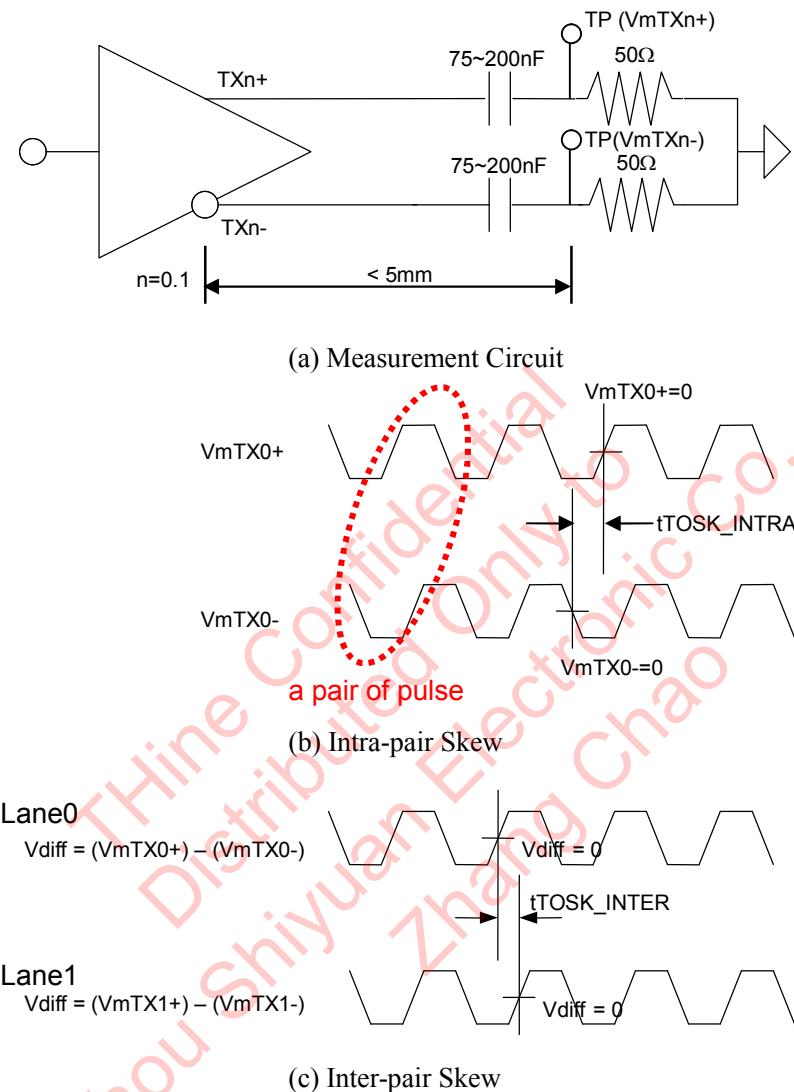


Figure 22 CML Test Circuit and Output AC Timing Diagrams

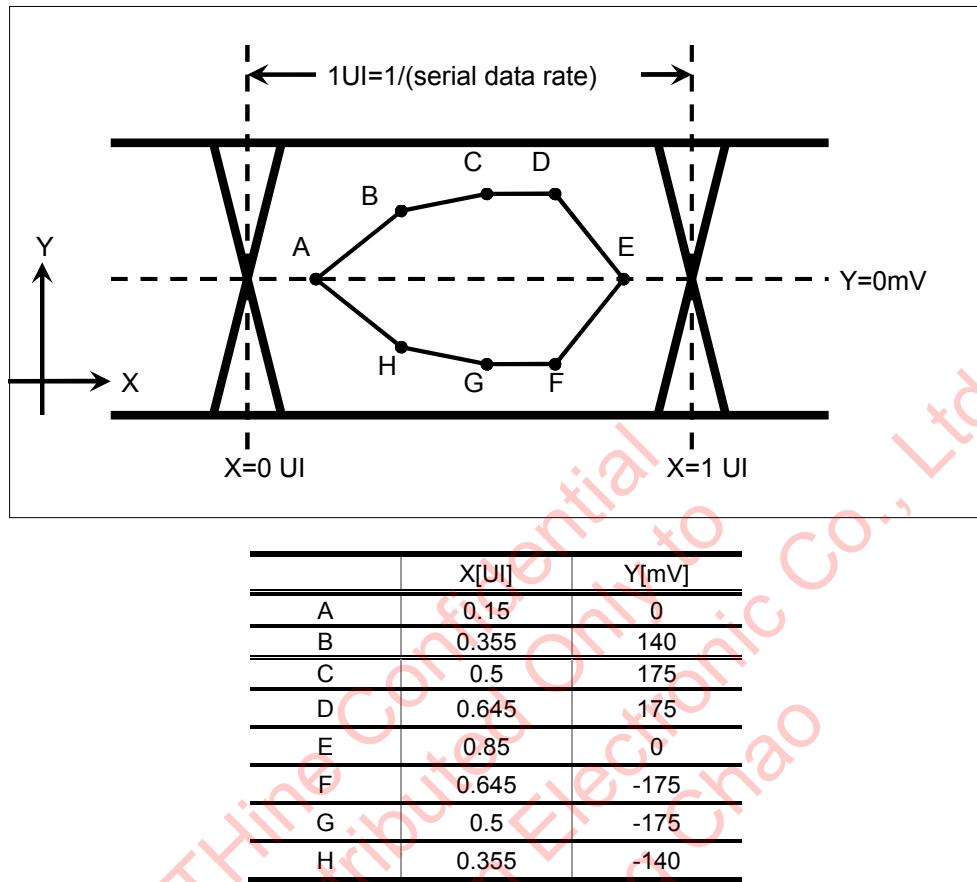


Figure 23 Eye Diagram at Transmitter

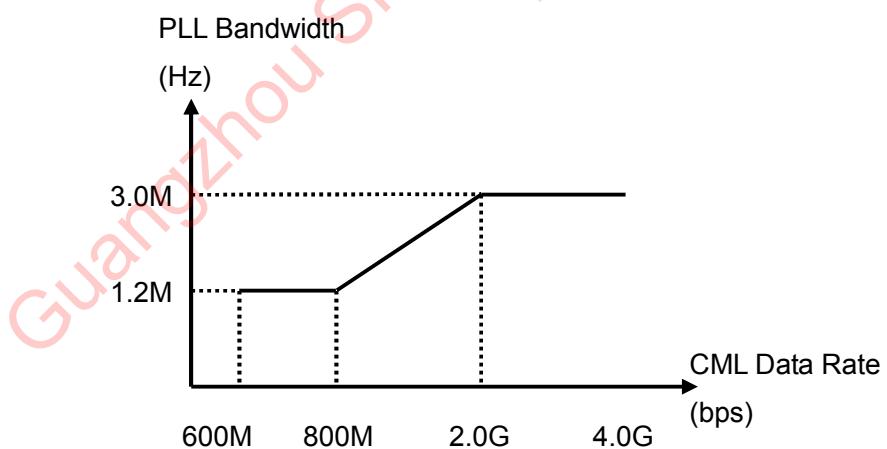


Figure 24 PLL Bandwidth of V-by-One[®] HS Transmitter

3.3. Receiver Electrical Specifications

The receiver must meet the signal requirement listed in Table 9 and Table 10

For the stable connection between transmitter and receiver, the PLL bandwidth of the receiver must be set properly to handle the CML signal from the transmitter which has the PLL bandwidth of Figure 24.

Table 9 Receiver DC Characteristics at Receiver Pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VRTH	CML Differential Input High Threshold	-	-	-	50	mV
VRTL	CML Differential Input Low Threshold	-	-50	-	-	mV
VRCT	CML Common mode Bias Voltage	-		Implementation Specific		V
RRIN	CML Differential Input Resistance	-	80	100	120	Ω
VDL	Pull-up Voltage		1.08	-	3.6	V
IOZ	Output Leak Current at Pin = VDL or GND	For LOCKN and HTPDN Pin	-10	-	10	uA
VOL	Low Level Output Voltage at IOL=2mA		-	-	0.2	V

Table 10 Receiver AC Characteristic at Receiver Pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
tRBIT *	Unit Interval	3byte Mode	266	tTCIP/30	1667	ps
		4byte Mode	266	tTCIP/40	1667	ps
		5byte Mode	266	tTCIP/50	1667	ps
tRISK_INTRA	Allowable Intra-pair Skew	-	0.3	-	-	UI
tRISK_INTER	Allowable Inter-pair Skew	-	5	-	-	UI
-	Loop Bandwidth	-		Implementation Specific		-

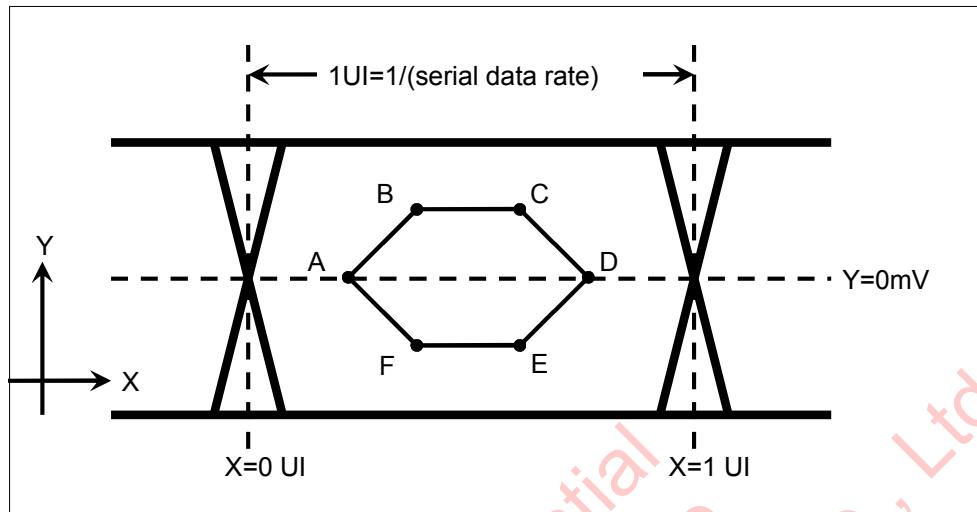
* The specification of tRBIT is defined only as the operation limitation. The receiver only required its operation range inside this specification. Full frequency range support is not required in the V-by-One® HS standard because most devices are used at the fixed data rate in the embedded applications, same as the transmitter. Full byte mode support does not have to be required, also same as the transmitter.

** tTCIP is the pixel data unit time per lane

Receiver should reproduce the data stream with pixel error rate 1e-9, when tested with the input signal illustrated by the eye diagram of Figure 25 at the receiver IC pins.

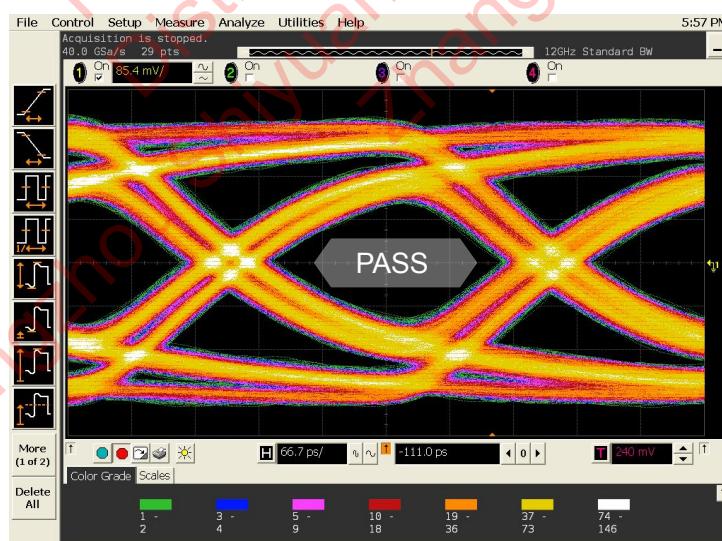
If receiver IC pin is not accessible, receiver must be evaluated at carefully chosen equivalent test point near IC. Use of transmitter pre-emphasis and receiver equalizer is up to situations under the same Eye-Mask criteria.

The definition of the receiver's intra-pair skew and inter-pair skew is the same as that of transmitter.



	X[UI]	Y[mV]
A	0.25	0
B	0.3	50
C	0.7	50
D	0.75	0
E	0.7	-50
F	0.3	-50

(a) Eye Mask



(b) Example of Eye Diagram

Figure 25 Eye Diagram at Receiver

3.4. Eye Diagram Measurement Setting

The eye diagram is measured by the oscilloscope and receiver CDR characteristics must be emulated.

At the condition when the spread spectrum is enabled or when low-frequency jitter exists, the eye opening measured may become narrower, if the CDR of the oscilloscope does not track such kind of frequency variations. In order to avoid this issue, this standard defines basic setting reference of the oscilloscope that the CDR of the oscilloscope is enabled with the loop bandwidth as shown in Figure 26, which is an example of receiver application having enough margins from transmitter bandwidth. It may be different according to the actual receiver implementation; therefore, if actual receiver application characteristics are clear, actual specifications should be taken into account prior to the reference.

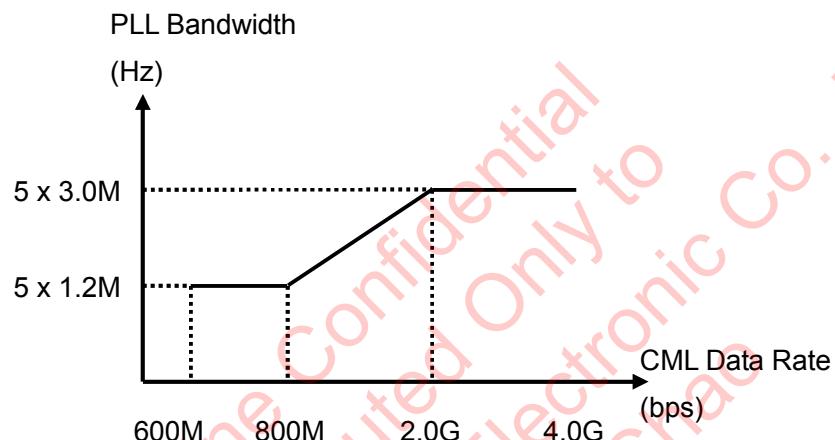


Figure 26 Oscilloscope Loop Bandwidth

3.5. Power on/off and Power Down Specification

The V-by-One® HS CML is AC-coupled between transmitter and receiver. Thus, there is a possibility to make damage by the coupling voltage when each of them is powered on and off. To avoid this kind of damage, the power supply time should be slower than 1msec (Soft start).

Similarly, when it enters and exits standby, acquisition described in Table 5 or power down state, the common mode voltage may vary on either side of transmitter or receiver (VTOD in Table 7 and VRCT in Table 9). The amount of voltage change at those occasions must be lower than the VTOD in Table 7.

3.6. Optional Functions

3.6.1. Pre-emphasis

Supporting pre-emphasis is the implementation specific feature for the transmitter.

3.6.2. Equalizer

Supporting equalizer is the implementation specific feature for the receiver.

4. Guideline for Interoperability

In this chapter, guideline for interoperability is described.

4.1. Byte length and Color Mapping

The V-by-One® HS can be used to various types of color video format allocating D[39:0] to pixel data in packer and unpacker mapping. The color data mapping should refer to Table 11 and Table 12

Table 11 RGB/YCbCr444/RGBW/RGBY Color Data Mapping

Mode		Packer Input & Unpacker Output	36bpp RGB /YCbCr444	30bpp RGB /YCbCr444	24bpp RGB /YCbCr444	18bpp RGB /YCbCr444	40bpp RGBW /RGBY	32bpp RGBW /RGBY
3byte Mode	Byte0	D[0]	R/Cr[4]	R/Cr[2]	R/Cr[0]	-	R[2]	R[0]
		D[1]	R/Cr[5]	R/Cr[3]	R/Cr[1]	-	R[3]	R[1]
		D[2]	R/Cr[6]	R/Cr[4]	R/Cr[2]	R/Cr[0]	R[4]	R[2]
		D[3]	R/Cr[7]	R/Cr[5]	R/Cr[3]	R/Cr[1]	R[5]	R[3]
		D[4]	R/Cr[8]	R/Cr[6]	R/Cr[4]	R/Cr[2]	R[6]	R[4]
		D[5]	R/Cr[9]	R/Cr[7]	R/Cr[5]	R/Cr[3]	R[7]	R[5]
		D[6]	R/Cr[10]	R/Cr[8]	R/Cr[6]	R/Cr[4]	R[8]	R[6]
		D[7]	R/Cr[11]	R/Cr[9]	R/Cr[7]	R/Cr[5]	R[9]	R[7]
	Byte1	D[8]	G/Y[4]	G/Y[2]	G/Y[0]	-	G[2]	G[0]
		D[9]	G/Y[5]	G/Y[3]	G/Y[1]	-	G[3]	G[1]
		D[10]	G/Y[6]	G/Y[4]	G/Y[2]	G/Y[0]	G[4]	G[2]
		D[11]	G/Y[7]	G/Y[5]	G/Y[3]	G/Y[1]	G[5]	G[3]
		D[12]	G/Y[8]	G/Y[6]	G/Y[4]	G/Y[2]	G[6]	G[4]
		D[13]	G/Y[9]	G/Y[7]	G/Y[5]	G/Y[3]	G[7]	G[5]
		D[14]	G/Y[10]	G/Y[8]	G/Y[6]	G/Y[4]	G[8]	G[6]
		D[15]	G/Y[11]	G/Y[9]	G/Y[7]	G/Y[5]	G[9]	G[7]
4byte Mode	Byte2	D[16]	B/Cb[4]	B/Cb[2]	B/Cb[0]	-	B[2]	B[0]
		D[17]	B/Cb[5]	B/Cb[3]	B/Cb[1]	-	B[3]	B[1]
		D[18]	B/Cb[6]	B/Cb[4]	B/Cb[2]	B/Cb[0]	B[4]	B[2]
		D[19]	B/Cb[7]	B/Cb[5]	B/Cb[3]	B/Cb[1]	B[5]	B[3]
		D[20]	B/Cb[8]	B/Cb[6]	B/Cb[4]	B/Cb[2]	B[6]	B[4]
		D[21]	B/Cb[9]	B/Cb[7]	B/Cb[5]	B/Cb[3]	B[7]	B[5]
		D[22]	B/Cb[10]	B/Cb[8]	B/Cb[6]	B/Cb[4]	B[8]	B[6]
		D[23]	B/Cb[11]	B/Cb[9]	B/Cb[7]	B/Cb[5]	B[9]	B[7]
	Byte3	D[24]	(3DLR*)	(3DLR*)	-	-	R[0]	-
		D[25]	(3DEN*)	(3DEN*)	-	-	R[1]	-
		D[26]	B/Cb[2]	B/Cb[0]	-	-	G[0]	-
		D[27]	B/Cb[3]	B/Cb[1]	-	-	G[1]	-
		D[28]	G/Y[2]	G/Y[0]	-	-	B[0]	-
		D[29]	G/Y[3]	G/Y[1]	-	-	B[1]	-
		D[30]	R/Cr[2]	R/Cr[0]	-	-	W/Y[0]	-
		D[31]	R/Cr[3]	R/Cr[1]	-	-	W/Y[1]	-
5byte Mode	Byte4	D[32]	-	-	-	-	W/Y[2]	W/Y[0]
		D[33]	-	-	-	-	W/Y[3]	W/Y[1]
		D[34]	B/Cb[0]	-	-	-	W/Y[4]	W/Y[2]
		D[35]	B/Cb[1]	-	-	-	W/Y[5]	W/Y[3]
		D[36]	G/Y[0]	-	-	-	W/Y[6]	W/Y[4]
		D[37]	G/Y[1]	-	-	-	W/Y[7]	W/Y[5]
		D[38]	R/Cr[0]	-	-	-	W/Y[8]	W/Y[6]
		D[39]	R/Cr[1]	-	-	-	W/Y[9]	W/Y[7]

* Implementation specific

Table 12 YCbCr422 Color Data Mapping

Mode		Packer Input & Unpacker Output	32bpp YCbCr422	24bpp YCbCr422	20bpp YCbCr422	16bpp YCbCr422
5byte Mode	Byte0	D[0]	Cb/Cr[8]	Cb/Cr[4]	Cb/Cr[2]	Cb/Cr[0]
		D[1]	Cb/Cr[9]	Cb/Cr[5]	Cb/Cr[3]	Cb/Cr[1]
		D[2]	Cb/Cr[10]	Cb/Cr[6]	Cb/Cr[4]	Cb/Cr[2]
		D[3]	Cb/Cr[11]	Cb/Cr[7]	Cb/Cr[5]	Cb/Cr[3]
	Byte1	D[4]	Cb/Cr[12]	Cb/Cr[8]	Cb/Cr[6]	Cb/Cr[4]
		D[5]	Cb/Cr[13]	Cb/Cr[9]	Cb/Cr[7]	Cb/Cr[5]
		D[6]	Cb/Cr[14]	Cb/Cr[10]	Cb/Cr[8]	Cb/Cr[6]
		D[7]	Cb/Cr[15]	Cb/Cr[11]	Cb/Cr[9]	Cb/Cr[7]
	Byte2	D[8]	Y[8]	Y[4]	Y[2]	Y[0]
		D[9]	Y[9]	Y[5]	Y[3]	Y[1]
		D[10]	Y[10]	Y[6]	Y[4]	Y[2]
		D[11]	Y[11]	Y[7]	Y[5]	Y[3]
		D[12]	Y[12]	Y[8]	Y[6]	Y[4]
		D[13]	Y[13]	Y[9]	Y[7]	Y[5]
		D[14]	Y[14]	Y[10]	Y[8]	Y[6]
		D[15]	Y[15]	Y[11]	Y[9]	Y[7]
	Byte3	D[16]	-	-	-	-
		D[17]	-	-	-	-
		D[18]	-	-	-	-
		D[19]	-	-	-	-
		D[20]	-	-	-	-
		D[21]	-	-	-	-
		D[22]	-	-	-	-
		D[23]	-	-	-	-
	Byte4	D[24]	Y[2]	-	-	-
		D[25]	Y[3]	-	-	-
		D[26]	Cb/Cr[2]	-	-	-
		D[27]	Cb/Cr[3]	-	-	-
		D[28]	Y[6]	Y[2]	Y[0]	-
		D[29]	Y[7]	Y[3]	Y[1]	-
		D[30]	Cb/Cr[6]	Cb/Cr[2]	Cb/Cr[0]	-
		D[31]	Cb/Cr[7]	Cb/Cr[3]	Cb/Cr[1]	-
		D[32]	Y[0]	-	-	-
		D[33]	Y[1]	-	-	-
		D[34]	Cb/Cr[0]	-	-	-
		D[35]	Cb/Cr[1]	-	-	-
		D[36]	Y[4]	Y[0]	-	-
		D[37]	Y[5]	Y[1]	-	-
		D[38]	Cb/Cr[4]	Cb/Cr[0]	-	-
		D[39]	Cb/Cr[5]	Cb/Cr[1]	-	-

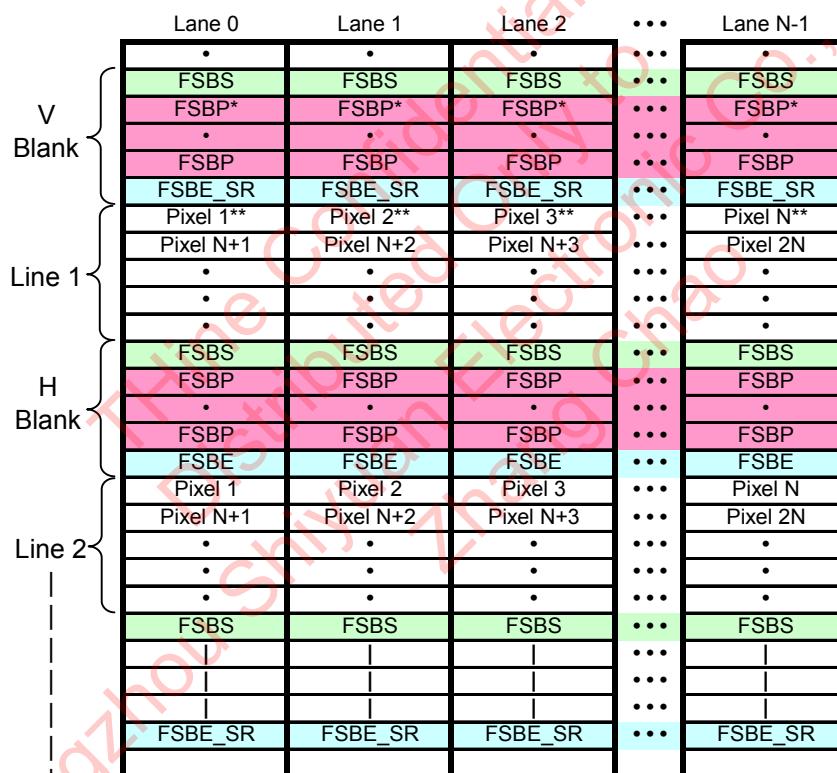
4.2. Multiple Data Lane Combination

4.2.1. Allocation of Pixel to Data Lane

Depend on the data rate and pixel color depth, it is permitted to increase the data lanes. About the multiple data lanes combination, refers to Figure 27 as first recommendation. For multiple device transmission, signal space can be divided into multiple sections vertically described in the following pages and figures.

The V-by-One® HS compliant components must be implemented with at least one data lane. If the data rate of the required color depth and timing is higher than the components maximum supported data rate, additional data lane can be used. (The maximum data rate of V-by-One® HS data lane is 4Gbps per lane and the minimum is 600Mbps.) In this case, total lane count should be even number, under the condition of the fewer lane number.

The pixel number for the horizontal active and blanking term (Hactive, Hblank) should be adjusted to become the multiple number of the lane count.



* The 1st pixel of each lane FSBP in vertical blanking period may convey 3D flag of next frame with particular assigned CTL bit

** The 1st pixel of each lane in a frame may convey 3D flag of current frame with particular assigned bit 3DLR and 3DEN

Figure 27 Allocation of Pixel to Data Lane

	Lane 0	Lane 1	...	Lane N/M-1	Lane N/M	Lane N/M+1	...	Lane N-1
V Blank	•	•	...	•	•	•	...	•
Line 1	FSBS	FSBS	...	FSBP*	FSBP*	FSBP*	...	FSBP*
	FSBP	FSBP	...	•	•	•	...	FSBP
	FSBE_SR	FSBE_SR	...	FSBE_SR	FSBE_SR	FSBE_SR	...	FSBE_SR
	Pixel 1**	Pixel 2**	...	Pixel N/M**	Pixel H/M+1**	Pixel H/M+2**	...	Pixel (M-1)H/M+N/M**
	Pixel N/M+1	Pixel N/M+2	...	Pixel 2N/M	Pixel H/M+N/M+1	Pixel H/M+N/M+2	...	Pixel (M-1)H/M+2N/M
Line 2	•	•	...	•	•	•	...	•
	FSBS	FSBS	...	FSBS	FSBS	FSBS	...	FSBS
	FSBP	FSBP	...	FSBP	FSBP	FSBP	...	FSBP
	•	•	...	•	•	•	...	FSBP
	FSBE	FSBE	...	FSBE	FSBE	FSBE	...	FSBE
	Pixel 1	Pixel 2	...	Pixel N/M	Pixel H/M+1	Pixel H/M+2	...	Pixel (M-1)H/M+N/M
	Pixel N/M+1	Pixel N/M+2	...	Pixel 2N/M	Pixel H/M+N/M+1	Pixel H/M+N/M+2	...	Pixel (M-1)H/M+2N/M
	•	•	...	•	•	•	...	•
	FSBS	FSBS	...	FSBS	FSBS	FSBS	...	FSBS
	•	•	...	•	•	•	...	•
	FSBE_SR	FSBE_SR	...	FSBE_SR	FSBE_SR	FSBE_SR	...	FSBE_SR

* The 1st pixel of each lane FSBP in vertical blanking period may convey 3D flag of next frame with particular assigned CTL bit

** The 1st pixel of each lane in a frame may convey 3D flag of current frame with particular assigned bit 3DLR and 3DEN

Figure 28 N Lane Data with M Section Allocation in Frame (Horizontal Active : H pixels)

	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
V Blank	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
Line 1	FSBP*	FSBP*	FSBP*	FSBP*	FSBP*	FSBP*	FSBP*	FSBP*
	•	•	•	•	•	•	•	•
	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR	FSBE_SR
	Pixel 1**	Pixel 2**	Pixel 481**	Pixel 482**	Pixel 961**	Pixel 962**	Pixel 1441**	Pixel 1442**
	Pixel 3	Pixel 4	Pixel 483	Pixel 484	Pixel 963	Pixel 964	Pixel 1443	Pixel 1444
	Pixel 479	Pixel 480	Pixel 959	Pixel 960	Pixel 1439	Pixel 1440	Pixel 1919	Pixel 1920
H Blank	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS
Line 2	FSBE	FSBE	FSBE	FSBE	FSBE	FSBE	FSBE	FSBE
	Pixel 1	Pixel 2	Pixel 481	Pixel 482	Pixel 961	Pixel 962	Pixel 1441	Pixel 1442
	Pixel 3	Pixel 4	Pixel 483	Pixel 484	Pixel 963	Pixel 964	Pixel 1443	Pixel 1444
	Pixel 479	Pixel 480	Pixel 959	Pixel 960	Pixel 1439	Pixel 1440	Pixel 1919	Pixel 1920
	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS	FSBS

* The 1st pixel of each lane FSBP in vertical blanking period may convey 3D flag of next frame with particular assigned CTL bit

** The 1st pixel of each lane in a frame may convey 3D flag of current frame with particular assigned bit 3DLR and 3DEN

Figure 29 8 Lane Data with 4 Section Allocation Example (Horizontal Active : 1920 pixels)

For the DTV application, data lane number in Table 1 is STRONGLY recommended for interoperability.

4.2.2. Inter-lane Skewing

Allowable inter-lane skew is defined as tRISK. Refer to section 3.3.

V-by-One[®] HS transmitter is not required to make any intentional inter-lane skew between lanes.

4.2.3. RGB+CMY Color Mode

If the transmitter and the receiver adopt the RGB+CMY (6 color mode) transmission, twice of the lanes are used for the RGB and CMY. In the CMY lanes, the positions of the C data, M data, and Y data are mapped at the positions of the R data, G data, and B data in the Table 11, respectively.

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4.3. 3D Frame Identification

3D display may have identification on every frame. Methods to label 3D information on frame are described. The description of 3D data allocation in this chapter is informative. Actual application may be different.

2 possible alternatives are introduced in this chapter; however, to apply both methods at the same time does not have to be required. Users have to choose one explicit method for their application.

4.3.1. 3D Flag on Blanking Period

Packer and unpacker data mapping in Table 2 and Table 3 show that there is a potential to send arbitrary data on V-by-One® HS during blanking period. One way to carry 3D information is to make use of CTL data mapping. Use of CTL<1:0> is implementation specific.

4.3.1.1. CTL Data Allocation to 3D Flag

It is suggested that CTL<0> and CTL<1> be used for 3D signaling. These signals correspond to CTL<1:0> in Table 2 and Table 3.

CTL<0> = Left/Right Indicator

CTL<0> = high (1) → the next frame is the left view

CTL<0> = low (0) → the next frame is the right view

CTL<1> = 3D Mode Enable

CTL<1> = high (1) → 3D video is being transmitted

CTL<1> = low (0) → 2D video is being transmitted

4.3.1.2. CTL Data Timing of 3D Flag

CTL<1:0> of the first pixel of the FSBP on each lane in vertical blanking period is recommended to be used for processing on receiver side.

It is recommended to apply to the active video that immediately follows the vertical blanking period.

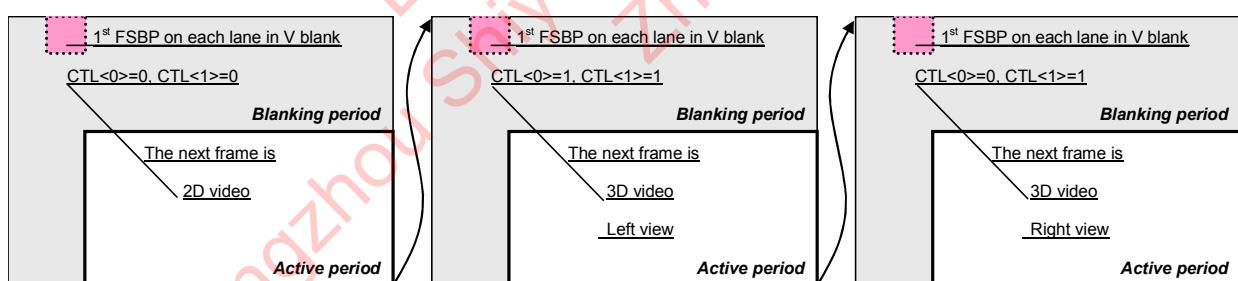


Figure 30 Schematic Diagram of 3D Flag on Blanking Period

4.3.2. 3D Flag on DE Active Period

The color data mapping in Table 11 and Table 12 show that there are unused bits depending on the colors and byte mode used. It is possible (and allowable) to make use of these unused bits to carry the 3D information. Use of 3DLR and 3DEN is implementation specific.

4.3.2.1. Color Data Mapping Allocation to 3D Flag

3D information can be conveyed using the 3DLR and 3DEN bits in Table 11. The 30bpp RGB/YCbCr 4 byte mode and 36bpp RGB/YCbCr 5 byte of Table 11 show the recommended placement of these controls.

3DLR = Left/Right Indicator

3DLR = high (1) → the next frame is the left view

3DLR = low (0) → the next frame is the right view

3DEN = 3D Mode Enable

3DEN = high (1) → 3D video is being transmitted

3DEN = low (0) → 2D video is being transmitted

4.3.2.2. Color Data Mapping Timing of 3D Flag

3DLR and 3DEN of the first pixel on each lane in particular frame is recommended to be used for processing.

It is recommended to apply 3D flag to the current frame.

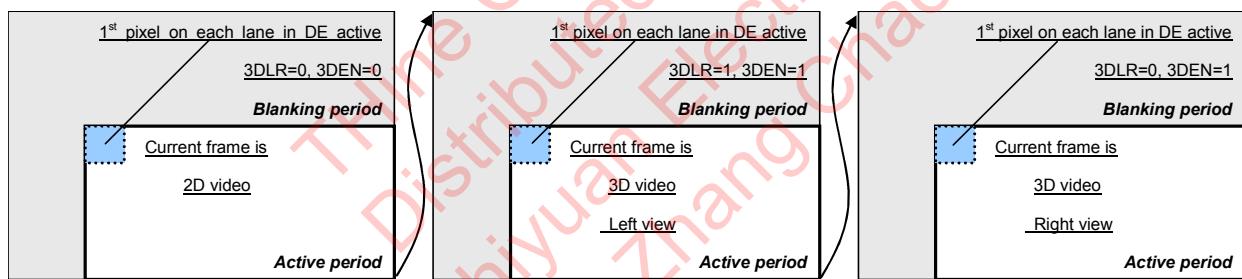


Figure 31 Schematic Diagram of 3D Flag on DE Active Period

4.4. Countermeasure against Frequency Change

Some systems have unavoidable frequency change during operation when it is supposed to keep particular frequency for continuous stream. Because V-by-One® HS is the signal stream whose speed depending on inputted clock frequency, this frequency change during operation can result into undesired visible error. In order to avoid harmful situation, possible options are presented in this section.

First method is to stop data stream completely as described in 2.2.4 case (a) before changing frequency and restart link with the new frequency. This method can avoid signal unstable period in whole system.

Second method is to make frequency anomaly slow and easy enough even if it is undesired when it is originally supposed to keep particular frequency.

Third method is to place short time frequency anomaly occasion on long enough invisible blanking period when it is originally supposed to keep particular frequency. Frequency shift may cause unstable signal and require recovery time, while blanking period could prevent this unstable situation from actual visible experience at maximum extent. Possible example is shown below. Early stage of FSBP in vertical blanking period is one reasonable recommended option for frequency change occasion.

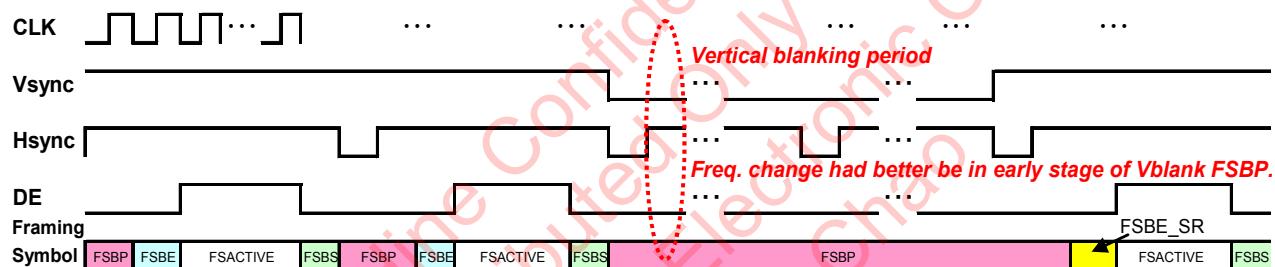


Figure 32 Frequency Change Timing Control Recommendation

Those method described in this section requires understanding of not only discrete device implementer but also whole system architect and especially designer of transmitter or signal source device.

4.5. Transmitter Output Sequence

Before CDR training, transmitter should be fixed to some voltage level in order to avoid undesired output. Otherwise, receiver operation may fail by the undesired output from the transmitter [Informative]. The detail of transmitter state diagram is shown in Figure 14.

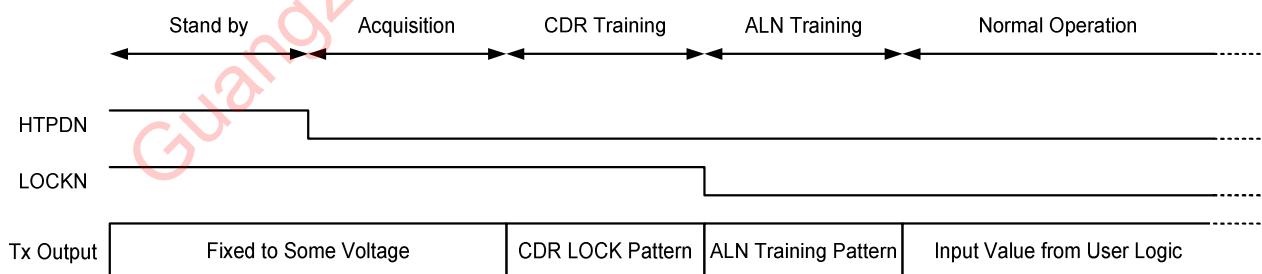


Figure 33 Transmitter Output Sequence

5. Connector and Cable

This chapter shows guideline of connector and cable to connect the V-by-One® HS transmitter (e.g. video processing unit) and receiver (e.g. panel module).

5.1. Interoperability Order of Priority

For interoperability, the following points are STRONGLY RECOMMENDED to be paid attention to.

- Pin assignment for V-by-One® HS transmission is absolutely irreplaceable and must be fixed.
- V-by-One® HS Hot Plug Detect
- V-by-One® HS Lock Detect
- V-by-One® HS CML Ground
- V-by-One® HS Lane

The following is an example of 8 lane case. V-by-One® HS related pin assignment must be kept.

Table 13 Irreplaceable V-by-One® HS Transmission Signals on 8 Lane Pin Assignment

Tx		Description	Rx	
Pin No.	Symbol		Symbol	Pin No.
51	Vcc	Supply voltage for module	Vcc	1
50	Vcc	Supply voltage for module	Vcc	2
49	Vcc	Supply voltage for module	Vcc	3
48	Vcc	Supply voltage for module	Vcc	4
47	(Option)	(User option)	(Option)	5
46	(Option)	(User option)	(Option)	6
45	(Option)	(User option)	(Option)	7
44	(Option)	(User option)	(Option)	8
43	(Option)	(User option)	(Option)	9
42	(Option)	(User option)	(Option)	10
41	(Option)	(User option)	(Option)	11
40	(Option)	(User option)	(Option)	12
39	(Option)	(User option)	(Option)	13
38	(Option)	(User option)	(Option)	14
37	(Option)	(User option)	(Option)	15
36	HTPDN	V-by-One HS Hot plug detect	HTPDN	16
35	LOCKN	V-by-One HS Lock detect	LOCKN	17
34	CML_GND	V-by-One HS CML Ground	CML_GND	18
33	Tx0n	V-by-One HS Lane0 (CML)	Rx0n	19
32	Tx0p	V-by-One HS Lane0 (CML)	Rx0p	20
31	CML_GND	V-by-One HS CML Ground	CML_GND	21
30	CML_GND	V-by-One HS CML Ground	CML_GND	22
29	Tx1n	V-by-One HS Lane1 (CML)	Rx1n	23
28	Tx1p	V-by-One HS Lane1 (CML)	Rx1p	24
27	CML_GND	V-by-One HS CML Ground	CML_GND	25
26	CML_GND	V-by-One HS CML Ground	CML_GND	26
25	Tx2n	V-by-One HS Lane2 (CML)	Rx2n	27
24	Tx2p	V-by-One HS Lane2 (CML)	Rx2p	28
23	CML_GND	V-by-One HS CML Ground	CML_GND	29
22	CML_GND	V-by-One HS CML Ground	CML_GND	30
21	Tx3n	V-by-One HS Lane3 (CML)	Rx3n	31
20	Tx3p	V-by-One HS Lane3 (CML)	Rx3p	32
19	CML_GND	V-by-One HS CML Ground	CML_GND	33
18	CML_GND	V-by-One HS CML Ground	CML_GND	34
17	Tx4n	V-by-One HS Lane4 (CML)	Rx4n	35
16	Tx4p	V-by-One HS Lane4 (CML)	Rx4p	36
15	CML_GND	V-by-One HS CML Ground	CML_GND	37
14	CML_GND	V-by-One HS CML Ground	CML_GND	38
13	Tx5n	V-by-One HS Lane5 (CML)	Rx5n	39
12	Tx5p	V-by-One HS Lane5 (CML)	Rx5p	40
11	CML_GND	V-by-One HS CML Ground	CML_GND	41
10	CML_GND	V-by-One HS CML Ground	CML_GND	42
9	Tx6n	V-by-One HS Lane6 (CML)	Rx6n	43
8	Tx6p	V-by-One HS Lane6 (CML)	Rx6p	44
7	CML_GND	V-by-One HS CML Ground	CML_GND	45
6	CML_GND	V-by-One HS CML Ground	CML_GND	46
5	Tx7n	V-by-One HS Lane7 (CML)	Rx7n	47
4	Tx7p	V-by-One HS Lane7 (CML)	Rx7p	48
3	CML_GND	V-by-One HS CML Ground	CML_GND	49
2	(Option)	(User option)	(Option)	50
1	(Option)	(User option)	(Option)	51

- If power is supplied, the following rules must be kept.
 - It must be placed from Rx pin No. 1 to Rx pin No. x .with sufficient number required.
 - Minimum number of power is standard defined and another (option) pins can be added to power.

The following is an example of 8 lane case. power supply pin assignment must be from Rx pin No. 1.

Table 14 Irreplaceable Power Supply Pins on 8 Lane Pin Assignment

Tx		Description	Rx	
Pin No.	Symbol		Symbol	Pin No.
51	Vcc	Supply voltage for module	Vcc	1
50	Vcc	Supply voltage for module	Vcc	2
49	Vcc	Supply voltage for module	Vcc	3
48	Vcc	Supply voltage for module	Vcc	4
47	(Option)	(User option)	(Option)	5
46	(Option)	(User option)	(Option)	6
45	(Option)	(User option)	(Option)	7
44	(Option)	(User option)	(Option)	8
43	(Option)	(User option)	(Option)	9
42	(Option)	(User option)	(Option)	10
41	(Option)	(User option)	(Option)	11
40	(Option)	(User option)	(Option)	12
39	(Option)	(User option)	(Option)	13
38	(Option)	(User option)	(Option)	14
37	(Option)	(User option)	(Option)	15
36	HTPDN	V-by-One HS Hot plug detect	HTPDN	16
35	LOCKN	V-by-One HS Lock detect	LOCKN	17
34	CML GND	V-by-One HS CML Ground	CML GND	18
33	Tx0n	V-by-One HS Lane0 (CML)	Rx0n	19
32	Tx0p	V-by-One HS Lane0 (CML)	Rx0p	20
31	CML GND	V-by-One HS CML Ground	CML GND	21
30	CML GND	V-by-One HS CML Ground	CML GND	22
29	Tx1n	V-by-One HS Lane1 (CML)	Rx1n	23
28	Tx1p	V-by-One HS Lane1 (CML)	Rx1p	24
27	CML GND	V-by-One HS CML Ground	CML GND	25
26	CML GND	V-by-One HS CML Ground	CML GND	26
25	Tx2n	V-by-One HS Lane2 (CML)	Rx2n	27
24	Tx2p	V-by-One HS Lane2 (CML)	Rx2p	28
23	CML GND	V-by-One HS CML Ground	CML GND	29
22	CML GND	V-by-One HS CML Ground	CML GND	30
21	Tx3n	V-by-One HS Lane3 (CML)	Rx3n	31
20	Tx3p	V-by-One HS Lane3 (CML)	Rx3p	32
19	CML GND	V-by-One HS CML Ground	CML GND	33
18	CML GND	V-by-One HS CML Ground	CML GND	34
17	Tx4n	V-by-One HS Lane4 (CML)	Rx4n	35
16	Tx4p	V-by-One HS Lane4 (CML)	Rx4p	36
15	CML GND	V-by-One HS CML Ground	CML GND	37
14	CML GND	V-by-One HS CML Ground	CML GND	38
13	Tx5n	V-by-One HS Lane5 (CML)	Rx5n	39
12	Tx5p	V-by-One HS Lane5 (CML)	Rx5p	40
11	CML GND	V-by-One HS CML Ground	CML GND	41
10	CML GND	V-by-One HS CML Ground	CML GND	42
9	Tx6n	V-by-One HS Lane6 (CML)	Rx6n	43
8	Tx6p	V-by-One HS Lane6 (CML)	Rx6p	44
7	CML GND	V-by-One HS CML Ground	CML GND	45
6	CML GND	V-by-One HS CML Ground	CML GND	46
5	Tx7n	V-by-One HS Lane7 (CML)	Rx7n	47
4	Tx7p	V-by-One HS Lane7 (CML)	Rx7p	48
3	CML GND	V-by-One HS CML Ground	CML GND	49
2	(Option)	(User option)	(Option)	50
1	(Option)	(User option)	(Option)	51

If system need more power supply line, another pins can be attached from (options) to power pin assignment.

Table 15 Expanded Power Supply Example on 8 Lane Pin Assignment

Tx		Description	Rx	
Pin No.	Symbol		Symbol	Pin No.
51	Vcc	Supply voltage for module	Vcc	1
50	Vcc	Supply voltage for module	Vcc	2
49	Vcc	Supply voltage for module	Vcc	3
48	Vcc	Supply voltage for module	Vcc	4
47	Vcc	Supply voltage for module (Added)	Vcc	5
46	Vcc	Supply voltage for module (Added)	Vcc	6
45	Vcc	Supply voltage for module (Added)	Vcc	7
44	Vcc	Supply voltage for module (Added)	Vcc	8
43	(Option)	(User option)	(Option)	9
42-1	-	-	-	10-51

- Pins originally assigned to (user option) can be used for any purpose.
 - It can be another power supply in order to support consumption.
 - It can be ground to stabilize power supply and V-by-One® HS transmission more.
 - Power ground pins assigned to (user option) should be beside power supply beyond 1 N/C pin
 - It can be another control signals like I2C, SPI, GPIO or other user defined transmission.
 - If there is remainder of (option) pins, those are supposed to be assigned to ground.

The following is an example of 8 lane case. There are 13 user option pins which can be used arbitrary.

Table 16 Multi Purpose User Option Pins on 8 Lane Pin Assignment

Tx		Description	Rx	
Pin No.	Symbol		Symbol	Pin No.
51	Vcc	Supply voltage for module	Vcc	1
50	Vcc	Supply voltage for module	Vcc	2
49	Vcc	Supply voltage for module	Vcc	3
48	Vcc	Supply voltage for module	Vcc	4
47	(Option)	(User option)	(Option)	5
46	(Option)	(User option)	(Option)	6
45	(Option)	(User option)	(Option)	7
44	(Option)	(User option)	(Option)	8
43	(Option)	(User option)	(Option)	9
42	(Option)	(User option)	(Option)	10
41	(Option)	(User option)	(Option)	11
40	(Option)	(User option)	(Option)	12
39	(Option)	(User option)	(Option)	13
38	(Option)	(User option)	(Option)	14
37	(Option)	(User option)	(Option)	15
36	HTPDN	V-by-One HS Hot plug detect	HTPDN	16
35	LOCKN	V-by-One HS Lock detect	LOCKN	17
34	CML GND	V-by-One HS CML Ground	CML GND	18
33	Tx0n	V-by-One HS Lane0 (CML)	Rx0n	19
32	Tx0p	V-by-One HS Lane0 (CML)	Rx0p	20
31	CML GND	V-by-One HS CML Ground	CML GND	21
30	CML GND	V-by-One HS CML Ground	CML GND	22
29	Tx1n	V-by-One HS Lane1 (CML)	Rx1n	23
28	Tx1p	V-by-One HS Lane1 (CML)	Rx1p	24
27	CML GND	V-by-One HS CML Ground	CML GND	25
26	CML GND	V-by-One HS CML Ground	CML GND	26
25	Tx2n	V-by-One HS Lane2 (CML)	Rx2n	27
24	Tx2p	V-by-One HS Lane2 (CML)	Rx2p	28
23	CML GND	V-by-One HS CML Ground	CML GND	29
22	CML GND	V-by-One HS CML Ground	CML GND	30
21	Tx3n	V-by-One HS Lane3 (CML)	Rx3n	31
20	Tx3p	V-by-One HS Lane3 (CML)	Rx3p	32
19	CML GND	V-by-One HS CML Ground	CML GND	33
18	CML GND	V-by-One HS CML Ground	CML GND	34
17	Tx4n	V-by-One HS Lane4 (CML)	Rx4n	35
16	Tx4p	V-by-One HS Lane4 (CML)	Rx4p	36
15	CML GND	V-by-One HS CML Ground	CML GND	37
14	CML GND	V-by-One HS CML Ground	CML GND	38
13	Tx5n	V-by-One HS Lane5 (CML)	Rx5n	39
12	Tx5p	V-by-One HS Lane5 (CML)	Rx5p	40
11	CML GND	V-by-One HS CML Ground	CML GND	41
10	CML GND	V-by-One HS CML Ground	CML GND	42
9	Tx6n	V-by-One HS Lane6 (CML)	Rx6n	43
8	Tx6p	V-by-One HS Lane6 (CML)	Rx6p	44
7	CML GND	V-by-One HS CML Ground	CML GND	45
6	CML GND	V-by-One HS CML Ground	CML GND	46
5	Tx7n	V-by-One HS Lane7 (CML)	Rx7n	47
4	Tx7p	V-by-One HS Lane7 (CML)	Rx7p	48
3	CML GND	V-by-One HS CML Ground	CML GND	49
2	(Option)	(User option)	(Option)	50
1	(Option)	(User option)	(Option)	51

- Multiple Rx PCBs with standard pin assignment can be connected to single carefully designed Tx PCB.
- Irreplaceable V-by-One® HS lines without HTPDN are supposed to be simply linked to Tx PCB node
- Tx HTPDN node should have two options to be connected to FFC or to be connected to Tx PCB GND
- Irreplaceable power supply lines are supposed to be simply linked to Tx PCB node
- (Option) pins are supposed to be linked to PCB node via passive component (e.g. 0Ω resistor)
- Tx PCB can be carefully designed in order to realize multi Rx supplier system with parts mount

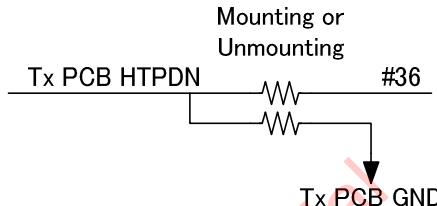


Figure 34 HTPDN Circuit on Tx PCB to Multiple Rx PCBs

The following two examples are 8 lane cases. Two standard recommended assignments are shown. Tx side PCB is the same one for both cases, while Rx side PCB is different; however, both follow the standard. Mounting or unmounting passive component on Tx PCB can realize multiple Rx PCB accommodation.

Table 17 Tx PCB Arrangement Example to Rx PCB #1 on 8 Lane Pin Assignment

Tx PCB Node via series resistor		Tx PCB arrangement condition	Rx	
Pin No.	Symbol		Symbol	Pin No.
51-50	-	Supply voltage for module	Vcc	1-2
49	Vcc	Supply voltage for module	Vcc	3
48	Vcc	Connected by mounting part on Tx PCB	Vcc	4
47	Vcc	Connected by mounting part on Tx PCB	Vcc	5
46	Vcc	Connected by mounting part on Tx PCB	Vcc	6
45	Vcc	Connected by mounting part on Tx PCB	Vcc	7
44	N/C	Not connected	N/C	8
43	GND	Connected by mounting part on Tx PCB	GND	9
42	GND	Connected by mounting part on Tx PCB	GND	10
41	GND	Connected by mounting part on Tx PCB	GND	11
40	SCL	Connected by mounting part on Tx PCB	SCL	12
39	SDA	Connected by mounting part on Tx PCB	SDA	13
38	DC control	Connected by mounting part on Tx PCB	DC control	14
37	DC control	Connected by mounting part on Tx PCB	DC control	15
36	HTPDN	Connected by mounting part on Tx PCB	HTPDN	16
35-4	CML GND	V-by-One HS CML Ground	CML GND	17-48
3	SCL	Not Connected by unmounting part on Tx PCB	GND	49
2	SDA	Not Connected by unmounting part on Tx PCB	GND	50
1	-		GND	51

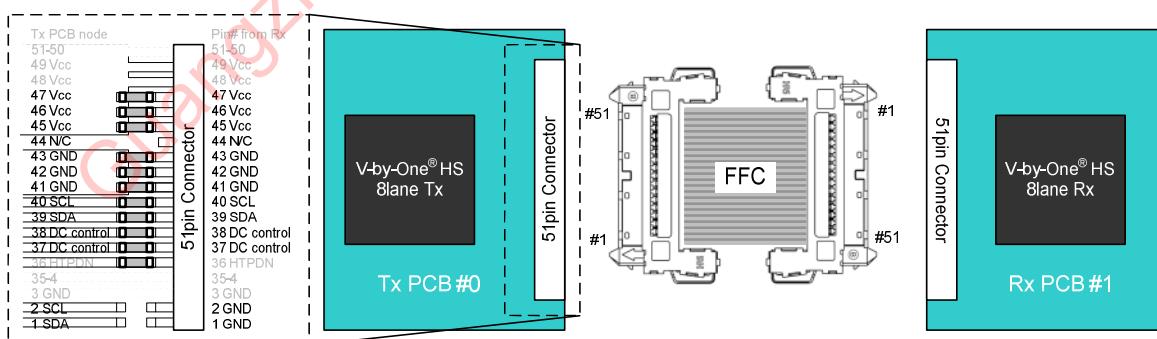
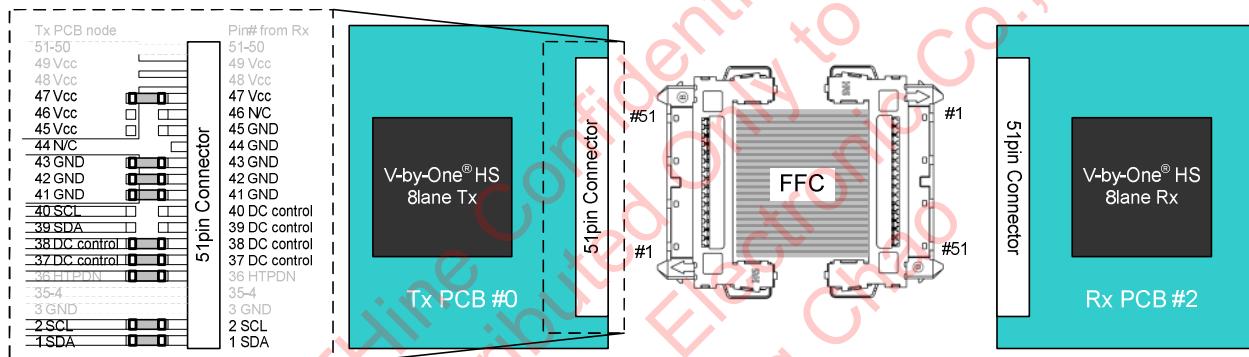


Figure 35 Tx PCB Arrangement Example to Rx PCB #1 on 8 Lane Pin Assignment

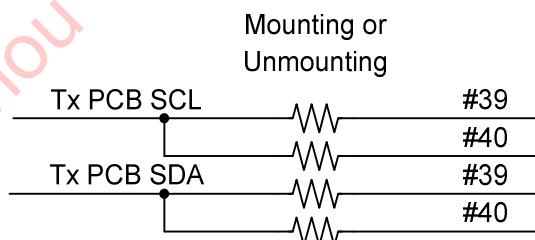
Table 18 Tx PCB Arrangement Example to Rx PCB #2 on 8 Lane Pin Assignment

Tx PCB Node via series resistor		Tx PCB arrangement condition	Rx	
Pin No.	Symbol		Symbol	Pin No.
51-50	-	-	-	1-2
49	Vcc	Supply voltage for module	Vcc	3
48	Vcc	Supply voltage for module	Vcc	4
47	Vcc	<u>Connected by mounting part on Tx PCB</u>	Vcc	5
46	Vcc	<u>Not Connected by unmounting part on Tx PCB</u>	NC	6
45	Vcc	<u>Not Connected by unmounting part on Tx PCB</u>	GND	7
44	N/C	<u>Not connected</u>	GND	8
43	GND	<u>Connected by mounting part on Tx PCB</u>	GND	9
42	GND	<u>Connected by mounting part on Tx PCB</u>	GND	10
41	GND	<u>Connected by mounting part on Tx PCB</u>	GND	11
40	SCL	<u>Not Connected by unmounting part on Tx PCB</u>	DC control	12
39	SDA	<u>Not Connected by unmounting part on Tx PCB</u>	DC control	13
38	DC control	<u>Connected by mounting part on Tx PCB</u>	DC control	14
37	DC control	<u>Connected by mounting part on Tx PCB</u>	DC control	15
36	HTPDN	<u>Connected by mounting part on Tx PCB</u>	HTPDN	16
35-4	-	V-by-One HS CML Ground	CML GND	17-48
3	CML GND	<u>Connected by mounting part on Tx PCB</u>	SCL	49
2	SCL	<u>Connected by mounting part on Tx PCB</u>	SDA	50
1	SDA	<u>Connected by mounting part on Tx PCB</u>	-	51

**Figure 36 Tx PCB Arrangement Example to Rx PCB #1 on 8 Lane Pin Assignment**

Just for more information, Tx side PCB can also be designed to reverse pin assignment.

For example, [pin #39 SCL, pin #40 SDA] can be inverted to [pin #39 SDA, pin #40 SCL] with carefully designed PCB and mounting several passive components at the same time.

**Figure 37 Circuit to Reverse Pin Assignment on Tx PCB**

5.2. Pin Assignments

5.2.1. Normal Ground Format

1,2,4, and 8-lane pin assignments are shown below.

Table 19 Normal CML Ground Format Pin Assignment

Normal CML GND Format	HD60Hz RGB30bit	FHD60Hz RGB30bit	FHD120Hz RGB30bit	FHD240Hz RGB30bit
Pin No.	21pins	21pins	31pins	51pins
to Panel (Rx)				
1	Vcc	Vcc	Vcc	Vcc
2	Vcc	Vcc	Vcc	Vcc
3	(Option)	(Option)	Vcc	Vcc
4	(Option)	(Option)	(Option)	Vcc
5	(Option)	(Option)	(Option)	(Option)
6	(Option)	(Option)	(Option)	(Option)
7	(Option)	(Option)	(Option)	(Option)
8	(Option)	(Option)	(Option)	(Option)
9	(Option)	(Option)	(Option)	(Option)
10	(HTPDN*)	(HTPDN*)	(Option)	(Option)
11	LOCKN	LOCKN	(Option)	(Option)
12	CML GND	CML GND	(HTPDN*)	(Option)
13	Rx0n	Rx0n	LOCKN	(Option)
14	Rx0p	Rx0p	CML GND	(Option)
15	CML GND	CML GND	Rx0n	(Option)
16	(Option)	CML GND	Rx0p	(HTPDN*)
17	(Option)	Rx1n	CML GND	LOCKN
18	(Option)	Rx1p	CML GND	CML GND
19	(Option)	CML GND	Rx1n	Rx0n
20	(Option)	(Option)	Rx1p	Rx0p
21	(Option)	(Option)	CML GND	CML GND
22			CML GND	CML GND
23			Rx2n	Rx1n
24			Rx2p	Rx1p
25			CML GND	CML GND
26			CML GND	CML GND
27			Rx3n	Rx2n
28			Rx3p	Rx2p
29			CML GND	CML GND
30			(Option)	Rx3n
31			(Option)	Rx3p
32			CML GND	CML GND
33			CML GND	CML GND
34			Rx4n	Rx4n
35			Rx4p	Rx4p
36			CML GND	CML GND
37			CML GND	Rx5n
38			Rx5p	Rx5p
39			CML GND	CML GND
40			CML GND	Rx6n
41			CML GND	Rx6p
42			CML GND	CML GND
43			Rx7n	Rx7n
44			Rx7p	Rx7p
45			CML GND	(Option)
46			CML GND	(Option)
47				
48				
49				
50				
51				

5.2.2. Reduced Ground Format

Some systems require both a lot of user option signals or power supply pins and a lot of lanes at the same time. For that case, reduced CML ground format is presented.

Around maximum speed transmission, this reduced ground format gives only slight margin; therefore, users must pay attentions to transmitter and receiver characteristics, PCB design, and connector/harness selection so that receiver side Eye diagram is wide enough to establish V-by-One® HS transmission.

Table 20 8 Lane Connector Reduced CML Ground Format Pin Assignment

Tx		Description	Rx	
Pin No.	Symbol		Symbol	Pin No.
51	Vcc	Supply voltage for module	Vcc	1
50	Vcc	Supply voltage for module	Vcc	2
49	Vcc	Supply voltage for module	Vcc	3
48	Vcc	Supply voltage for module	Vcc	4
47	(Option)	(User option)	(Option)	5
46	(Option)	(User option)	(Option)	6
45	(Option)	(User option)	(Option)	7
44	(Option)	(User option)	(Option)	8
43	(Option)	(User option)	(Option)	9
42	(Option)	(User option)	(Option)	10
41	(Option)	(User option)	(Option)	11
40	(Option)	(User option)	(Option)	12
39	(Option)	(User option)	(Option)	13
38	(Option)	(User option)	(Option)	14
37	(Option)	(User option)	(Option)	15
36	(Option)	(User option)	(Option)	16
35	(Option)	(User option)	(Option)	17
34	(Option)	(User option)	(Option)	18
33	(Option)	(User option)	(Option)	19
32	(Option)	(User option)	(Option)	20
31	(Option)	(User option)	(Option)	21
30	(Option)	(User option)	(Option)	22
29	(Option)	(User option)	(Option)	23
28	(Option)	(User option)	(Option)	24
27	(HTPDN*)	(V-by-One HS Hot plug detect*)	(HTPDN*)	25
26	LOCKN	V-by-One HS Lock detect	LOCKN	26
25	CML GND	V-by-One HS CML Ground	CML GND	27
24	Tx0n	V-by-One HS Lane0 (CML)	Rx0n	28
23	Tx0p	V-by-One HS Lane0 (CML)	Rx0p	29
22	CML GND	V-by-One HS CML Ground	CML GND	30
21	Tx1n	V-by-One HS Lane1 (CML)	Rx1n	31
20	Tx1p	V-by-One HS Lane1 (CML)	Rx1p	32
19	CML GND	V-by-One HS CML Ground	CML GND	33
18	Tx2n	V-by-One HS Lane2 (CML)	Rx2n	34
17	Tx2p	V-by-One HS Lane2 (CML)	Rx2p	35
16	CML GND	V-by-One HS CML Ground	CML GND	36
15	Tx3n	V-by-One HS Lane3 (CML)	Rx3n	37
14	Tx3p	V-by-One HS Lane3 (CML)	Rx3p	38
13	CML GND	V-by-One HS CML Ground	CML GND	39
12	Tx4n	V-by-One HS Lane4 (CML)	Rx4n	40
11	Tx4p	V-by-One HS Lane4 (CML)	Rx4p	41
10	CML GND	V-by-One HS CML Ground	CML GND	42
9	Tx5n	V-by-One HS Lane5 (CML)	Rx5n	43
8	Tx5p	V-by-One HS Lane5 (CML)	Rx5p	44
7	CML GND	V-by-One HS CML Ground	CML GND	45
6	Tx6n	V-by-One HS Lane6 (CML)	Rx6n	46
5	Tx6p	V-by-One HS Lane6 (CML)	Rx6p	47
4	CML GND	V-by-One HS CML Ground	CML GND	48
3	Tx7n	V-by-One HS Lane7 (CML)	Rx7n	49
2	Tx7p	V-by-One HS Lane7 (CML)	Rx7p	50
1	CML GND	V-by-One HS CML Ground	CML GND	51

* HTPDN connection can be eliminated in prepared system and turn it into ground or other user options.

4,8,16, 32 lane pin assignments are shown below.

Table 21 Reduced CML Ground Format Pin Assignment

Reduced CML GND Format	FHD120Hz RGB30bit 41pins	FHD240Hz RGB30bit 51pins	4K2K120Hz RGB30bit 51pins	41pins
Pin No.	41pins	51pins	51pins	41pins
to Panel (Rx)				
1	Vcc	Vcc	Vcc	CML GND
2	Vcc	Vcc	Vcc	Rx8n
3	Vcc	Vcc	Vcc	Rx8p
4	(Option)	Vcc	Vcc	CML GND
5	(Option)	(Option)	(Option)	Rx9n
6	(Option)	(Option)	(Option)	Rx9p
7	(Option)	(Option)	(Option)	CML GND
8	(Option)	(Option)	(Option)	Rx10n
9	(Option)	(Option)	(Option)	Rx10p
10	(Option)	(Option)	(Option)	CML GND
11	(Option)	(Option)	(Option)	Rx11n
12	(Option)	(Option)	(Option)	Rx11p
13	(Option)	(Option)	(Option)	CML GND
14	(Option)	(Option)	(Option)	Rx12n
15	(Option)	(Option)	(Option)	Rx12p
16	(Option)	(Option)	(Option)	CML GND
17	(Option)	(Option)	(Option)	Rx13n
18	(Option)	(Option)	(Option)	Rx13p
19	(Option)	(Option)	(Option)	CML GND
20	(Option)	(Option)	(Option)	Rx14n
21	(Option)	(Option)	(Option)	Rx14p
22	(Option)	(Option)	(Option)	CML GND
23	(Option)	(Option)	(Option)	Rx15n
24	(Option)	(Option)	(Option)	Rx15p
25	(HTPDN*)	(HTPDN*)	(HTPDN*)	CML GND
26	LOCKN	LOCKN	LOCKN	(Option)
27	CML GND	CML GND	CML GND	(Option)
28	Rx0n	Rx0n	Rx0n	(Option)
29	Rx0p	Rx0p	Rx0p	(Option)
30	CML GND	CML GND	CML GND	(Option)
31	Rx1n	Rx1n	Rx1n	(Option)
32	Rx1p	Rx1p	Rx1p	(Option)
33	CML GND	CML GND	CML GND	(Option)
34	Rx2n	Rx2n	Rx2n	(Option)
35	Rx2p	Rx2p	Rx2p	(Option)
36	CML GND	CML GND	CML GND	(Option)
37	Rx3n	Rx3n	Rx3n	(Option)
38	Rx3p	Rx3p	Rx3p	(Option)
39	CML GND	CML GND	CML GND	(Option)
40	(Option)	Rx4n	Rx4n	(Option)
41	(Option)	Rx4p	Rx4p	(Option)
42		CML GND	CML GND	
43		Rx5n	Rx5n	
44		Rx5p	Rx5p	
45		CML GND	CML GND	
46		Rx6n	Rx6n	
47		Rx6p	Rx6p	
48		CML GND	CML GND	
49		Rx7n	Rx7n	
50		Rx7p	Rx7p	
51		CML GND	CML GND	

Table 22 Reduced CML Ground Format Pin Assignment (Continue)

Reduced CML GND Format	4K2K240Hz RGB30bit		
Pin No.	51pins	41pins	41pins
to Panel (Rx)			
1	Vcc	CML GND	CML GND
2	Vcc	Rx8n	Rx20n
3	Vcc	Rx8p	Rx20p
4	Vcc	CML GND	CML GND
5	(Option)	Rx9n	Rx21n
6	(Option)	Rx9p	Rx21p
7	(Option)	CML GND	CML GND
8	(Option)	Rx10n	Rx22n
9	(Option)	Rx10p	Rx22p
10	(Option)	CML GND	CML GND
11	(Option)	Rx11n	Rx23n
12	(Option)	Rx11p	Rx23p
13	(Option)	CML GND	CML GND
14	(Option)	Rx12n	Rx24n
15	(Option)	Rx12p	Rx24p
16	(Option)	CML GND	CML GND
17	(Option)	Rx13n	Rx25n
18	(Option)	Rx13p	Rx25p
19	(Option)	CML GND	CML GND
20	(Option)	Rx14n	Rx26n
21	(Option)	Rx14p	Rx26p
22	(Option)	CML GND	CML GND
23	(Option)	Rx15n	Rx27n
24	(Option)	Rx15p	Rx27p
25	(HTPDN*)	CML GND	CML GND
26	LOCKN	Rx16n	Rx28n
27	CML GND	Rx16p	Rx28p
28	Rx0n	CML GND	CML GND
29	Rx0p	Rx17n	Rx29n
30	CML GND	Rx17p	Rx29p
31	Rx1n	CML GND	CML GND
32	Rx1p	Rx18n	Rx30n
33	CML GND	Rx18p	Rx30p
34	Rx2n	CML GND	CML GND
35	Rx2p	Rx19n	Rx31n
36	CML GND	Rx19p	Rx31p
37	Rx3n	CML GND	CML GND
38	Rx3p	(Option)	(Option)
39	CML GND	(Option)	(Option)
40	Rx4n	(Option)	(Option)
41	Rx4p	(Option)	(Option)
42	CML GND		
43	Rx5n		
44	Rx5p		
45	CML GND		
46	Rx6n		
47	Rx6p		
48	CML GND		
49	Rx7n		
50	Rx7p		
51	CML GND		

Note:

Some cables like Flexible Printed Circuits (FPC) do not have the symmetric conductor layout. This means that if users connect the cable at reverse direction, i.e. Rx plug is connected to transmitter's receptacle and Tx plug to receiver's receptacle, the correct connection cannot be achieved. Users must take care with the cable direction.

5.3. Connector Characteristics

5.3.1. Electrical

- Operating Current : 0.5A per pin minimum
- Operating Voltage : 150VAC rms, maximum
- Voltage proof : 200VAC for minimum of 1 minute

5.3.2. Recommended Receptacle Interface Dimensions

0.5mm signal terminal pitch connector is recommended for interoperability.

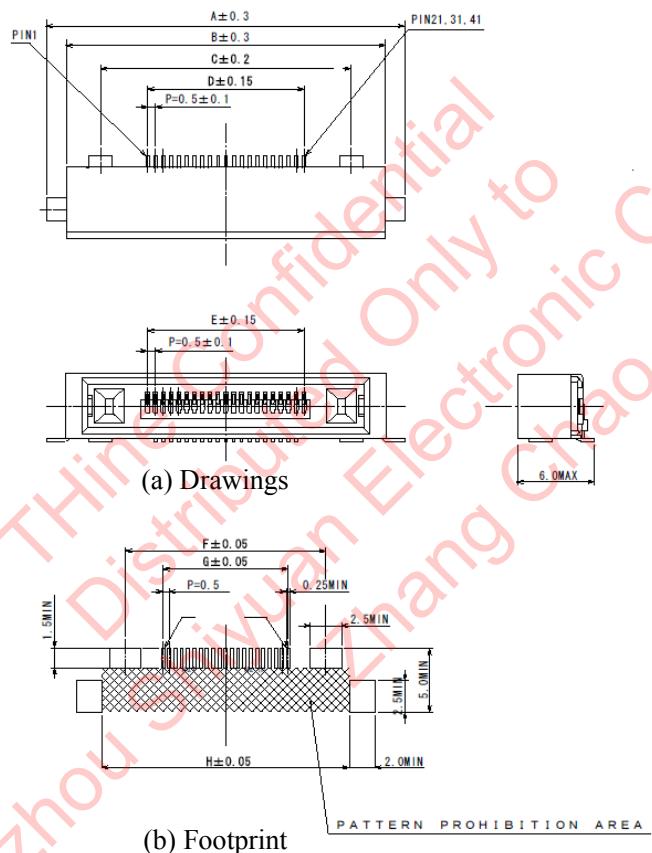


Figure 38 PCB Mount Receptacle Drawings (Recommended)

Table 23 Form Factor of Receptacle

No. of CONTACT	A	B	C	D	E	F	G	H
21	22.85	20.46	16	10	10	16	10	19.75
31	27.85	25.46	21	15	15	21	15	24.75
41	32.85	30.46	26	20	20	26	20	29.75
51	37.85	35.46	31	25	25	31	25	34.75

5.4. PCB Layout Considerations

Use at least 4-layer PCB with signals, GND, power, and signals assigned for each layer. Refer to figure below.

PCB traces for the high-speed signals must be single-ended microstrip lines or coupled microstrip lines whose differential characteristic impedance is 100Ω .

Minimize the distance between traces of a differential pair (S1 of Figure 39) to maximize common mode rejection and coupling effect which works to reduce Electro-Magnetic Interference (EMI).

Route differential signal traces symmetrically.

Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity. Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed lanes.

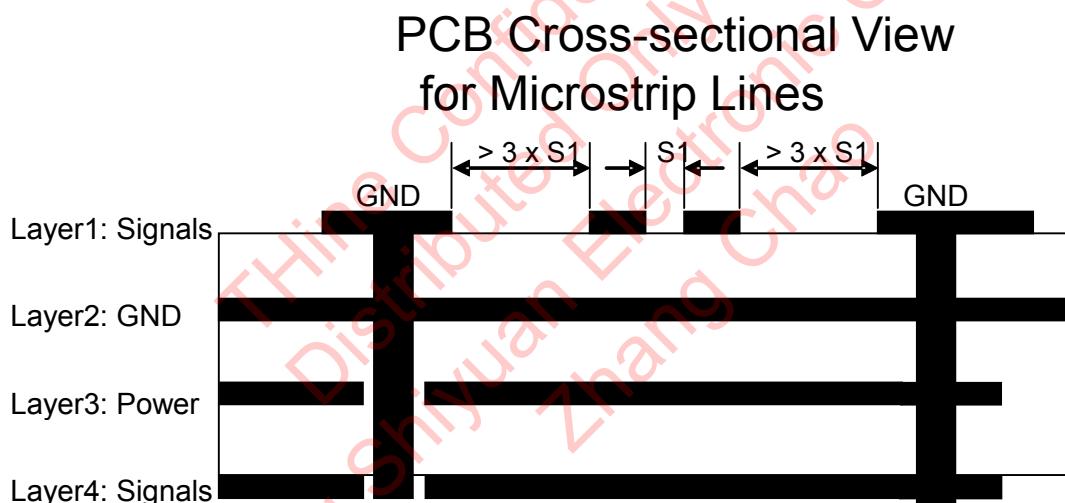


Figure 39 PCB Cross-sectional View for Microstrip Lines

6. Glossary

Table 24 Glossary of Terms

Data Lane	One Differential Signal Line
Framing Symbol	FSACTIVE, FSBS, FSBP, FSBE, and FSBE_SR are the framing symbols. One framing symbol is transmitted at the one pixel clock The size of framing symbols is decided by the byte mode
Byte Mode	3, 4, and 5 byte mode is prepared. The byte mode is decided by the color depth and color format (RGB or YCbCr etc.)
Character	8 bit data before 8b/10 encoder and after 8b/10b decoder 10 bit data after 8b/10 encoder and before 8b/10b decoder In addition to the pixel data, special character is assigned. See Table 4.

7. Revision History

Date	Version	
2008/5/26	Ver. 1.0	Original (obsolete)
2008/11/22	Ver. 1.1	<p>The color mapping is changed. The order of the pin assignment is changed.</p> <p>PLL loop bandwidth of the transmitter is defined. Electrical specifications are described for LOCKN and HTPDN. Clarify the inter-pair skew and intra-pair skew specifications. RGBY and RGB+CMY are added to the color mapping. Inter lane skew is specified in the chapter 4.2.2. Collected the training pattern (D10.2) frequency for link training in chapter 2.4.5.1 CDR training. Organization and wording correction and clarification. (obsolete)</p>
2009/1/15	Ver. 1.2	<p>The range of VDL is extended, and VOL spec. is changed. The behavior of the scrambler is corrected. Correction of the value in tRISK_INTRA and tRISK_INTER.</p> <p>The eye diagram and CML jitter at transmitter are relaxed. Clarify the receiver eye measurement point. Correction of the range of tTBIT and tRBIT. Correction of some typos.</p>
2010/07/07	Ver.1.3	<p>Scrambler/descrambler chart is corrected. LFSR proceeds with K code. Vsync “1” in ALN training allocation is corrected to 4th last pixel. ALN training period per lane is fixed independent of lane counts. No HTPDN connection option is introduced.</p> <p>Basic receiver eye diagram measurement point is at CML input pins. Transmitter intra-pair skew accuracy definition is conditioned and relaxed. Examples of lane number according to format (2560x1080p, 480Hz) are added. Guideline of frame ID transmission method for 3D display is added Receiver side eye diagram measurement CDR setting explanation is added. Data lane consideration chapter is added. Section “Cable Characteristics” is deleted. Recommended approach to interoperable pin assignment is explained. 16 lane connection pin assignment guideline is added. Discrepancy of pulled up voltage is corrected. Description of FSBE_SR is clarified. Connector form factor of 51 pins receptacle is added. Page numbers on table of contents are corrected. Correction of some typos. Some descriptions are added.</p>
2011/12/15	Ver.1.4	<p>Maximum speed is enlarged to 4Gbps. Transmitter output under Tx PLL unstable condition is defined to be fixed. Countermeasure against frequency change is additionally described. Reduced pin number pin assignment guideline is added.</p> <p>HTPDN/LOCKN detection voltages are loosened. Multiple vertical section transmission mode guideline is additionally described. Freedom of polarity about DE, Vsync, and Hsync is explicitly described. Detailed measurement method of Tx eye diagram is additionally described. 3D flag and its timing description are additionally described. Recommended approach to interoperable pin assignment is re-defined. Correction of some typos. Some descriptions are altered or added</p>
2016/11/01	Ver.1.5	<p>Requirement of FSBE_SR input interval is extended. every 512th FSBE \Rightarrow less than or equal to 512 times of FSBE input. Input timing of Vsync='1' in ALN pattern is extended. 4th last pixel \Rightarrow within the last 32 pixel counts except for 1st, 30th, 31st and 32nd pixel cycle. Transmitter output sequence is added in chapter 4.5. Some wrong descriptions are revised.</p>

8. Notices and Requests

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