AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

ELECTRICAL AND ELECTRONIC ENGINEERING

PROJECT REPORT

Project Title: Different CMOS Full Adders Analysis and Simulation

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Comparative Analysis and Simulation of Different CMOS Full Adders Using Cadence in 90 nm Technology

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***Abstract*— This project evaluates and compares four adders with different logic types (conventional, transmission gate, 14 transistors, and GDI based approach) for transistor count, power dissipation, latency, and power delay product. It is carried out on the Virtuoso platform, the Cadence tool and the available GPDK - 90nm kit. The widths of NMOS and PMOS are tuned at 330nm and 120nm, respectively. Transmission gate full adders have the advantage of fast speed but waste more power. The GDI full adder has a smaller voltage swing and is incapable of passing logic and logic 0 entirely, resulting in poor output.**

***KEYWORDS*—*CMOS*, *FULL ADDER*, *TRANSMISSION GATE*, *GATE DIFFUSION INPUT* *(GDI)*, *14T*, *DELAY*, *POWER CONSUMPTION*, *POWER DELAY PRODUCT* *(PDP)*.**

I. INTRODUCTION

Because of transferrable devices with high speed, compact size, high reliability, low power consumption, and low cost, the use of VLSI (Very Large Scale Integration) has increased.

Battery life is extended. The primary problem in this case is the amounts of transistors. The complex devices since it disrupts the area and speed of the gadget in its entirety. Many VLSI applications, such as digital signal processing, image and video processing, and microprocessors, Arithmetic operations are frequently used. As a result, the integrated the performance of a circuit is heavily dependent on how the arithmetic is done. Modules are used. The most important arithmetic operation Because a logic unit is the sum of two binary values, a full adder is the most important component of complex arithmetic circuits. The performance of integrated circuits is expected to improve significantly.

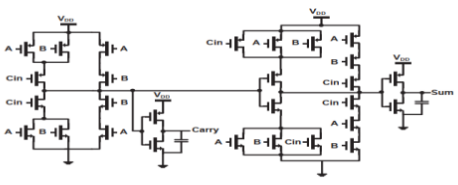


Fig. Conventional CMOS full adder.

$$Sum = ABC + (A + B + C)$$
$$Cout = AB + C(A + B)$$

The most fundamental method for implementing full adder logic across design styles is the traditional CMOS full adder. In its design, 28 transistors are used. Because the pull up network is made up of PMOS networks, it has a high input capacitance, which results in increased dynamic power and delay.

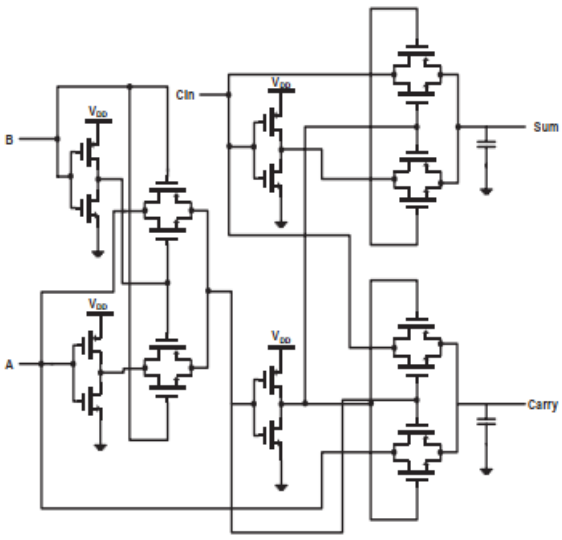


Fig. Transmission gate full adder.

Transmission gate full adder circuit requires 20 transistors to implement the design of full adder. Since the XOR gate is a crucial component of the full adder, increasing its performance will also improve the full adder's performance. Transmission gates, which require fewer transistors, are used in this circuit to build the XOR gate [5]. The transmission gate's output traverses the whole voltage range, hence the adder's output voltage degradation is quite minimal. However, compared to a typical full adder, a transmission gate full adder consumes more power.

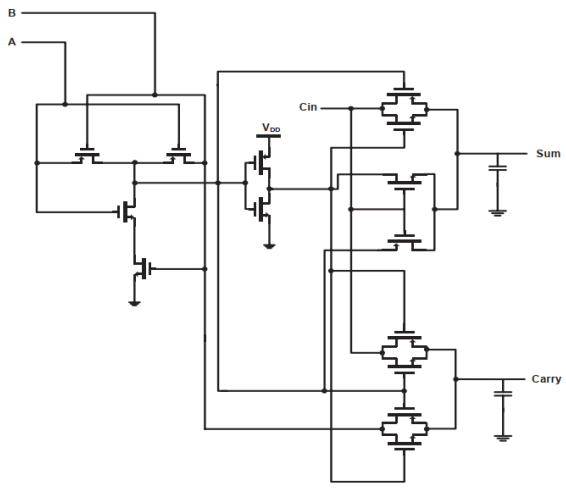


Fig. . 14 Transistor full adder.

Six transistors are saved in a 14T full adder by using only one inverter as opposed to four in a transmission gate full adder. The circuit is faster and takes up less space than a traditional CMOS full adder.

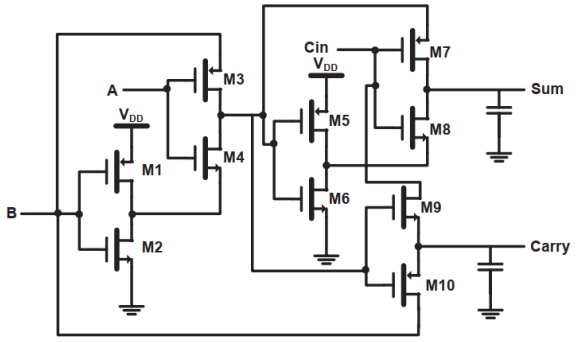


Fig. Gate diffusion input full adder.

A substitute method for CMOS logic is called Gate Diffusion Input, or GDI. It provides a way to implement logic functions using fewer transistors. Additionally, the There is little power consumption. Among the important distinctions between a GDI- and CMOS-based structure are as follows rather than attaching VDD & Ground to the PMOS source. A GDI cell contains the input signals for NMOS & & NMOS, respectively. Morgenshtein was the one who proposed the basic GDI cell. It's got three terminals for input: G (gate input from PMOS and NMOS).PMOS source input P (shorted), N (source input of NMOS. For simulating and comparing the performances of 1 bit full adder with different design topologies, CADENCE Design Suite 6.1.6 for GPDK 90nm CMOS technology operating in Virtuoso environment at room temperature was used. For the analysis, the supply voltage VDD was set at 1.2 Volt for each of the full adder. During the simulation, the inputs (A, B, C), pulses with diffrent periods were given which is VPULSE in this software, where the pulses were varied from 0 Volt to 1.2 Volt.

II. RESULTS.(DATA REPRESENTATION)

A. *Truth Table:*

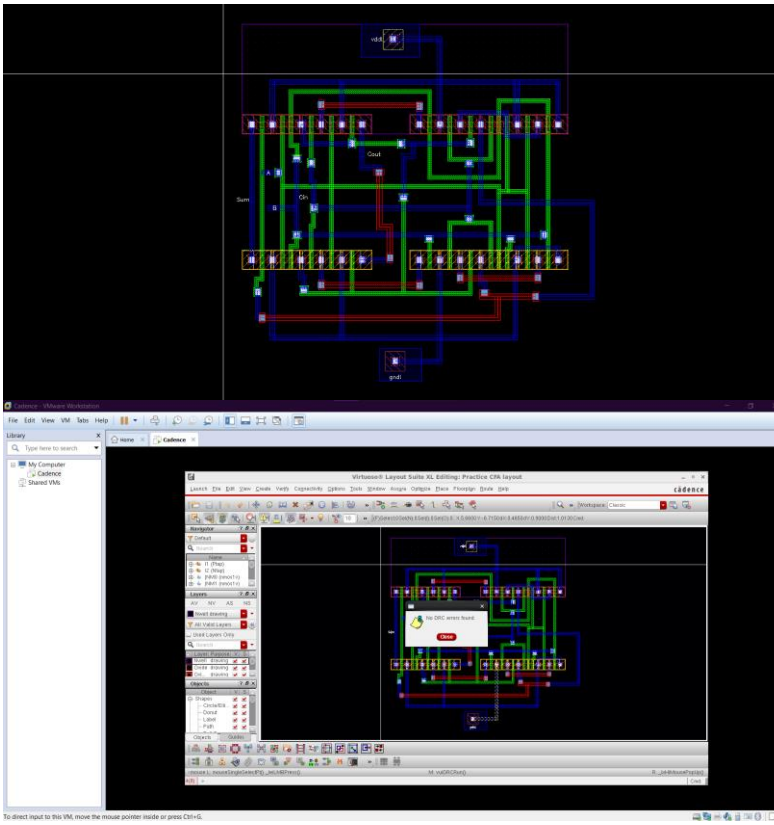
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

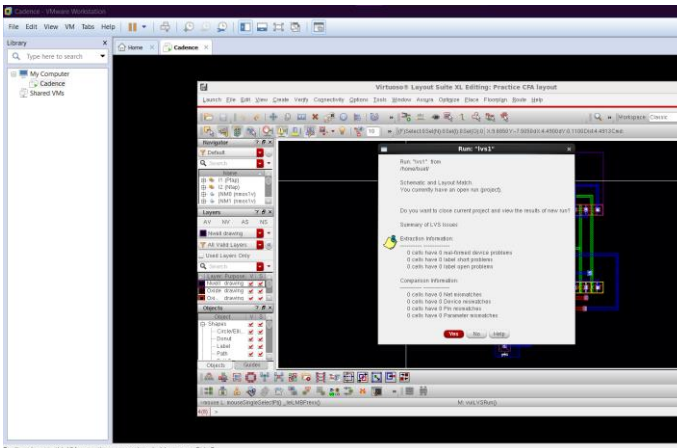
B. *Comparison Table:*

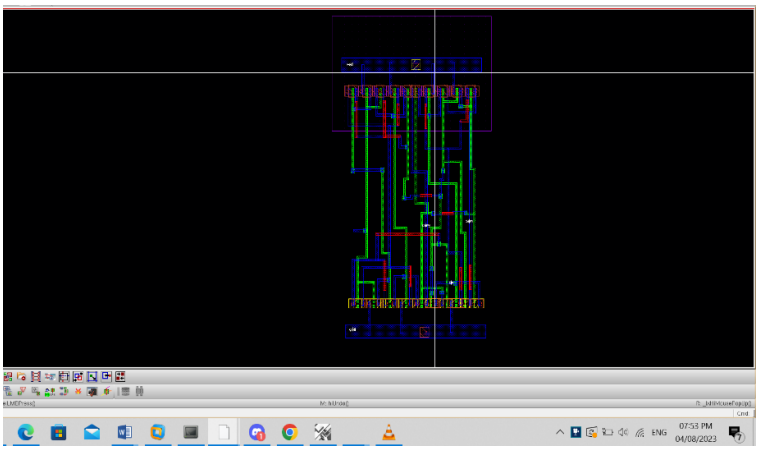
Comparison Table							
	Propagation Delay	Average Power	Power Delay Product	Cell Area	No. of Transistors	No. of DRC Errors	No. of LVS Mismatches
Conventional	67.72 ps	456.6 nW	3.09×10^{-17} J	88.497 sq um	28	0	0
Transmission Gate	4.27 ps	650.1 nW	2.77×10^{-18} J	146.5 sq um	20	0	0
14T Full Adder	3.821 ps	1.837 uW	5.613×10^{-25} J	24.2025 um	14	0	0
Gate Diffusion	7.238 ps	1.28 uW	9.26×10^{-18} J	57.696 sq um	10	0	0

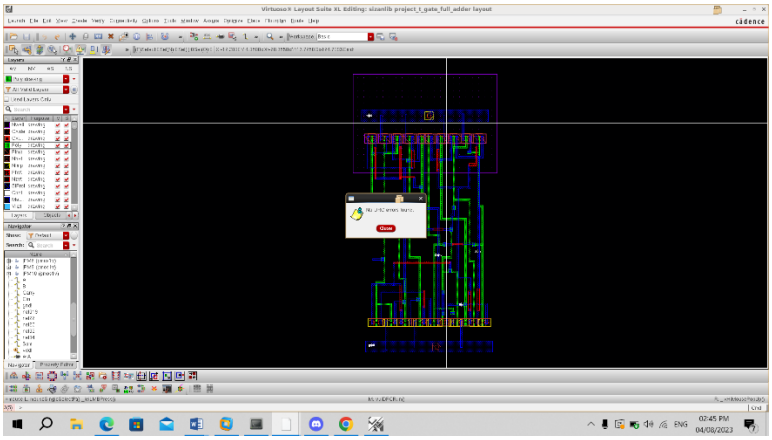
III. RESULTS.(PICTORIAL REPRESENTATION)

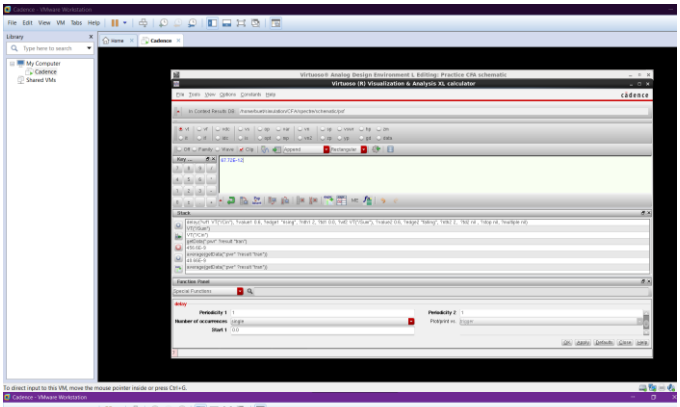
A. *Conventional CMOS Full Adder (28T)*

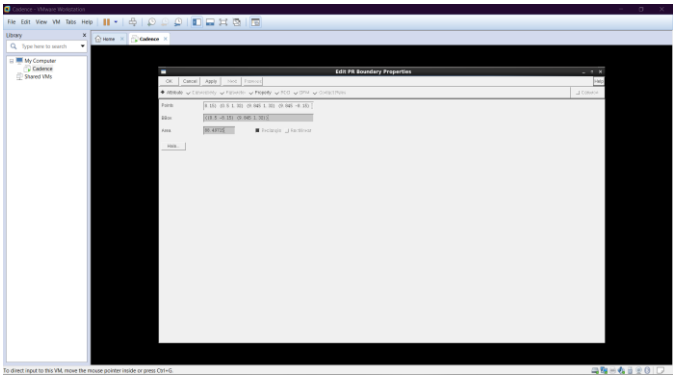


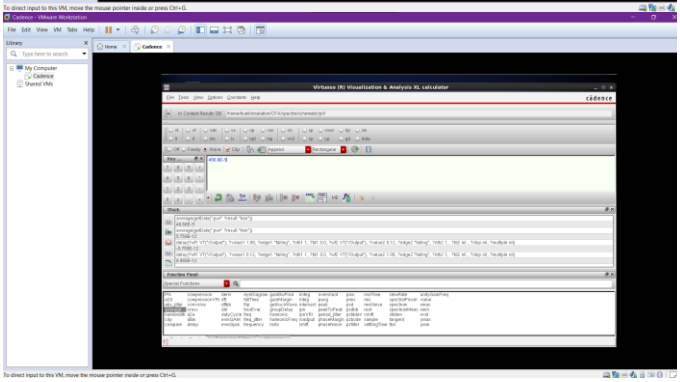




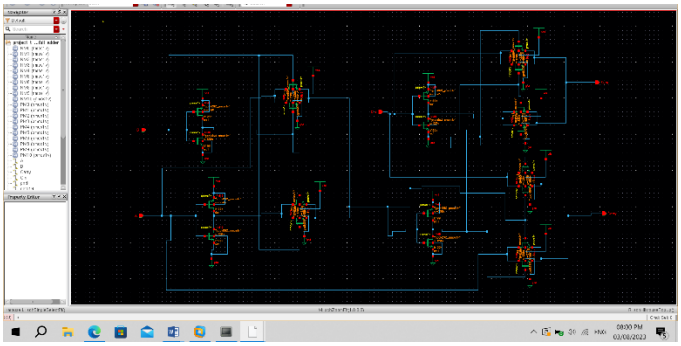


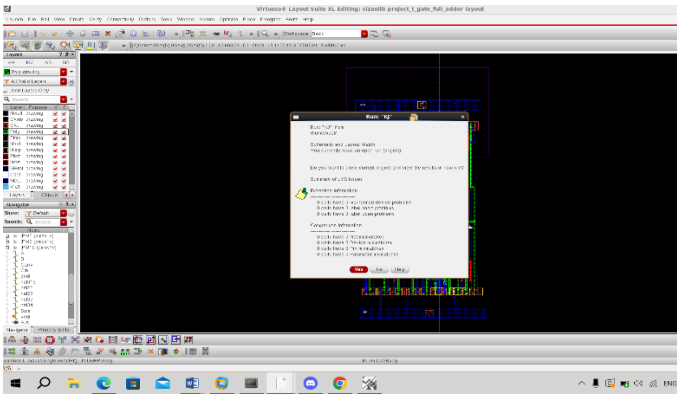


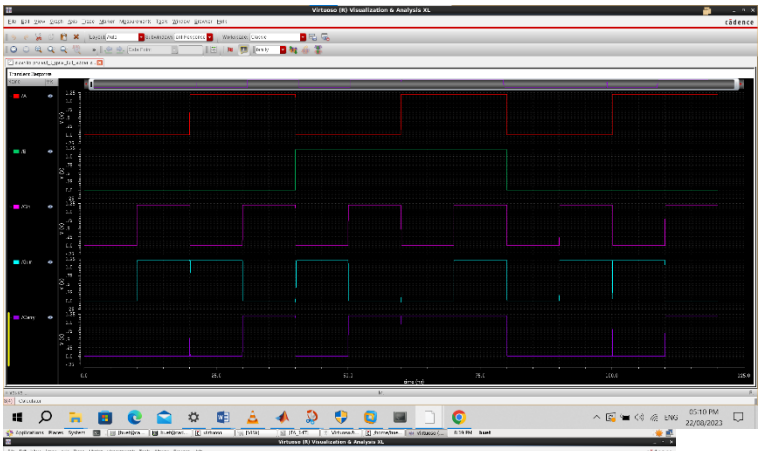


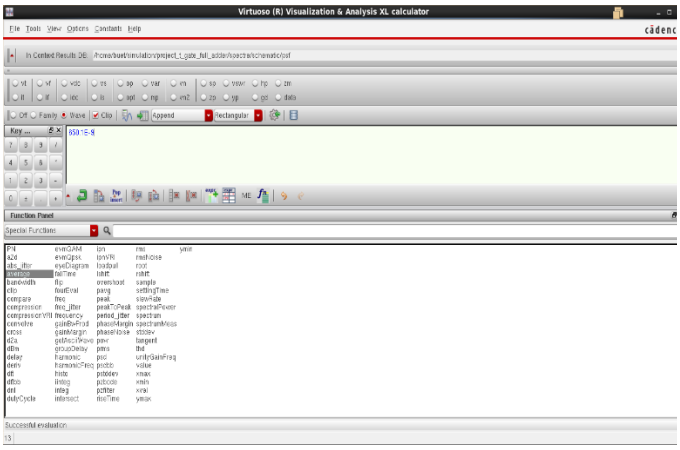


B. *Transmission Gate Full Adder (20T)*









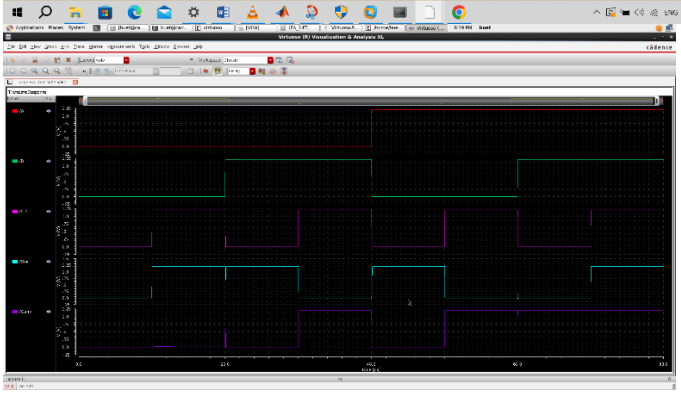
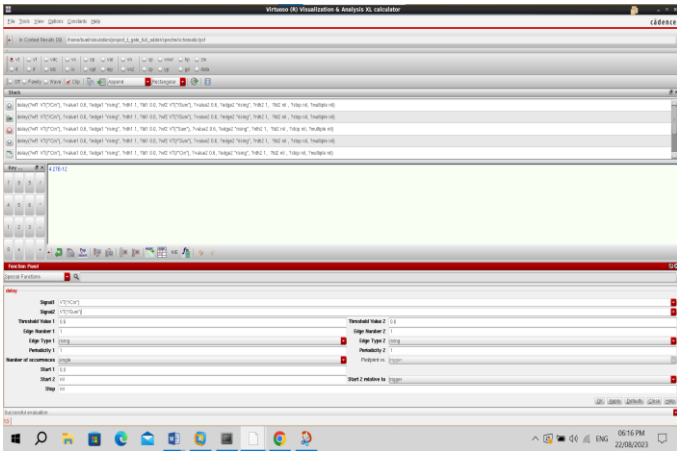


Figure: Output Waveform of Schematic



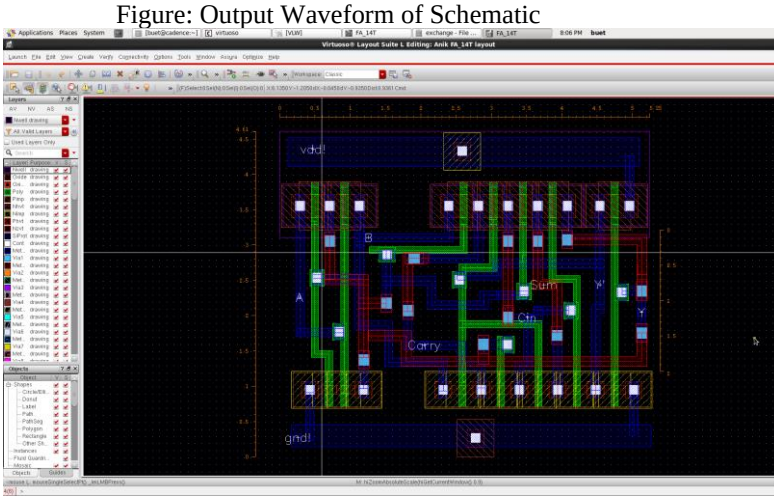


Figure: Layout

C. 14 Transistor Full Adder (14T)

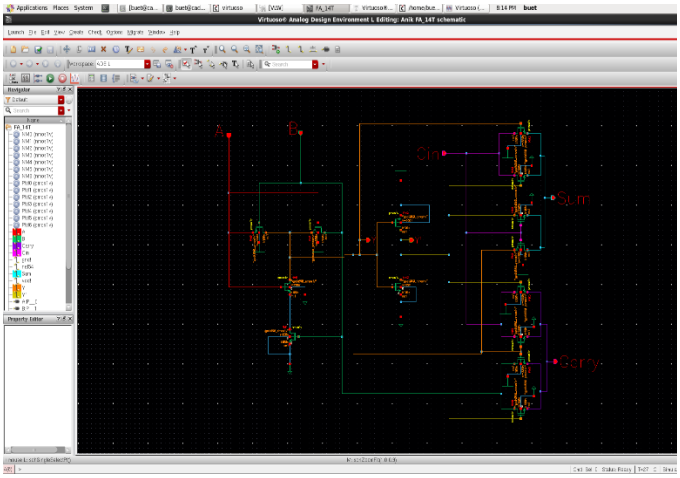


Figure: 14T Full adder

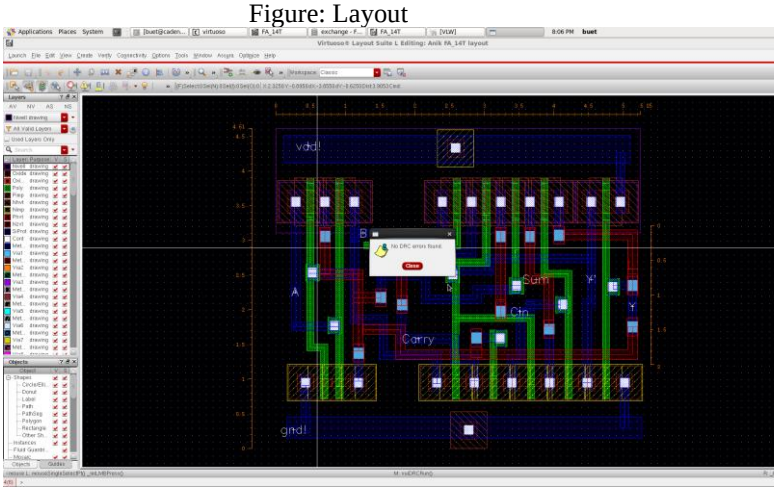


Figure: DRC Error Check

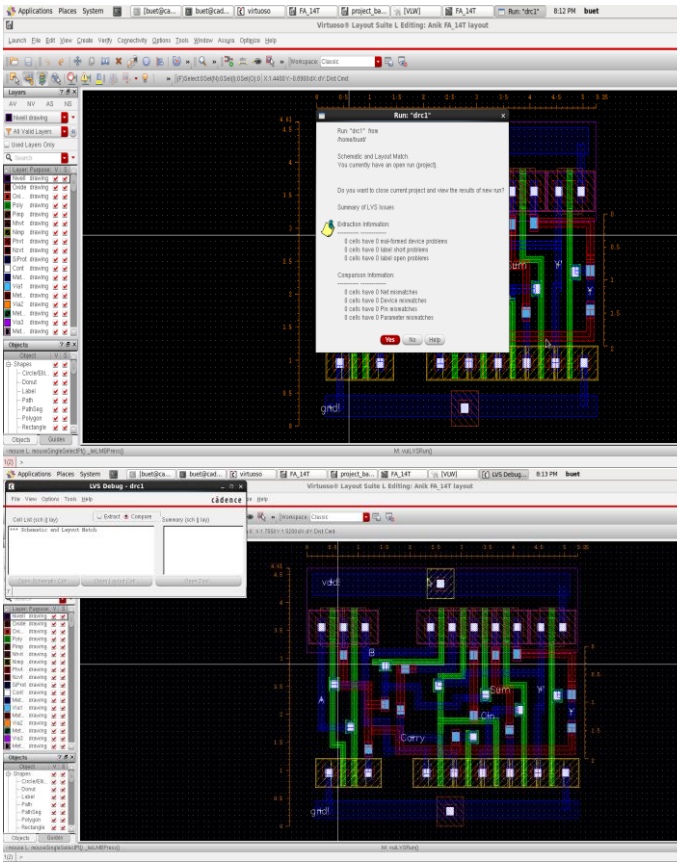


Figure: LVS Error Check

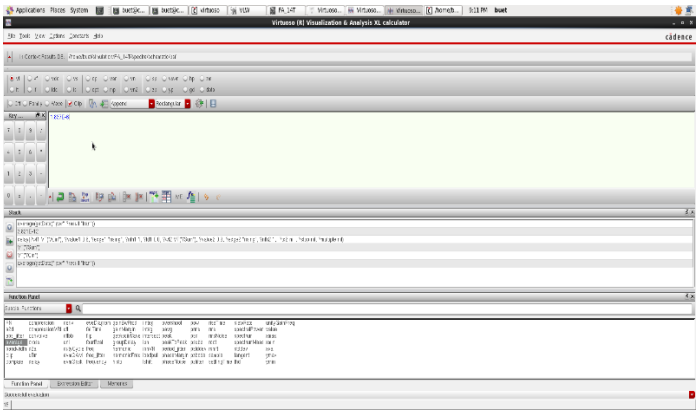


Figure: Average Power.

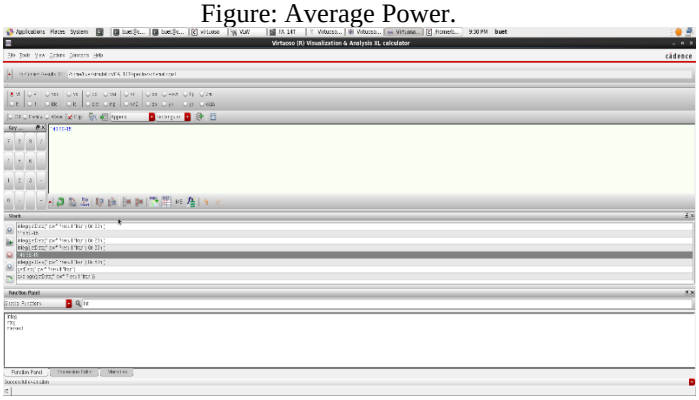


Figure: Energy

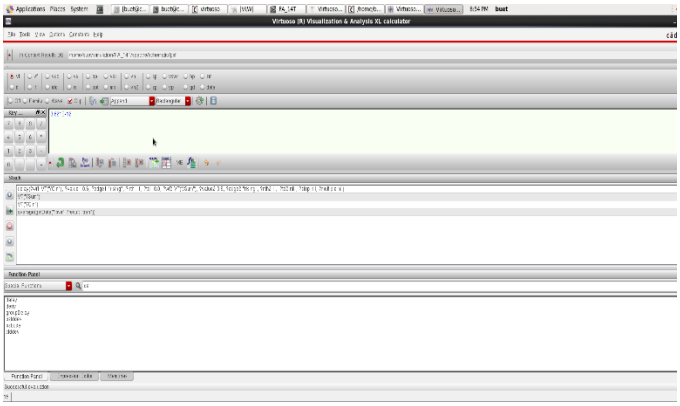
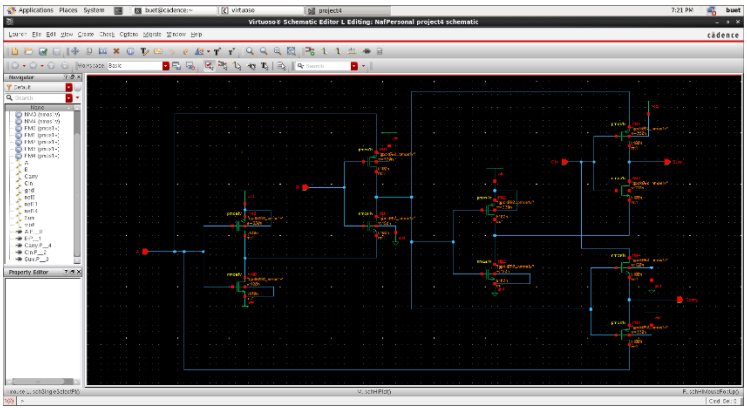


Figure: Propagation Delay.

D. Gate Diffusion Input (GDI) Full Adder (10T).

`Schematic`



`Output`

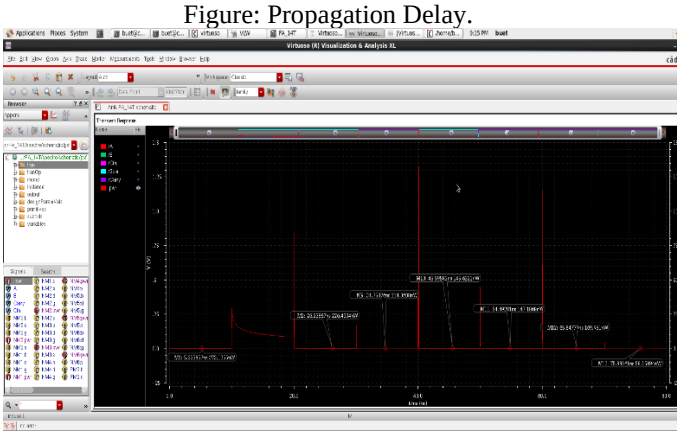
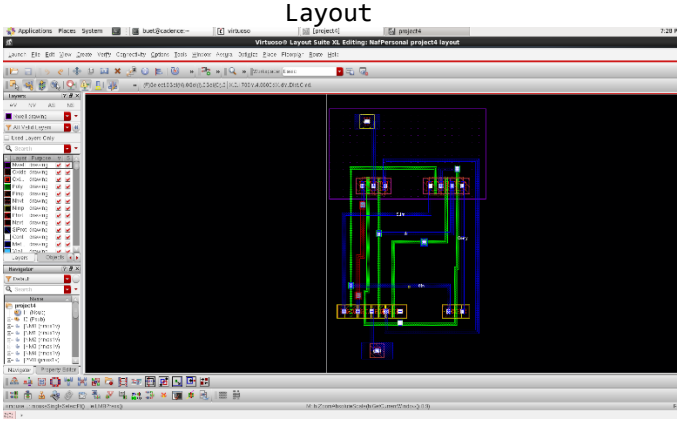
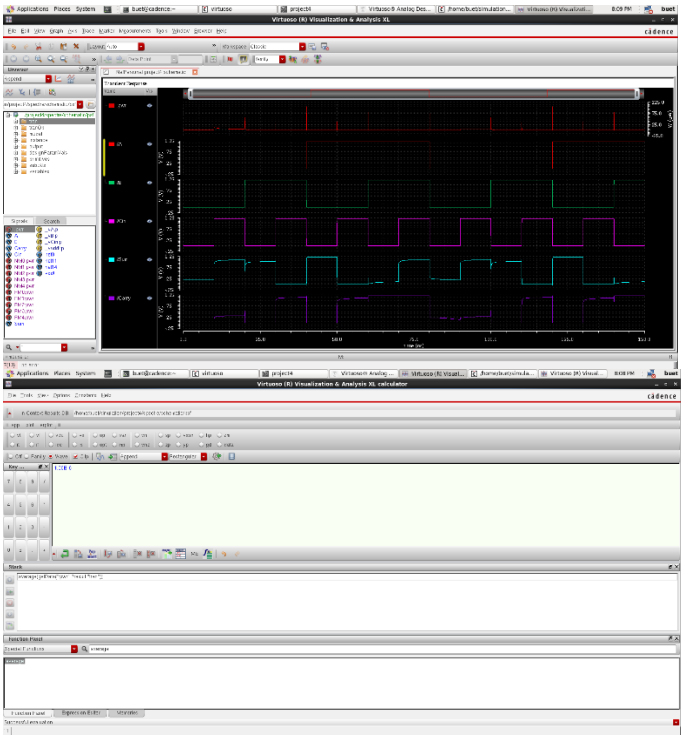


Figure: Power.

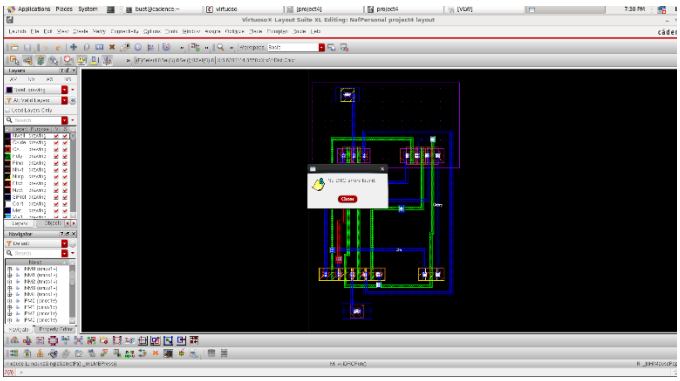
Layout



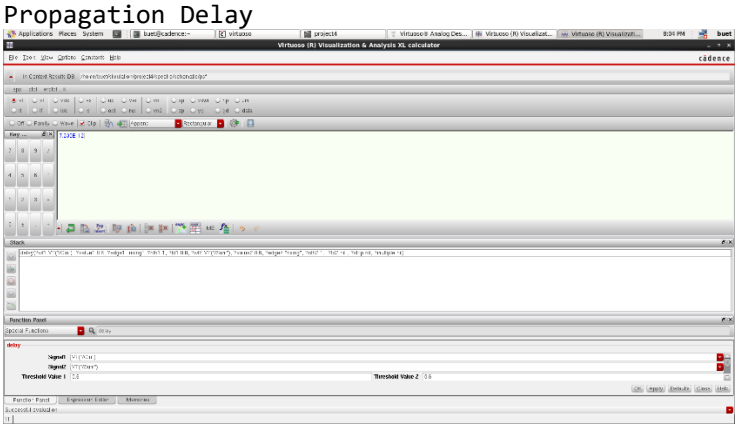
Power



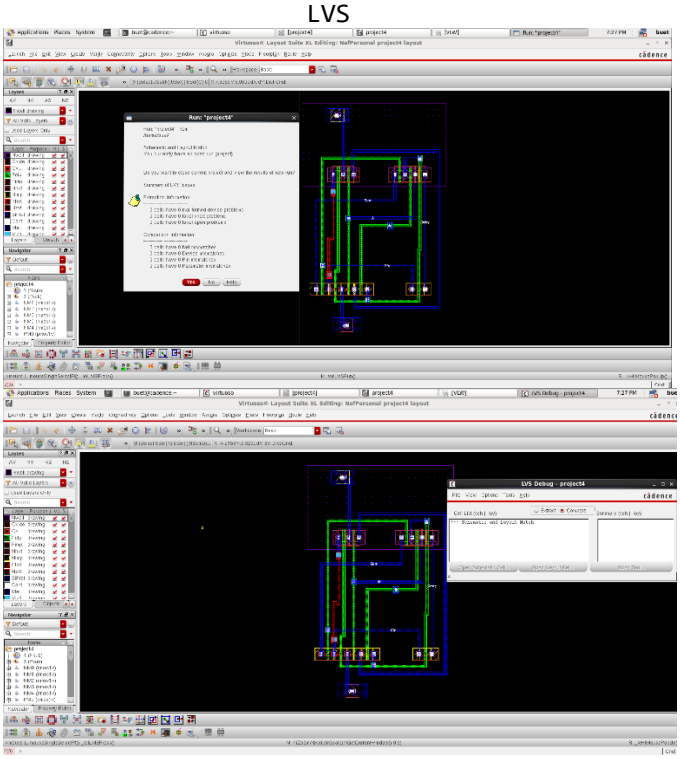
DRC



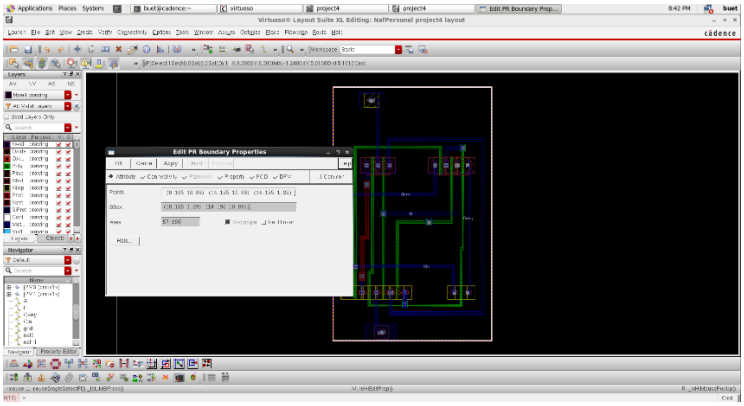
Propagation Delay



LVS



Cell Area



IV. Future Aspects

The articles showcase complete adder designs that mainly concentrate on upcoming enhancements in 0.35µm and 0.18µm technology nodes. To implement and assess novel full adder architectures in more sophisticated process nodes, such as 22nm, 16nm, etc., more study can be done. Lower power consumption and increased speed can be attained by utilizing the performance benefits that come with scaling to smaller geometries. Furthermore, it is possible to investigate hybrid full adder architectures that incorporate many logic approaches. To save power and time, for instance, the XOR-XNOR logic can be implemented using pass transistor logic, and the carry generation can be carried out using transmission gates or GDI approaches. These hybrid strategies might offer improved performance metric tuning.

V. Conclusion:

Our research's primary goal has been to compare several full adders with diverse logic approaches in order to determine which full adder has the most potential for performance. Four full adders were evaluated for performance in this paper: a traditional CMOS full adder with 28 transistors, transmission gate full adder with 20 transistors, a 14 transistor adder employing pass transistor logic, and a 10 transistor GDI based full adder. The designs are made more exact by using Cadence 6.1.6 software to ensure that all design requirements are met. According to the analysis, the transmission gate full adder performed the best out of all of them in terms of latency as determined by transient analysis. However, a 14 transistor full adder performs better when taking

VI. Acknowlodhement

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