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Logic Design with Verilog
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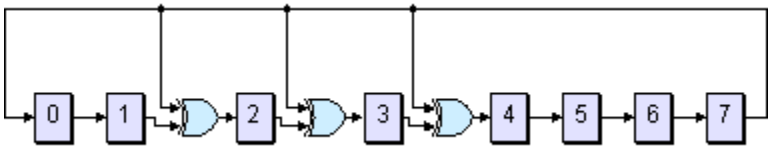
Linear Feedback Shift Registers

LFSRs (Linear Feedback Shift Registers) are frequently used to produce pseudo-random sequences of bits using XOR gates and Flip Flops. LFSRs have low overhead in hardware because they only use XOR gates to generate new bits. Two implementations of an 8-bit LFSR can be found in this folder: one implemented with **structural Verilog** and one implemented with **behavioral Verilog.** Figure 1 depicts the design of the LFSR.



Timing and Resource Analysis: lfsr_8b_behav & lfsr_8b_struc	
Specified clock period	400ns
Worst Negative Slack **WNS**	398.861ns
Minimum clock period **Tmin**	1.139ns
Maximum clock frequency **Fmax**	0.87796 GHz
# look up tables **LUT**	5
# of registers	8

The timing and resource reports for both implementations yielded the same results.