CSSE 232 COMP ARCH 1 JOURNAL

TEAM ORANGE:

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9/27/23: (1 hour) Brainstorm what type of architecture we want. Then we landed on an 8 register design. Possible future problems could be not enough registers. Created all the instructions needed to run the algorithm. Key takeaways: focusing on speed, running Euclid algorithm as fast as possible, ended on Load/Store.

10/4/23: (after meeting): (30 minutes) Made ways to change our project from being a 16 bit RISC-V. Key takeaways: changed all symbols for instructions, rearranged it to rd operation rs1, rs2 (a = b + c type of structure).

10/4/23: (15 minutes) Updated symbols in existing document and found some new ideas and changes nothing major.

10/6/23: (2 hours) Created basic examples of functions. Translated from java type code to assembly to machine code. Key takeaways: still felt like RISC-V maybe find some things to change about it later.

10/8/23: (45 minutes) Changed symbols and instructions in my parts of the document to match new instructions. Key takeaways: now feels like our own project no longer RISC-V in 16 bits.

10/8/23 (3 hours) - Created the RTL path for M-Type (loading and storing memory) instructions and the 2 first base instructions for all types. Then started the table of components. Key takeaways: 2nd step creates 3 arguments from rs1 rs2 and rd for later use due to needing those based on our use of instruction types.

10/11/23 (1 and a half hours) – Edited RTL for implementation of pipeline. Added registers we need for pipelining and split memory. Planned for Milestone 3. I will be taking control of the datapath and planning out the pipelining. Key takeaways: RTL is now mostly set for pipelining, and I will be the main outlook for the pipelining.