Si5350/51 PCB Layout Guide

1. Introduction

The Si5350/51 Any-Frequency Octal CMOS Clock Generator + VCXO are the industry's most frequency flexible, lowest power, lowest jitter programmable clocks targeting cost-sensitive consumer, enterprise and communications applications. The devices can synthesize combinations of 8 unique, non-integer related frequencies up to 160 MHz with 0 ppm frequency error, providing greater frequency flexibility than competing solutions. The Si5350/51 simultaneously generates free-running and synchronous clocks, making it ideal for replacing multiple clock ICs, XOs and VCXOs with a single device. Because the Si5350/51 consolidates clocking to a central location, it is necessary to consider the layout implications. This application note provides layout guidance to ease PCB development with centralized clocking.

2. Topologies

Several layout strategies can be employed when routing CMOS (single-ended) signals. The most common technique is a simple point-to-point connection, but other techniques involve fanout (point-to-multi-point). All topologies rely upon transmission lines (lines long enough, electrically, to have delay from source to receiver).

3. Transmission Lines

For optimized clock signal routing, clock signals should be kept relatively short or treated as transmission lines for longer distances. The connection is considered a transmission line when the line length measured in delay (seconds) is close to the 20–80% rise/fall time of the clock signal. Lines shorter than this metric will settle quickly with little overshoot or undershoot. For the Si5350/51, it is recommended to treat clock signals as transmission lines if the trace distance is greater than 5 cm. As shown in Figure 1, there are multiple industry-standard PCB layout techniques to create a transmission line. For the Si5350/51, microstrip is recommended if dedicated GND planes are available Coplanar microstrip is recommended if dedicated GND planes are not available. Both techniques can be used in the same design to optimize layout.

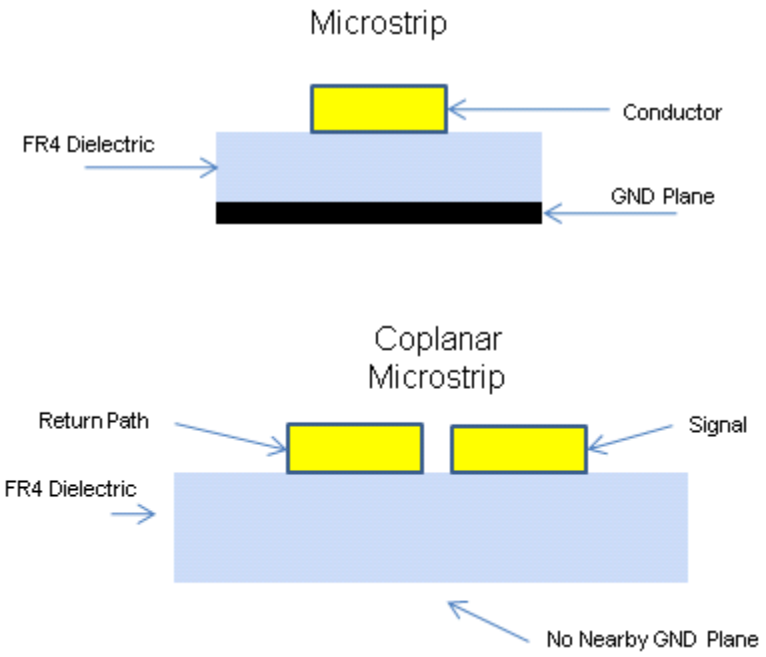

Figure 1. Transmission Lines

A series termination resistor is typically required to terminate CMOS clock signals because most receivers are high dc-impedance (e.g., CMOS gate input). This resistor can either be an external component or integrated within the clock IC. The resistor value is selected to match the transmission line impedance with the characteristic impedance of the clock driver. Matching to ±10% is adequate for clock signals. Ideally, termination resistors are placed near the output driver of the transmitting device, but they may be placed at the receiver or at both ends, depending on the design.

4. Point-to-Point Connections

A point-to-point connection exists when tying one output of the Si5350/51 to a single clock input of another device. The most common input type is a high impedance CMOS input that electrically appears to be a low value capacitor to GND (e.g., 4 pF). The Si5350/51 output buffers have a nominal output impedance in the range of 40 to 65 Ω (approximately 40, 55, and 65 Ω for VDDO = 1.8, 2.5, and 3.3 V, respectively) when set for the highest drive strength setting (CLKx_IDRV = 11). It is recommended that the Si5350/51 output clock traces have a characteristic impedance of 50–60 Ω. When VDDO = 1.8 V, it's also recommended that a 10–20 Ω external series resistor be placed right at the clock output pin in order to match driver output impedance with the characteristic impedance of the clock trace. A standard 10% tolerance resistor will suffice. When VDDO = 2.5 or 3.3 V, no series resistance will be needed as long as the output clock trace characteristic impedance is 50–60 Ω.

Clock signals up to 20 cm in length can be easily routed with excellent signal integrity using this approach. Signals greater than 20 cm may experience reduced amplitude due to other loss mechanisms. Check the input receiver’s VIH and VIL requirements for long clock traces to ensure compatibility.

4.1. Recommendations for Rev A Devices

The Si5350/51 rev A has higher impedance output buffers. Although this serves to optimize while minimizing clock jitter and output-to-output coupling, it does require a higher characteristic trace impedance. When using the Si5350/51 rev A devices, keep in mind that the driver output impedance ranges from 65 to 85 Ω (approximately 65, 75, and 85 Ω with VDDO = 1.8, 2.5, and 3.3 V, respectively)

If transmission line characteristic impedance matches driver output impedance, output clocks do not require external series termination resistors. Add a series resistor for line impedances greater than driver impedance. Select a standard resistor value near to the difference between driver impedance and calculated line impedance. For example, a 120 Ω line would employ a standard 33 Ω external resistor. In these instances, 10% tolerance resistors are acceptable.

5. Point to Multi-Point Connections

A point-to-multi-point connection exists when tying one Si5350/51 output to more than one input. This type of connection is useful in applications that require multiple copies of the same frequency. For example, some applications require multiple 27 MHz crystals to provide reference timing for multiple ICs. Point to multi-point routing can be used to route one Si5350/51 output to each IC’s input receiver, eliminating the need for multiple crystals. Since multiple potential points of failure in the design are replaced with a simple PCB trace, the new solution improves system reliability.

There are two basic methods to implement a point-to-multi-point connection. First, the clock signal can be branched out from a single point in a star fashion to the various receivers. Second, the clock signal can be tapped from a single PCB trace to multiple receivers. The second choice (single line with multiple taps) is preferable for devices with relatively fast rise/fall times (e.g., 1 ns). Make sure to set the line's characteristic impedance between 50 to 60 Ω (between 65 and 90 Ω when using a rev A device). To minimize reflections, each tap should be as short as possible. Achieve short taps by routing the trace through the solder pad of each receiver.

6. Importance of Matching Clock Output Drive and Trace Impedances

As stated earlier, output impedances of the Si5350/51 2.5 V VDDO output driver are 55 and 75 Ω for rev B and rev A devices, respectively. The figures below represent three different matching conditions.

- Figure 2—Rev A device (2.5 V, 75 Ω driver) driving an 80 Ω trace
- Figure 3—Rev B device (2.5 V, 55 Ω driver) driving a 50 Ω trace
- Figure 4—Rev A device (2.5 V, 75 Ω driver) driving a 50 Ω trace

Note that the first two waveforms look ideal, but in the case of the 75 Ω driver into a 50 Ω trace, there is a stair-step at approximately 70% of the positive edge (and about 30% of the negative edge). This is due to reflections caused by the driver-to-trace mismatch. Some amount of reflection is acceptable, but reflection that causes a stair-step in the logic transition zone, as is the case in Figure 4, add to the uncertainty of the transition zone resulting in higher jitter than expected. If jitter is a concern in your application, please follow the impedance matching guidelines in the preceding sections.

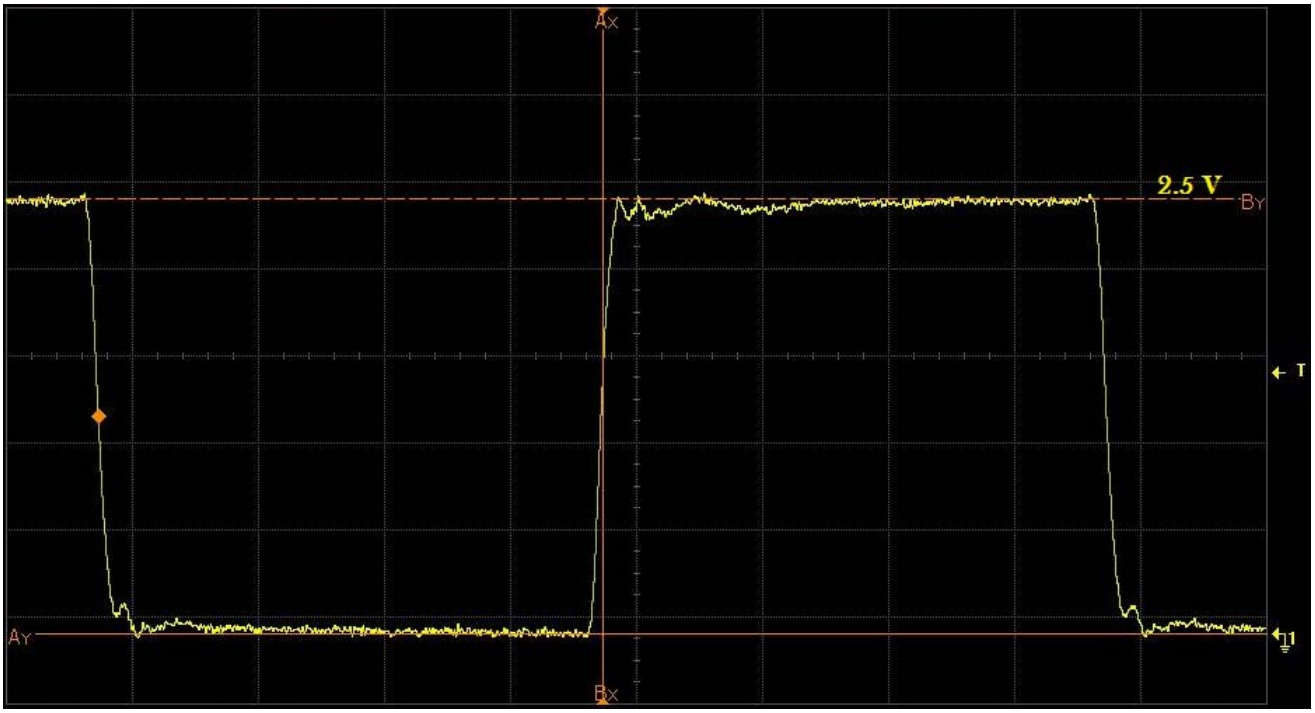

Figure 2. Rev A device (75 Ω Driver) into 80 Ω Trace

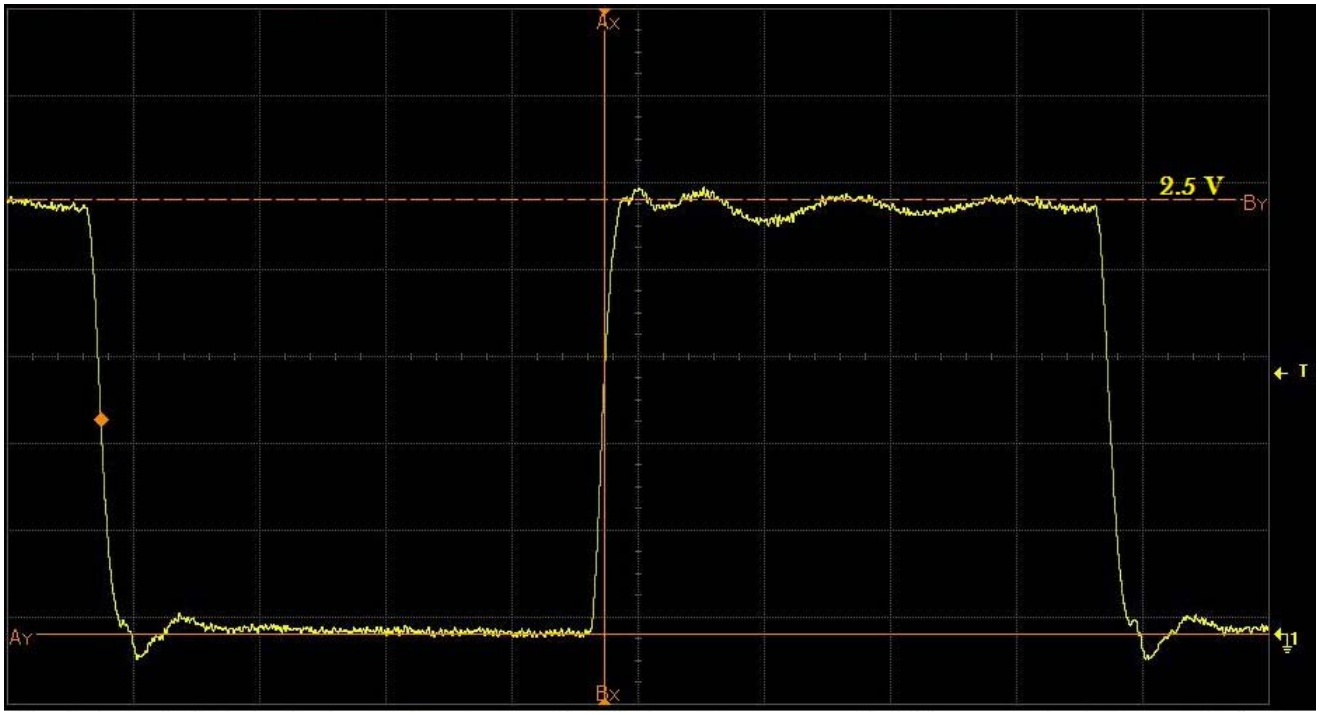

Figure 3. Rev B device (55 Ω Driver) into 50 Ω Trace

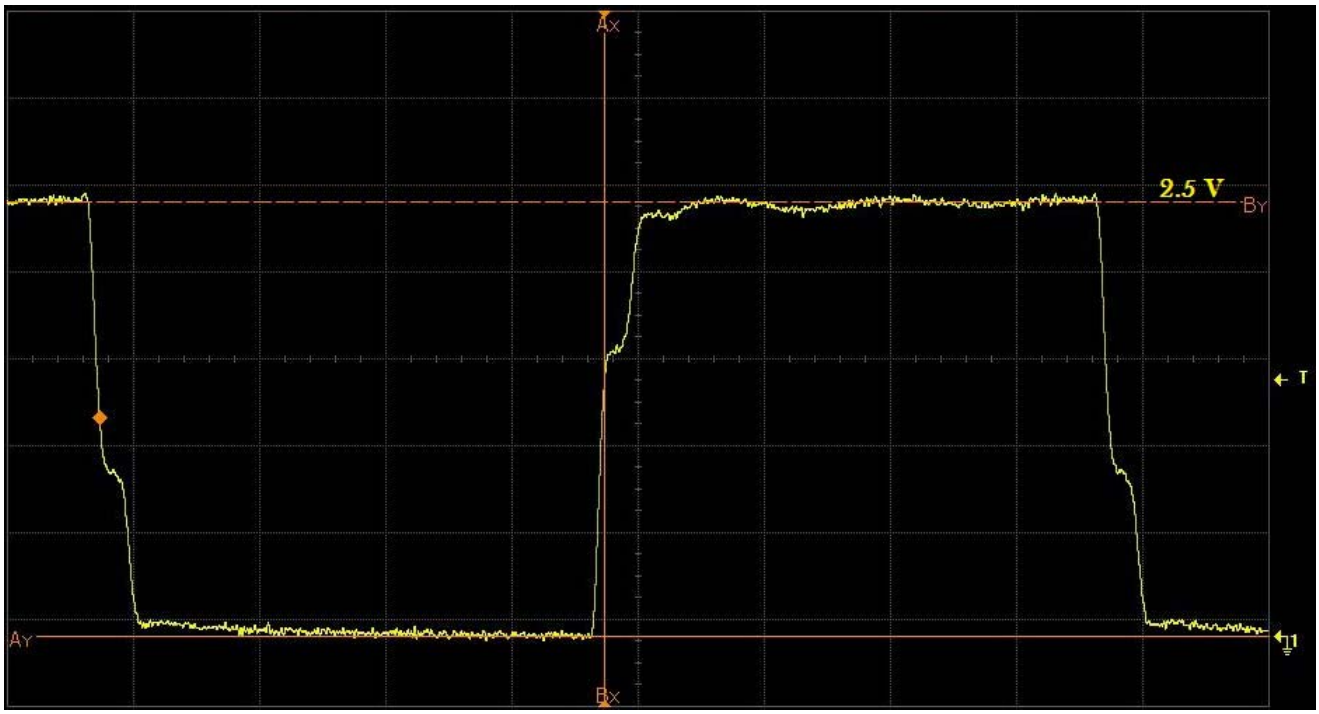

Figure 4. Rev A device (75 Ω Driver) into 50 Ω Trace

7. Minimizing EMI

PCB layout techniques can be used to minimize radiated emissions (EMI). Because voltage requires a reference point, the CMOS clock signal references include both GND and VDD. GND and VDD are at the same potential from an ac perspective when sufficient power-supply bypass-capacitors are used. To minimize EMI, it is necessary to ensure that the clock trace has a known return path along GND or VDD. This return path is formed by running a parallel trace of GND or VDD next to the clock signal using the coplanar microstrip technique described in Figure 1. Alternatively, the parallel return path can be above or below the clock signal trace using the microstrip technique described above.

By maintaining the characteristic impedance along the entire length of the line, the signal is assured to have a known return path and good signal integrity. Characteristic impedance can be determined using textbook formulas, online utilities, or features within the PCB CAD tools. The impedance should be estimated for each PCB layer that the clock signal traverses. Ensure that the return path is not broken or voided since such breaks or voids are the source of EMI.

8. Device Placement

Because signal reflections are associated with transmission line delay, shorter lines are preferred where possible. For the Si5350/51, it is recommended that the highest clock frequencies use the shortest traces when practical. Place the Si5350/51 nearest to the receiver needing the highest rate. This placement also helps reduce EMI by reducing breaks or voids in the GND reference or via discontinuities.

9. Using Phase Offset to Reduce Synchronous Clock Coupling

Adjacent synchronous clocks that are either at the same frequency or integer-related frequencies can couple to each other during rising or falling events. To reduce coupling during these transitions, the phase of each Si5350/51 output clock can be adjusted in relation to the other output clocks to avoid coincident edges. Since the Si5350 is a factory or field-programmed device, these initial phase offsets are set during factory or field programming. With the Si5351 I^2C programmable clock generator, the clock phase of each output can be adjusted in-circuit to reduce coupling and optimize jitter performance.

10. Packaging Requirements

The Si5350/51 comes in a space saving 20-QFN package. The exposed die attach paddle on the bottom efficiently conducts heat to the PCB and provides a stable ground through down bonds or by electrical connections through conductive die attach material. The design of the QFN packages allows for flexibility and enhances electrical performance to very high-speed operating frequencies. In order to obtain peak performance, the board must be designed and the package mounted with consideration. For enhanced thermal, electrical, and performance, the exposed pad on the package must be soldered to the board using a corresponding thermal pad. For proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region. Clearance between the inner row's leads and the thermal pad are required for vias to route the inner row signals. The amount of clearance required depends on the application. It is recommended to incorporate an array of thermal vias at 1.0 mm pitch with via diameters of 0.3 mm (See Figure 5). The number of vias must be determined for each application operating environment and condition.

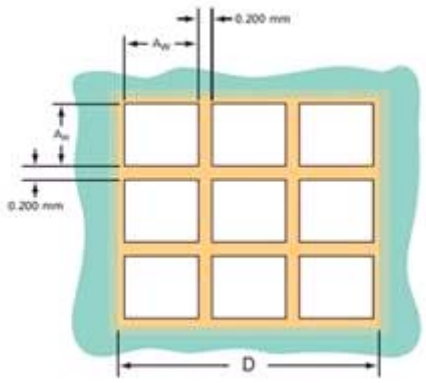

Figure 5. Recommend Ground VIA Pattern

11. Summary

The Si5350/51 is a highly flexible clock generator that can centralize clocking to reduce components and simplify designs. By following the guidelines listed above, designers can maximize the BOM consolidation and minimize their design time. Contact Silicon Labs to consult on any layout questions.

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