CRYSTAL SELECTION GUIDE FOR Si5350/51 DEVICES

1. Introduction

This application note provides general guidelines for the selection and use of crystals for the Si5350/51 Any-Frequency CMOS Clock Generators + VCXO. If the Si5350/51 timing IC is not right for your application, see the many other timing IC products at http://www.silabs.com/products/clocksoscillators/pages/default.aspx. Topics covered include crystal frequency accuracy, VCXO operation, selection, and layout. The equivalent circuit of a crystal and its connection to the Si5350/51 device is shown in Figure 1.

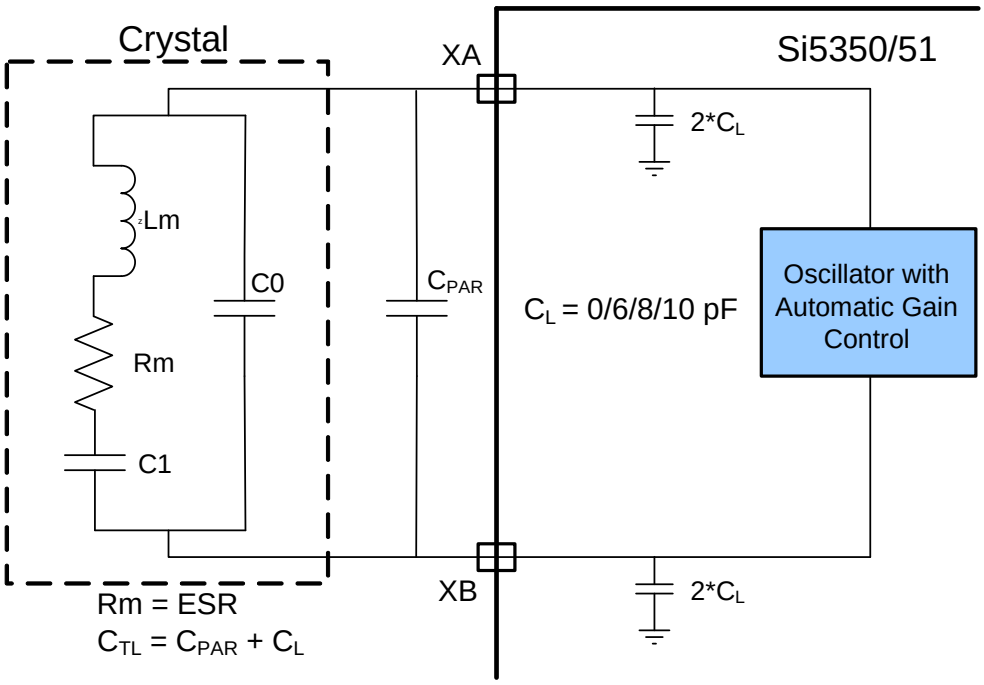

Figure 1. Equivalent Crystal Circuit

The input reference to the Si5350/51 devices can be:

1. Crystal
2. Crystal + analog control voltage (VCXO function)
3. External clock
4. Crystal and External clock

If driven with a crystal input, the devices can operate using either a 25 MHz or 27 MHz crystal. The devices support internal load capacitors, eliminating the need for external capacitors. The Si5350 is a factory- or field-programmable clock generator, and the C_L is factory- or field-programmed to 0, 6, 8, or 10 pF. The Si5351 is an I^2C-programmable clock generator for which the C_L is user-configured via its I^2C interface.

The crystal should be placed as closely to the device as possible to eliminate stray capacitance and ensure optimal device performance. See "5. Crystal Layout Guidelines" on page 5 for more details.

2. Frequency Accuracy

The Si5350/51 output frequency accuracy depends completely upon the accuracy of the input reference clock. When a crystal is the input reference, it is necessary to understand the parameters that affect the crystal oscillation frequency. The frequency accuracy of the crystal oscillator primarily depends on the following parameters:

- Initial accuracy, typically ±20, ±50, or ±100 ppm.
- Variation with temperature. The crystal data sheet should specify the ppm/°C variation.
- Variation with time (aging).
- Crystal load capacitance mismatch.

Crystal load capacitance mismatch is caused by the total load capacitance (C_{TL}) being different from the specified load capacitance (CSPEC) for the crystal. The total load capacitance (C_{TL}) is the sum of the PCB layout capacitance and the capacitance between pins XA and XB of the Si5350/51. If the traces between the crystal and the Si5350/51 are less than 9 mm, it is reasonable to ignore the added capacitance from the PCB traces. The actual oscillation frequency due to the load capacitance mismatch can be calculated as:

$$F_{ACT} = F_{XTAL} \times \left(1 - \frac{C_1}{2} \times \left(\frac{1}{C_0 + C_{SPEC}} - \frac{1}{C_0 + C_{TL}}\right)\right)$$

where:

F_{XTAL} = Design frequency of the crystal

C_{SPEC} = Specified load for the crystal

C_{TL} = Total load seen by the crystal = $C_L + C_{PAR}$

C_0 = Crystal shunt capacitance

C_1 = Crystal motional capacitance

3. VCXO Operation

The Si5350/51 VCXO is an advancement in VCXO technology since it modulates the PLL parameters to create the VCXO function. In contrast, conventional solutions rely on internal varactors (voltage variable capacitors) to tune or pull a crystal's nominal frequency. The Si5350/51's VCXO implementation eliminates the need for higher cost, custom pullable crystals, providing multiple benefits outlined in Table 1.

Table 1. Si5350/51 VCXO Benefits

Conventional Clock VCXOs	Si5350/51 VCXO
Higher cost, custom pullable crystal	Standard, low cost non-pullable crystal
Varactor-based non-linearity limits operating range	High linearity maximizes range: 10–90%VDD
Potential crystal startup issues	Reliable startup and operation
Limited crystal sourcing options	Simplified crystal sourcing
VCXO gain varies with different crystals	No VCXO gain variation with different crystals
No/limited VCXO gain programmability	Very large programmable VCXO gain range*
***Note:** See the Si5350B or Si5351 data sheet for additional information.	

With competing VCXOs, the following crystal parameters must be considered:

1. C0/C1 ratio
2. Max drive level
3. Mechanical third overtone and the location of associated harmonic spurs. This can produce a highly undesirable VCXO linearity curve as shown in Figure 2.

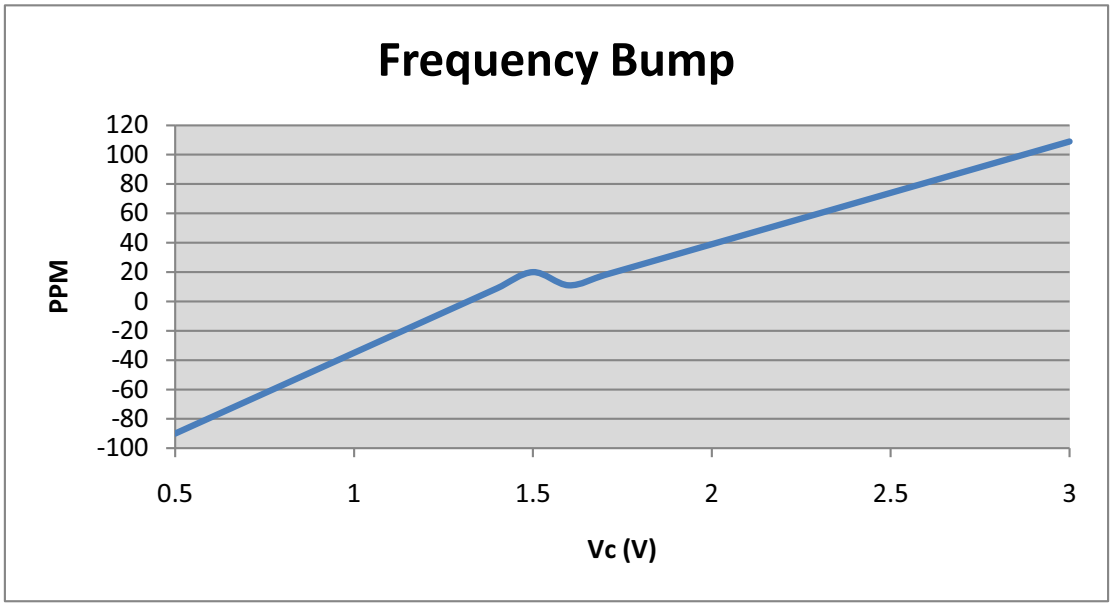

Figure 2. Frequency Bump due to "Pulling" of Crystal

Because the Si5350/51 VCXO function only changes the PLL parameters, the resulting VCXO transfer function is substantially more linear than competing devices which "pull" the crystal. Figure 3 shows the actual measured linearity of the Si5350/51 compared to the competition.

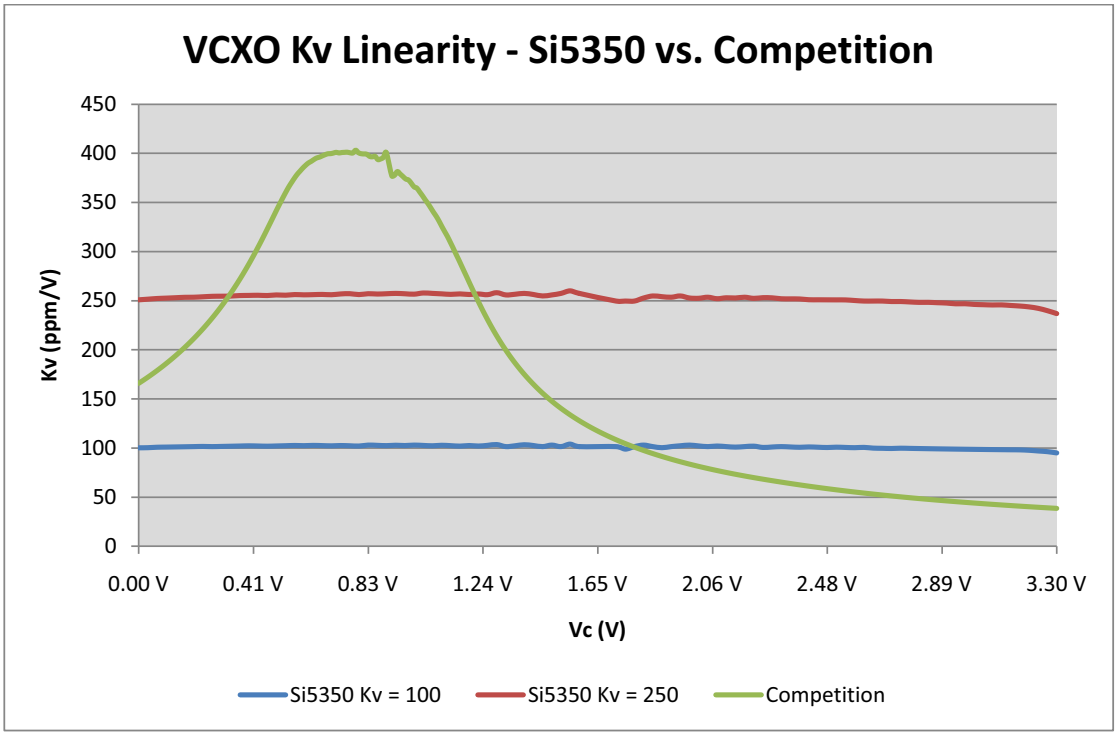

Figure 3. kV Linearity Comparison

4. Crystal Selection

The Si5350/51 is designed to operate with crystals that have a load capacitance (C_L) of 6–12 pF. The Si5350/51 provides a crystal load capacitance that can be set to 0, 6, 8 or 10 pF. A crystal with a load capacitance of up to 12 pF can be used with the Si5350/51 by selecting the 10 pF crystal load setting of the Si5350/51 and adding external capacitors as shown in Figure 4. Choose the crystal load capacitance of the Si5350/51 to be as high as possible but less than or equal to the crystal load capacitance specification. For crystals with load capacitance greater than 12 pF, contact Silicon Labs. Crystals with an HC-49 package are not approved for use with the Si5350/51. Any crystal with an ESR of 150 Ω or less that is in a package of size 5x7 mm or smaller will work with the Si5350/51. ESR for a crystal can be obtained from the crystal data sheet.

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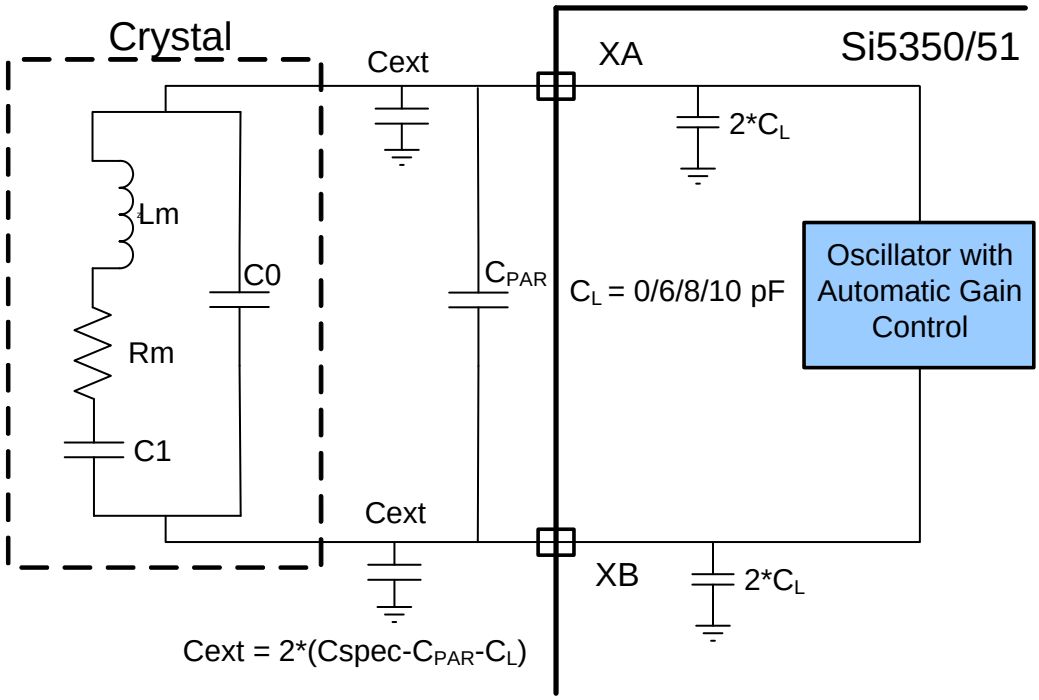

Figure 4. Adding External Crystal Capacitance

Table 2 lists some crystals that can be used with the Si5350/51.

Table 2. Crystals

Mfr	Part Number	Freq	Load Capacitance	Initial Accuracy	Stability over Temp	Web Site
Kyocera	CX3225SB25000D0FLJZ1	25 MHz	8 pF	±10 ppm	±15 ppm	http://global.kyoc-era.com/index.html
	CX3225SB27000D0FLJZ1	27 MHz				
Sunny	SP10115J6-25.000MHz	25 MHz	10 pF	±15 ppm	±30 ppm	http://www.sunny-usa.com/
	SP10115J6-27.000MHz	27 MHz				
NDK	NX3225GA-25.000M-STD-CRG-2	25 MHz	8 pF	±20 ppm	±30 ppm	http://www.ndk.com/en/
	NX3225GA-27.000M-STD-CRG-2	27 MHz				
Epson	FA-238 25.0000MB-K	25 MHz	10 pF	±50 ppm	±30 ppm	http://www.eea.epson.com/
TXC	7M-27.000MEEQ	27 MHz	10 pF	±10 ppm	±10 ppm	http://www.txc.com.tw

5. Crystal Layout Guidelines

Any crystal has the potential to pick up noise from external sources. To minimize this effect and optimize performance, the crystal should be placed as close to the Si5350/51 as possible. Limit trace lengths from the crystal to the Si5350/51 to be less than 9 mm. In addition, EMI effects from other sources of radiated energy, including switching power supplies and signal traces, should be isolated as much as possible from the crystal.

Contact Information

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