LMAC on ZCU102 FPGA Board

ZCU102 is an evaluation board based on ZYNQ® UltraScale+ MPSoC. This document focuses on the implementation of the LeWiz Ethernet MAC (LMAC) on the ZCU102 Board and running the Ping Test to verify the proper functioning.

NOTE: This project is tested on the 'xczu15eg-ffvb1156-2-e' and VIVADO/SDK 2018.2; however, the project given in the release is synthesized for 'xczu9eg-ffvb1156-2-e'.

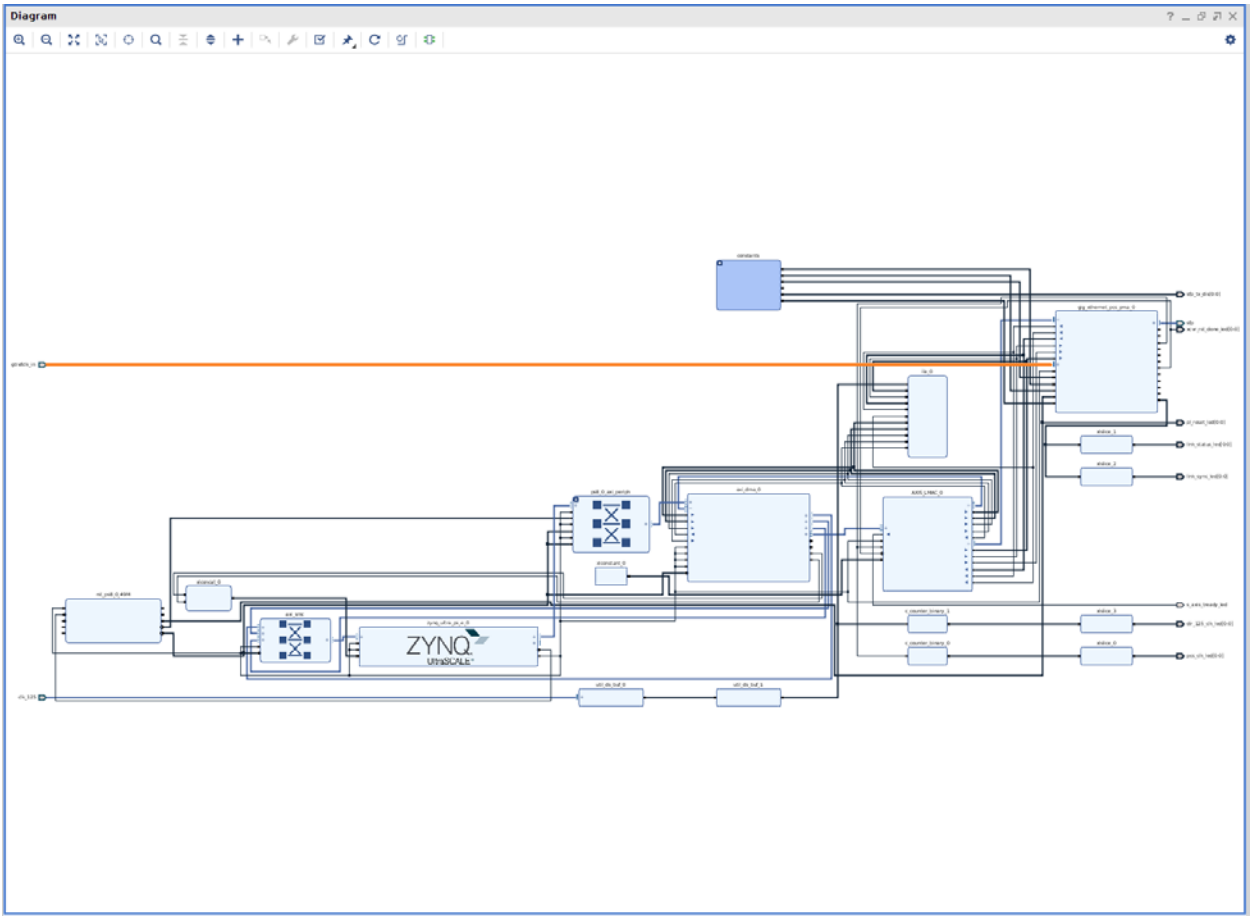

Fig. 1: Block Design

The above figure shows the block design for the project. Main components: ZYNQ ULTRASCALE+ MPSOC, LMAC, AXI DMA, 1G ETHERNET PCS/PMA, ILA and their interconnections.

This project uses Xilinx's Zynq SoC Ultrascale+ FPGA on ZCU102 board with LWIP software as the base. It is intended to show the use of LEWIZ ETHERNET MAC IP CORE-1 with SoC FPGA device and DMA.

The board with LMAC1 was able to connect to the network and ping other systems on the network successfully. All the project files and codes are provided here for the regular ZCU102 board. The synthesis, implementation and bit-stream generation is already done & released here for 'xczu9eg-ffvb1156-2-e' FPGA.

The software provided will test simple ping packets for network compatibility. This software hard coded ping packets with fixed IP and MAC addresses

To modify addresses, go to:

`.../runs_lmac_eth_1g/ps_emio_eth_1g.sdk/hello_world/src/helloworld.c`

In 'helloworld.c':

function: `static int SendPacket(XAxiDma * AxiDmaInstPtr)`

variable: `'temp[0], temp[1], temp[2], temp[3]' which goes to TxPacket []`

For board, ZCU102 (SOURCE) - hard coded for testing

- IP ADDR: 192.168.7.213
- MAC ADDR: 00:12:32:FF:FF:FF //LEWIZ MAC address

For Destination System - hard coded for testing

- IP ADDR: 192.168.7.175
- MAC ADDR: F4:8E:38:B0:2D:02

The ARP Table on the Destination System has to be modified to add the LEWIZ MAC ADDR to the IP ADDR as follows (This will help to generate the PING RESPONSE for correct address):

```
lewiz_175:/usr/sbin$ sudo arp -an
? (192.168.7.213) at <incomplete> on enp1s0
lewiz_175:/usr/sbin$ sudo arp -s 192.168.7.213 00:12:32:ff:ff:ff
lewiz_175:/usr/sbin$ sudo arp -an
? (192.168.7.213) at 00:12:32:ff:ff:ff [ether] PERM on enp1s0
```

The steps below will only work after above configurations are done properly:

- Open Vivado, load the project file:
  `.../runs_lmac_eth_1g/ps_emio_eth_1g.xpr`
- Bit-stream is already generated and exported in the SDK Directory for the 'xczu9eg-ffvb1156-2-e'.
- In vivado, goto: `File -> Launch SDK`
- Once the SDK finishes loading the hardware files, build project 'hello_world'.
- Then program the FPGA.
- Then right click on 'hello_world' click:
  `Run -> Launch on Hardware (System Debugger)`

The included file 'putty.txt' contains the serial output from the FPGA Board. The packets displayed there are the transmitted and received packets on the DMA side.

As you run the test in your network, you should capture the packets on the Destination Node to see the packets transmitted and received.