
数字世界精彩无限

Unit 5

——Multi-Level Gate Circuits
NAND and NOR Gates

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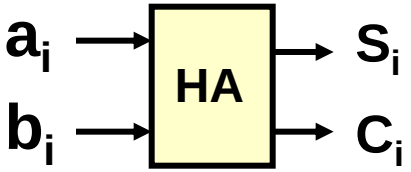
5.5 几种典型的组合逻辑部件_加法器

- 半加器
- 全加器

半加器（Half adder）

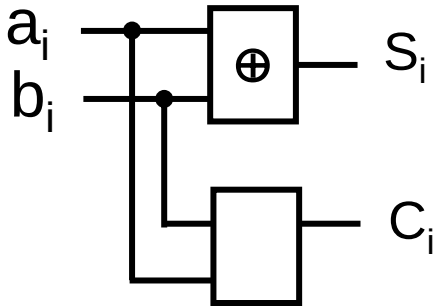
功能：对两个1位二进制数执行相加运算



$$\begin{cases} S_i = a_i \oplus b_i \\ C_i = a_i b_i \end{cases}$$

真值表

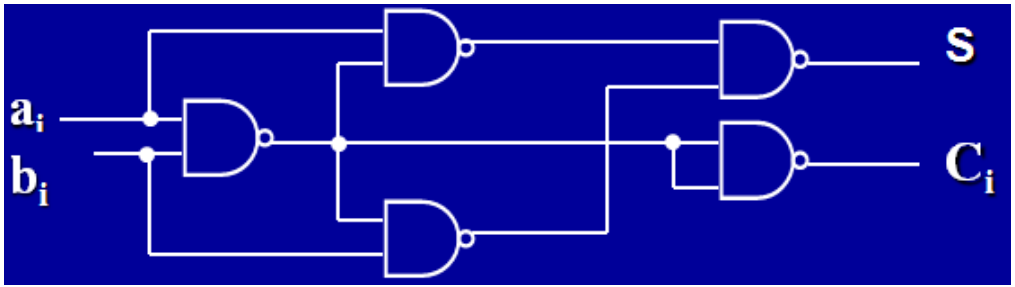
a_i	b_i	S_i	C_i
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



半加器（Half adder）

利用单一逻辑门与非门实现半加器

$$
\begin{cases}
S_i = \bar{a}_i b_i + a_i \bar{b}_i = \bar{a}_i b_i + a_i \bar{b}_i + \bar{a}_i a_i + \bar{b}_i b_i \\
\quad = a_i (\bar{a}_i + \bar{b}_i) + b_i (\bar{a}_i + \bar{b}_i) = a_i \overline{a_i b_i} + b_i \overline{a_i b_i} \\
\quad = \overline{a_i \overline{a_i b_i}} \ \overline{b_i \overline{a_i b_i}} \\
C_i = \overline{a_i b_i}
\end{cases}
$$



全加器（Full adder）

1 0 1 1 …… A

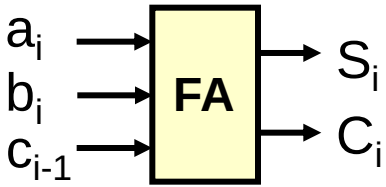
1 1 1 0 …… B

\+ 0 ……C_{i-1}

…… S_i

$A = a_3\, a_2\, a_1\, a_0 = 1011$

$B = b_3\, b_2\, b_1\, b_0 = 1110$



真值表

a_i	b_i	C_{i-1}	S_i	C_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

全加器（Full adder）

真值表

a_i	b_i	C_{i-1}	S_i	C_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S_i

a_i \ b_ic_{i-1}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

C_i

a_i \ b_ic_{i-1}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

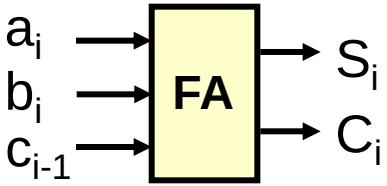
$$S_i = \bar{a}_i\bar{b}_ic_{i-1} + \bar{a}_ib_i\bar{c}_{i-1} + a_i\bar{b}_i\bar{c}_{i-1} + a_ib_ic_{i-1}$$
$$=(\bar{a}_i\bar{b}_i + a_ib_i)c_{i-1} + (\bar{a}_ib_i + a_i\bar{b}_i)\bar{c}_{i-1}$$
$$=\overline{(a_i \oplus b_i)}\,c_{i-1} + (a_i \oplus b_i)\bar{c}_{i-1}$$
$$= a_i \oplus b_i \oplus C_{i-1}$$

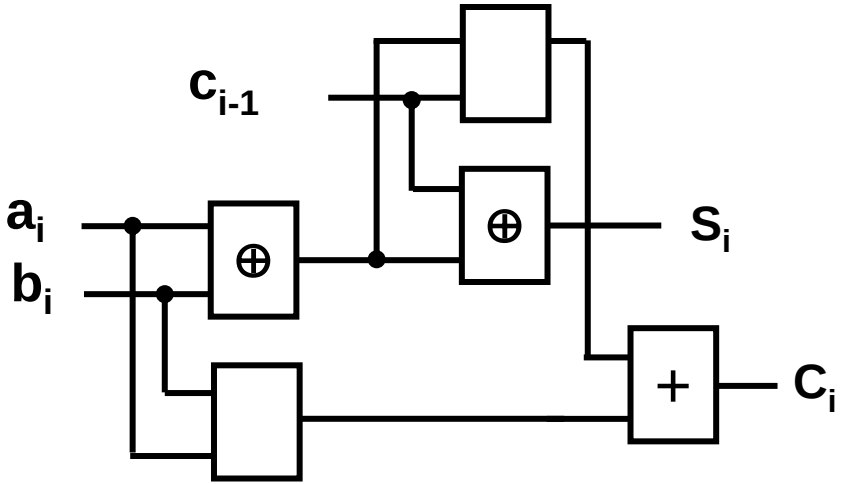
$$C_i=(a_i \oplus b_i)C_{i-1} + a_ib_i$$

全加器（Full adder）

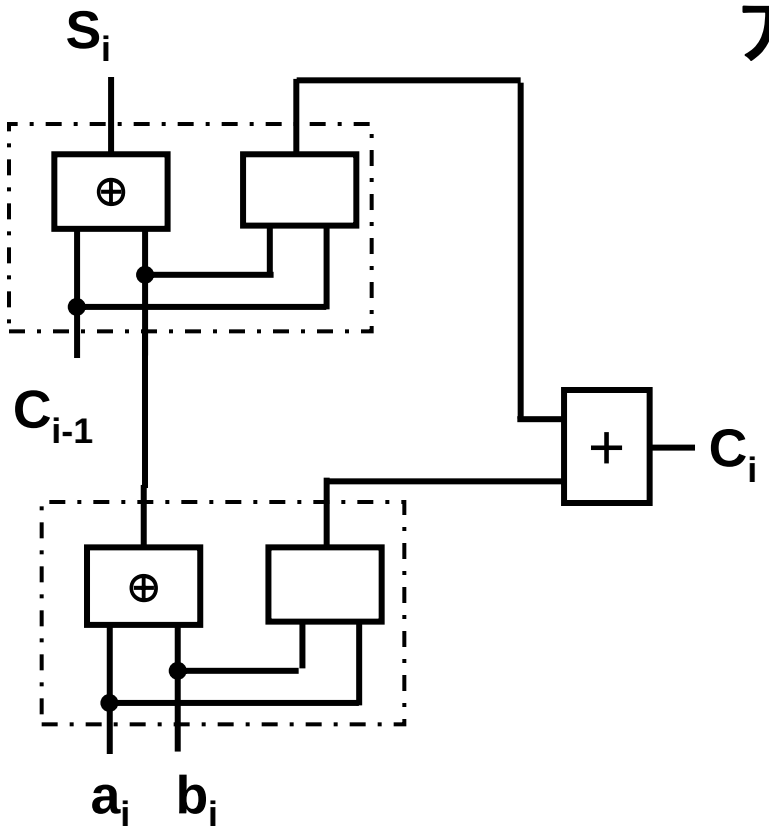
方案 1：

$$\begin{cases} S_i = a_i \oplus b_i \oplus C_{i-1} \\ C_i=(a_i \oplus b_i)\, C_{i-1} + a_i b_i \end{cases}$$





全加器（Full adder）



方案2：

$$\begin{cases} S_i = a_i \oplus b_i \oplus C_{i-1} \\ C_i=(a_i \oplus b_i)\, C_{i-1} + a_i b_i \end{cases}$$

$$\begin{cases} S_i = a_i \oplus b_i \\ C_i= a_i b_i \end{cases}$$

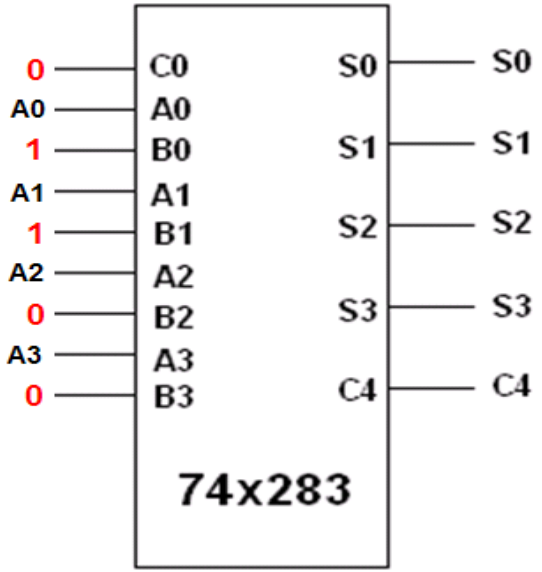
全加器（Full adder）

典型芯片

- **74LS82：** 2-bit adder
- **74LS283：** 4-bit adder

二进制数 $A_3A_2A_1A_0$	余三码 $S_3S_2S_1S_0$	二进制数 $A_3A_2A_1A_0$	余三码 $S_3S_2S_1S_0$
0 0 0 0	0 0 1 1	1 0 0 0	1 0 1 1
0 0 0 1	0 1 0 0	1 0 0 1	1 1 0 0
0 0 1 0	0 1 0 1	1 0 1 0	×
0 0 1 1	0 1 1 0	1 0 1 1	×
0 1 0 0	0 1 1 1	1 1 0 0	×
0 1 0 1	1 0 0 0	1 1 0 1	×
0 1 1 0	1 0 0 1	1 1 1 0	×
0 1 1 1	1 0 1 0	1 1 1 1	×

应用——余3码产生器



$A_3A_2A_1A_0$: 输入 8421 BCD码

$S_3S_2S_1S_0$: 输出余3 码

S = A+0011

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