Unit 12

——Asynchronous sequential circuit design

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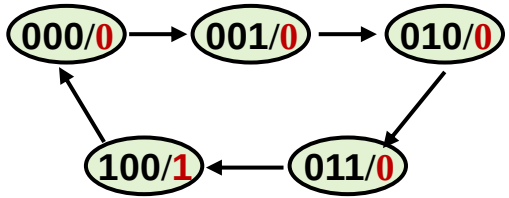
利用触发器设计异步计数器

例1：试用JK触发器设计异步模5加法计数器

① 确定触发器个数：需要3个JK触发器，↓触发

② 画状态转换图



③ 确定触发器CP的接法

CP	Q_3	Q_2	Q_1
↓	0	0	0
↓	0	0	1
↓	0	1	0
↓	0	1	1
↓	1	0	0
↓	0	0	0

设计原则

- 时序图中，凡是触发器状态翻转的地方，都必须为其提供时钟脉冲。
- 在满足翻转的前提下，时钟脉冲越少越好

对触发器而言：只要提供时钟，状态的保持就必须依靠输入端（如J、K）的控制来实现。

Q_1——由CP提供下降沿，CP_1 =CP

Q_2——翻转两次，需两个下降沿，恰好此时Q_1有两个下降沿，CP_2 = Q_1 ↓

Q_3——翻转两次，需两个下降沿，此时Q_2、Q_1都不能提供，CP_3只能接CP

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④ 状态转换真值表

$CP_1 = CP_3 = CP \downarrow$, $CP_2 = Q_1 \downarrow$

确定J_3K_3：看$Q_3^n \rightarrow Q_3^{n+1}$
确定J_1K_1：看$Q_1^n \rightarrow Q_1^{n+1}$

现态			次态			输入						输出
Q_3^n	Q_2^n	Q_1^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}	J_3	K_3	J_2	K_2	J_1	K_1	Z
0	0	0	0	0	1	0	X	X	X	1	X	0
0	0	1	0	1	0	0	X	1	X	X	1	0
0	1	0	0	1	1	0	X	X	X	1	X	0
0	1	1	1	0	0	1	X	X	1	X	1	0
1	0	0	0	0	0	X	1	X	X	0	X	1

此时Q_1无下降沿，J_2 K_2为任意

确定J_2K_2：
看$Q_1^n \rightarrow Q_1^{n+1}$

$$\begin{cases} J_3 = Q_2^n Q_1^n \text{ , } K_3 = 1 \\ J_2 = 1 \text{ , } K_2 = 1 \\ J_1 = \overline{Q}_3^n \text{ , } K_1 = 1 \\ Z = Q_3^n \quad \text{,} CP_2 = Q_1 \downarrow \quad \text{,} CP_3 = CP_1 = CP \end{cases}$$

⑤ 卡诺图化简

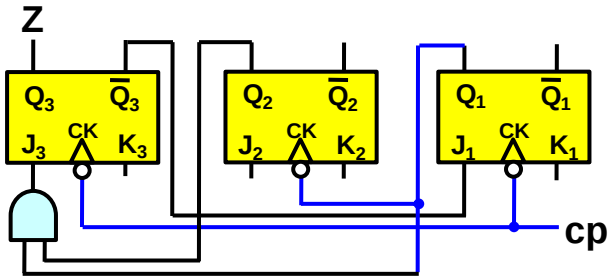
Q_3^n \ $Q_2^nQ_1^n$	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_3 = Q_2^n Q_1^n$

Q_3^n \ $Q_2^nQ_1^n$	00	01	11	10
0	1	X	X	1
1	0	X	X	X

$J_1 = \overline{Q}_3^n$

⑥ 逻辑图



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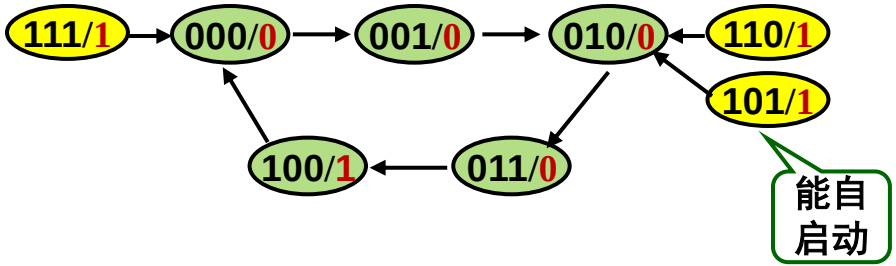
⑦检查无关项

现态			次态			输入			输出
Q_3^n	Q_2^n	Q_1^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}	CP_3	CP_2	CP_1	Z
1	0	1	0	1	0	↓	↓	↓	1
1	1	0	0	1	0	↓	0	↓	1
1	1	1	0	0	0	↓	↓	↓	1

$$\begin{cases} J_3 = Q_2^n Q_1^n \ , K_3 = 1 \\ J_2 = 1 \ , K_2 = 1 \\ J_1 = \overline{Q}_3^n , K_1 = 1 \\ Z = Q_3^n \quad , CP_2 = Q_1 \downarrow \quad , CP_3 = CP_1 = CP \end{cases}$$



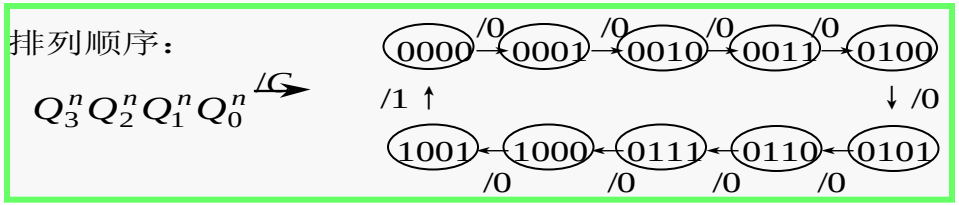
利用触发器设计异步计数器

例2：用*D*触发器设计实现十进制异步加法计数器

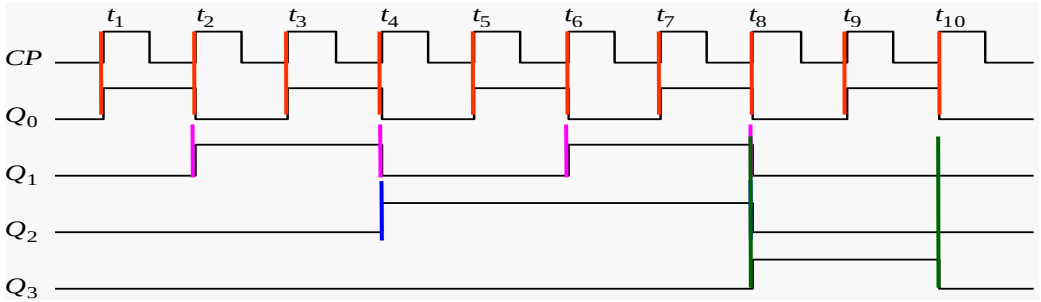
① 确定触发器个数：需要4个D触发器，↑触发

② 画状态转换图

输出方程：$C = Q_3^n Q_0^n$



③ 确定触发器CP的接法



$$\begin{cases} CP_0 = CP \\ CP_1 = \overline{Q_0} \\ CP_2 = \overline{Q_1} \\ CP_3 = \overline{Q_0} \end{cases}$$

选择时钟脉冲的基本原则：在满足翻转要求的条件下，触发沿越少越好。

利用触发器设计异步计数器

④ 状态转换真值表

$$\begin{cases} CP_0 = CP \\ CP_1 = \overline{Q_0} \\ CP_2 = \overline{Q_1} \\ CP_3 = \overline{Q_0} \end{cases}$$

现态				次态				输入							
Q_3^n	Q_2^n	Q_1^n	Q_0^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	CP_3	CP_2	CP_1	CP_0	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	1	0	0	0	↑	X	X	X	1
0	0	0	1	0	0	1	0	↑	0	↑	↑	0	X	1	0
0	0	1	0	0	0	1	1	0	0	0	↑	X	X	X	1
0	0	1	1	0	1	0	0	↑	↑	↑	↑	0	1	0	0
0	1	0	0	0	1	0	1	0	0	0	↑	X	X	X	1
0	1	0	1	0	1	1	0	↑	0	↑	↑	0	X	1	0
0	1	1	0	0	1	1	1	0	0	0	↑	X	X	X	1
0	1	1	1	1	0	0	0	↑	↑	↑	↑	1	0	0	0
1	0	0	0	1	0	0	1	0	0	0	↑	X	X	X	1
1	0	0	1	0	0	0	0	↑	0	↑	↑	0	X	0	0

⑤ 卡诺图化简

$Q_3^nQ_2^n$ \ $Q_1^nQ_0^n$	00	01	11	10
00	X	0	0	X
01	X	0	1	X
11	X	X	X	X
10	X	0	X	X

$D_3 = Q_2^nQ_1^n$

$Q_3^nQ_2^n$ \ $Q_1^nQ_0^n$	00	01	11	10
00	X	X	1	X
01	X	X	0	X
11	X	X	X	X
10	X	X	X	X

$D_2 = \overline{Q_2}^n$

$Q_3^nQ_2^n$ \ $Q_1^nQ_0^n$	00	01	11	10
00	X	1	0	X
01	X	1	0	X
11	X	X	X	X
10	X	0	X	X

$D_1 = \overline{Q_3}^n\,\overline{Q_1}^n$

$Q_3^nQ_2^n$ \ $Q_1^nQ_0^n$	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

$D_0 = \overline{Q_0}^n$

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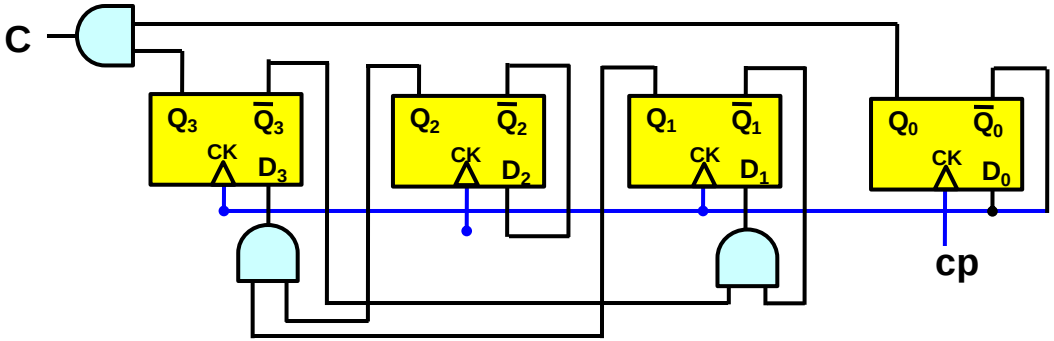
⑥ 逻辑图



$$\begin{cases} CP_0 = CP \\ CP_1 = \overline{Q}_0 \\ CP_2 = \overline{Q}_1 \\ CP_3 = \overline{Q}_0 \end{cases} \qquad \begin{cases} D_3 = Q_2^n Q_1^n \\ D_2 = \overline{Q}_2^n \\ D_1 = \overline{Q}_3^n \, \overline{Q}_1^n \\ D_0 = \overline{Q}_0^n \\ C = Q_3^n Q_0^n \end{cases}$$

⑦检查无关项

将无效状态1010～1111分别代入状态方程,可以验证该电路能够自启动。

现态				次态				输入			
Q_3^n	Q_2^n	Q_1^n	Q_0^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	CP_3	CP_2	CP_1	CP_0
1	0	1	0	0	0	0	1	0	0	0	↑
1	0	1	1	0	1	0	0	↑	↑	↑	↑
1	1	0	0	1	1	0	1	0	0	0	↑
1	1	0	1	0	1	0	0	↑	0	↑	↑
1	1	1	0	1	1	1	1	0	0	0	↑
1	1	1	1	0	0	0	0	↑	↑	↑	↑