Unit 13

——Programmable Logic Devices

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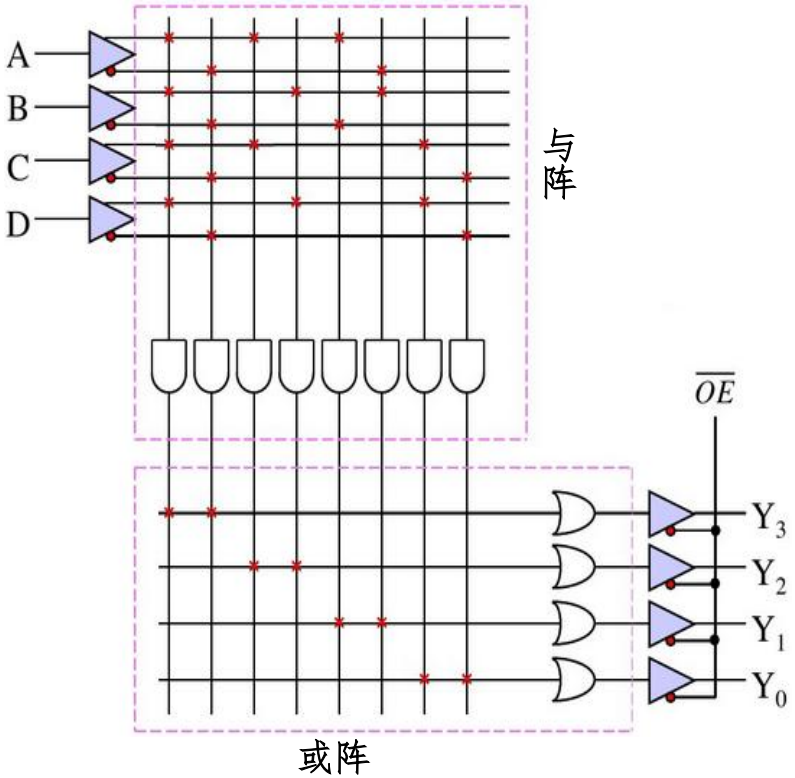
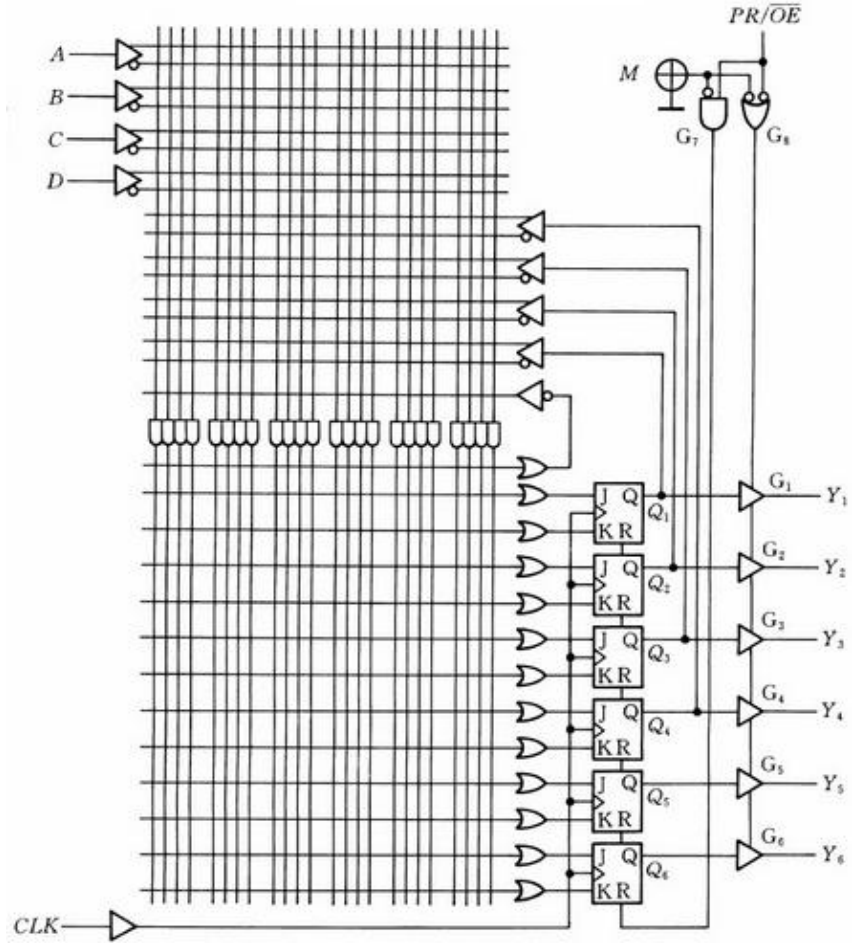
组合型FPLA



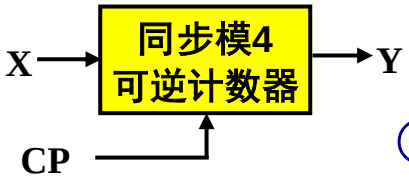
时序型FPLA



Example

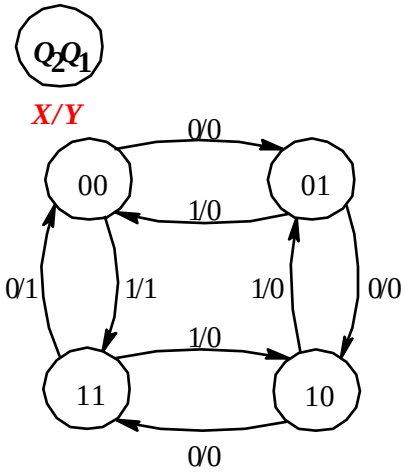
PLA及其应用

例4：利用PLA设计2位二进制同步可逆计数器，假设PLA中是JK触发器.



X=0:加法；X=1:减法；
Y: 进位（借位）

① state graph

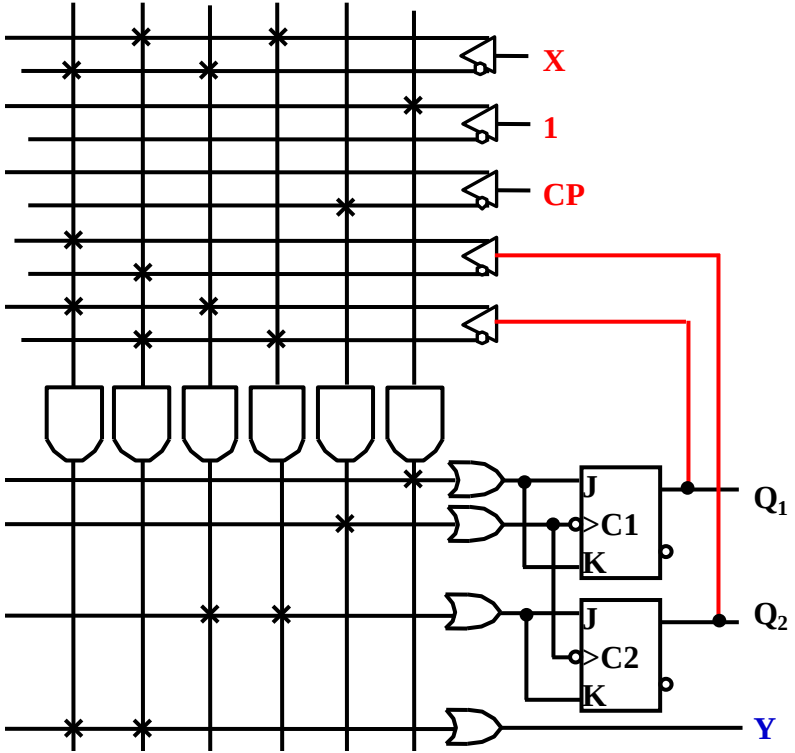


② transition table

X	Q_2^n	Q_1^n	Q_2^{n+1}	Q_1^{n+1}	Y
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	1	0
1	1	1	1	0	0

$$\begin{cases} J_1 = K_1 = 1 \\ J_2 = K_2 = X\overline{Q}_1^n + \overline{X}Q_1^n \end{cases}$$

③ Realize



Example

PLA及其应用

例5：利用PLA设计模12计数器，并在七段数码管上显示计数值， 假设PLA中是 JK触发器。

① 设计模12计数器

$y_4 y_3 y_2 y_1$	$y_4^{n+1} y_3^{n+1} y_2^{n+1} y_1^{n+1}$	$J_4 K_4$	$J_3 K_3$	$J_2 K_2$	$J_1 K_1$
0 0 0 0	0 0 0 1	0 ×	0 ×	0 ×	1 ×
0 0 0 1	0 0 1 0	0 ×	0 ×	1 ×	× 1
0 0 1 0	0 0 1 1	0 ×	0 ×	× 0	1 ×
0 0 1 1	0 1 0 0	0 ×	1 ×	× 1	× 1
0 1 0 0	0 1 0 1	0 ×	× 0	0 ×	1 ×
0 1 0 1	0 1 1 0	0 ×	× 0	1 ×	× 1
0 1 1 0	0 1 1 1	0 ×	× 0	× 0	1 ×
0 1 1 1	1 0 0 0	1 ×	× 1	× 1	× 1
1 0 0 0	1 0 0 1	× 0	0 ×	0 ×	1 ×
1 0 0 1	1 0 1 0	× 0	0 ×	1 ×	× 1
1 0 1 0	1 0 1 1	× 0	0 ×	× 0	1 ×
1 0 1 1	0 0 0 0	0 ×	1 ×	× 1	× 1

J_4

y_4y_3 \ y_2y_1	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	×	×	×	×
10	×	×	×	×

K_4

y_4y_3 \ y_2y_1	00	01	11	10
00	×	×	×	×
01	×	×	×	×
11	×	×	×	×
10	0	0	1	0

J_3

y_4y_3 \ y_2y_1	00	01	11	10
00	0	0	1	0
01	×	×	×	×
11	×	×	×	×
10	0	0	0	0

K_3

y_4y_3 \ y_2y_1	00	01	11	10
00	×	×	×	×
01	0	0	1	0
11	×	×	×	×
10	×	×	×	×

$$\begin{cases} J_4 = y_3y_2y_1 \\ K_4 = y_2y_1 \end{cases}$$

J_2

y_4y_3 \ y_2y_1	00	01	11	10
00	0	1	×	×
01	0	1	×	×
11	×	×	×	×
10	0	1	×	×

K_2

y_4y_3 \ y_2y_1	00	01	11	10
00	×	×	1	0
01	×	×	1	0
11	×	×	×	×
10	×	×	1	0

$$\begin{cases} J_3 = \overline{y}_4y_2y_1 \\ K_3 = y_2y_1 \end{cases}$$

J_1

y_4y_3 \ y_2y_1	00	01	11	10
00	1	×	×	1
01	1	×	×	1
11	×	×	×	×
10	1	×	×	1

K_1

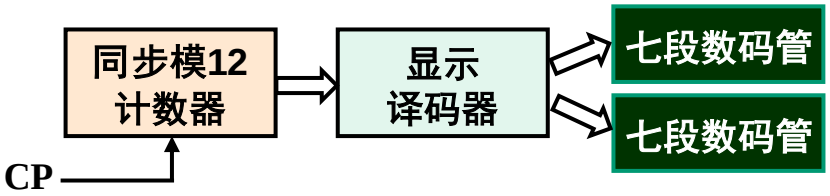
y_4y_3 \ y_2y_1	00	01	11	10
00	×	1	1	×
01	×	1	1	×
11	×	×	×	×
10	×	1	1	×

$$\begin{cases} J_2 = y_1 \\ K_2 = y_1 \end{cases}$$

$$\begin{cases} J_1 = 1 \\ K_1 = 1 \end{cases}$$

PLA及其应用

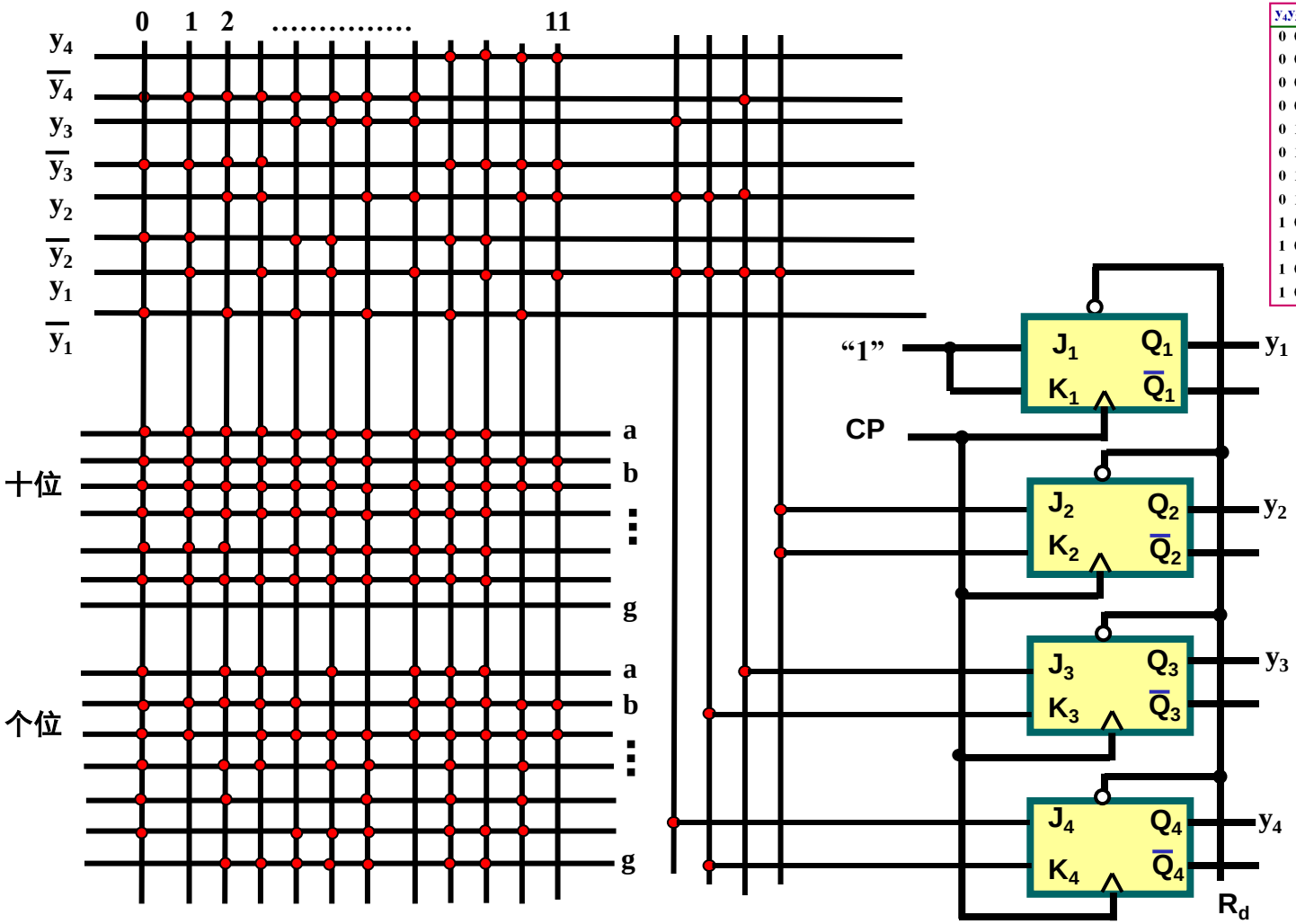
② 设计显示译码器



译码器输入：4位，来自模12计数器

译码器输出：14位，驱动两个7段数码管

	十位			个位	
$y_4y_3\,y_2y_1$	a b c d e f g		$y_4y_3\,y_2y_1$	a b c d e f g	
0 0 0 0	1 1 1 1 1 1 0	0	0 0 0 0	1 1 1 1 1 1 0	0
0 0 0 1	1 1 1 1 1 1 0	0	0 0 0 1	0 1 1 0 0 0 0	1
0 0 1 0	1 1 1 1 1 1 0	0	0 0 1 0	1 1 0 1 1 0 1	2
0 0 1 1	1 1 1 1 1 1 0	0	0 0 1 1	1 1 1 1 0 0 1	3
0 1 0 0	1 1 1 1 1 1 0	0	0 1 0 0	0 1 1 0 0 1 1	4
0 1 0 1	1 1 1 1 1 1 0	0	0 1 0 1	1 0 1 1 0 1 1	5
0 1 1 0	1 1 1 1 1 1 0	0	0 1 1 0	0 0 1 1 1 1 1	6
0 1 1 1	1 1 1 1 1 1 0	0	0 1 1 1	1 1 1 0 0 0 0	7
1 0 0 0	1 1 1 1 1 1 0	0	1 0 0 0	1 1 1 1 1 1 1	8
1 0 0 1	1 1 1 1 1 1 0	0	1 0 0 1	1 1 1 0 0 1 1	9
1 0 1 0	0 1 1 0 0 0 0	1	1 0 1 0	1 1 1 1 1 1 0	0
1 0 1 1	0 1 1 0 0 0 0	1	1 0 1 1	0 1 1 0 0 0 0	1

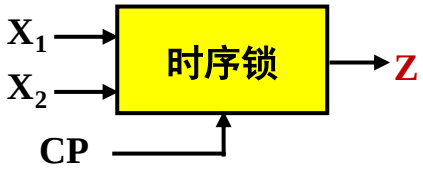


十位								个位							
$y_4y_3y_2y_1$	a	b	c	d	e	f	g	$y_4y_3y_2y_1$	a	b	c	d	e	f	g
0 0 0 0	1	1	1	1	1	1	0	0 0 0 0	1	1	1	1	1	1	0
0 0 0 1	1	1	1	1	1	1	0	0 0 0 1	0	1	1	0	0	0	0
0 0 1 0	1	1	1	1	1	1	0	0 0 1 0	1	1	0	1	1	0	1
0 0 1 1	1	1	1	1	1	1	0	0 0 1 1	1	1	1	1	0	0	1
0 1 0 0	1	1	1	1	1	1	0	0 1 0 0	0	1	1	0	0	1	1
0 1 0 1	1	1	1	1	1	1	0	0 1 0 1	1	0	1	1	0	1	1
0 1 1 0	1	1	1	1	1	1	0	0 1 1 0	0	0	1	1	1	1	1
0 1 1 1	1	1	1	1	1	1	0	0 1 1 1	1	1	1	0	0	0	0
1 0 0 0	1	1	1	1	1	1	0	1 0 0 0	1	1	1	1	1	1	1
1 0 0 1	1	1	1	1	1	1	0	1 0 0 1	1	1	1	0	0	1	1
1 0 1 0	0	1	1	0	0	0	0	1 0 1 0	1	1	1	1	1	1	0
1 0 1 1	0	1	1	0	0	0	0	1 0 1 1	0	1	1	0	0	0	0

Example

PLA及其应用

例6：利用PLA设计时序锁（假设PLA中是 JK触发器）



- 输入: X_1X_2，输出: Z
- 该锁内部有四个状态R、B、C、E
- 依次输入00、01、11，时序锁从状态 R→B→C，并开锁（Z=1）
- 不是上述序列，进入状态 E（error）
- 任何时候只要输入00，都将返回状态 R

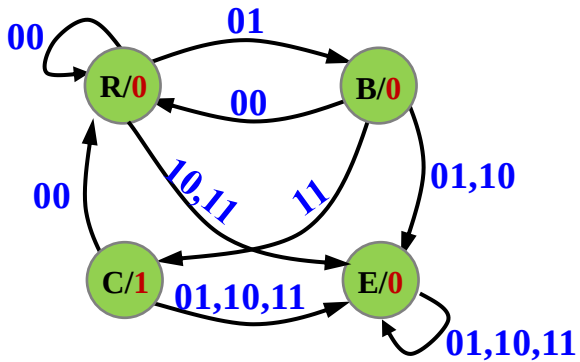
① 状态设定

R—初始状态，输入00

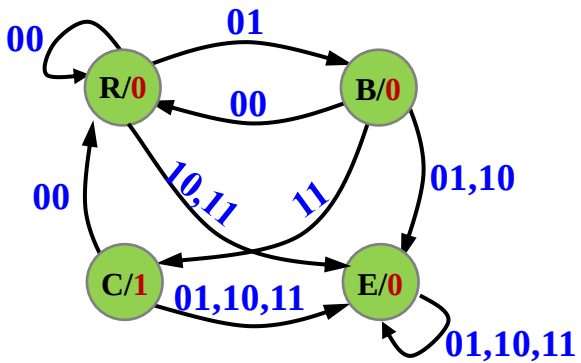
B—输入00后，再输入01

C—输入00、01后，再输入11

E—错误状态



PLA及其应用



现态 S_n	次态 S_{n+1}				输出 Z
	$X_1X_2=00$	$X_1X_2=01$	$X_1X_2=11$	$X_1X_2=10$	
R	R	B	E	E	0
B	R	E	C	E	0
C	R	E	E	E	1
E	R	E	E	E	0

2. 状态化简

3. 状态分配

R: 00, B : 01

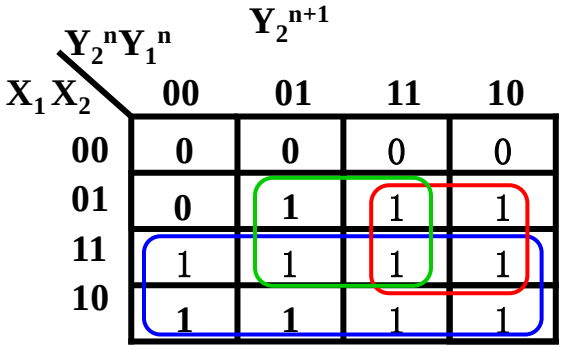
E : 10, C: 11

需要2个JK触发器

	0	1
0	R	B
1	E	C

输入		现态		次态		输入				输出
X_1	X_2	Y_2^n	Y_1^n	Y_2^{n+1}	Y_1^{n+1}	J_2	K_2	J_1	K_1	Z
0	0	0	0	0	0	0	X	0	X	0
0	0	0	1	0	0	0	X	X	1	0
0	0	1	0	0	0	X	1	0	X	0
0	0	1	1	0	0	X	1	X	1	1
0	1	0	0	0	1	0	X	1	X	0
0	1	0	1	1	0	1	X	X	1	0
0	1	1	0	1	0	X	0	0	X	0
0	1	1	1	1	0	X	0	X	1	1
1	0	0	0	1	0	1	X	0	X	0
1	0	0	1	1	0	1	X	X	1	0
1	0	1	0	1	0	X	0	0	X	0
1	0	1	1	1	0	X	0	X	1	1
1	1	0	0	1	0	1	X	0	X	0
1	1	0	1	1	1	1	X	X	0	0
1	1	1	0	1	0	X	0	0	X	0
1	1	1	1	1	0	X	0	X	1	1

输入		现态		次态		输入				输出
X_1	X_2	Y_2^n	Y_1^n	Y_2^{n+1}	Y_1^{n+1}	J_2	K_2	J_1	K_1	Z
0	0	0	0	0	0	0	X	0	X	0
0	0	0	1	0	0	0	X	X	1	0
0	0	1	0	0	0	X	1	0	X	0
0	0	1	1	0	0	X	1	X	1	1
0	1	0	0	0	1	0	X	1	X	0
0	1	0	1	1	0	1	X	X	1	0
0	1	1	0	1	0	X	0	0	X	0
0	1	1	1	1	0	X	0	X	1	1
1	0	0	0	1	0	1	X	0	X	0
1	0	0	1	1	0	1	X	X	1	0
1	0	1	0	1	0	X	0	0	X	0
1	0	1	1	1	0	X	0	X	1	1
1	1	0	0	1	0	1	X	0	X	0
1	1	0	1	1	1	1	X	X	0	0
1	1	1	0	1	0	X	0	0	X	0
1	1	1	1	1	0	X	0	X	1	1

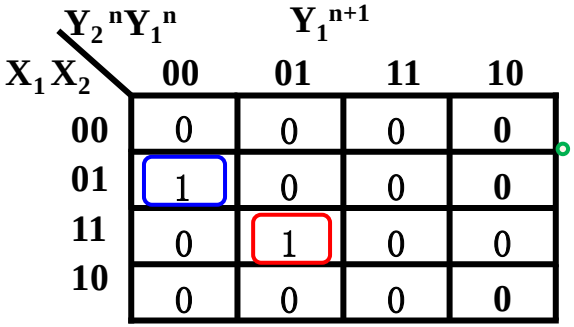


$$\begin{cases} J_2 = X_2Y_1^n + X_1 \\ K_2 = \overline{X_1 + X_2} = \overline{X}_1\overline{X}_2 \end{cases}$$

$$Y_2^{n+1} = X_2Y_1^n + X_1 + X_2Y_2^n$$

$$= (Y_1^n + \overline{Y}_1^n)(X_2Y_1^n + X_1) + X_2Y_1^n$$

$$= (X_2Y_1^n + X_1)\overline{Y}^n_1 + (X_1 + X_2)Y_1^n$$



一张卡诺图确定两个输入函数

$$Y_1^{n+1} = \overline{X}_1X_2\overline{Y}_2^n\overline{Y}_1^n + X_1X_2\overline{Y}_2^nY_1^n$$

$$\begin{cases} J_1 = \overline{X}_1X_2\overline{Y}_2^n \\ K_1 = \overline{X_1X_2\overline{Y}_2^n} \end{cases}$$

$$= \overline{X}_2 + \overline{X}_1 + Y_2^n$$

或者：

J_2

X_1X_2 \ $Y_2^nY_1^n$	00	01	11	10
00	0	0	X	X
01	0	1	X	X
11	1	1	X	X
10	1	1	X	X

K_2

X_1X_2 \ $Y_2^nY_1^n$	00	01	11	10
00	X	X	1	1
01	X	X	0	0
11	X	X	0	0
10	X	X	0	0

$$\begin{cases} J_2 = X_2Y_1^n + X_1 \\ K_2 = \overline{X_1 + X_2} = \overline{X}_1\overline{X}_2 \end{cases}$$

J_1

X_1X_2 \ $Y_2^nY_1^n$	00	01	11	10
00	0	X	X	0
01	1	X	X	0
11	0	X	X	0
10	0	X	X	0

K_1

X_1X_2 \ $Y_2^nY_1^n$	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	0	1	X

$$\begin{cases} J_1 = \overline{X}_1X_2\overline{Y}_2^n \\ K_1 = \overline{X}_2 + \overline{X}_1 + Y_2^n \end{cases}$$

X_1X_2 \ $Y_2^nY_1^n$	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	1	0
10	0	0	1	0

Y_2^{n+1}

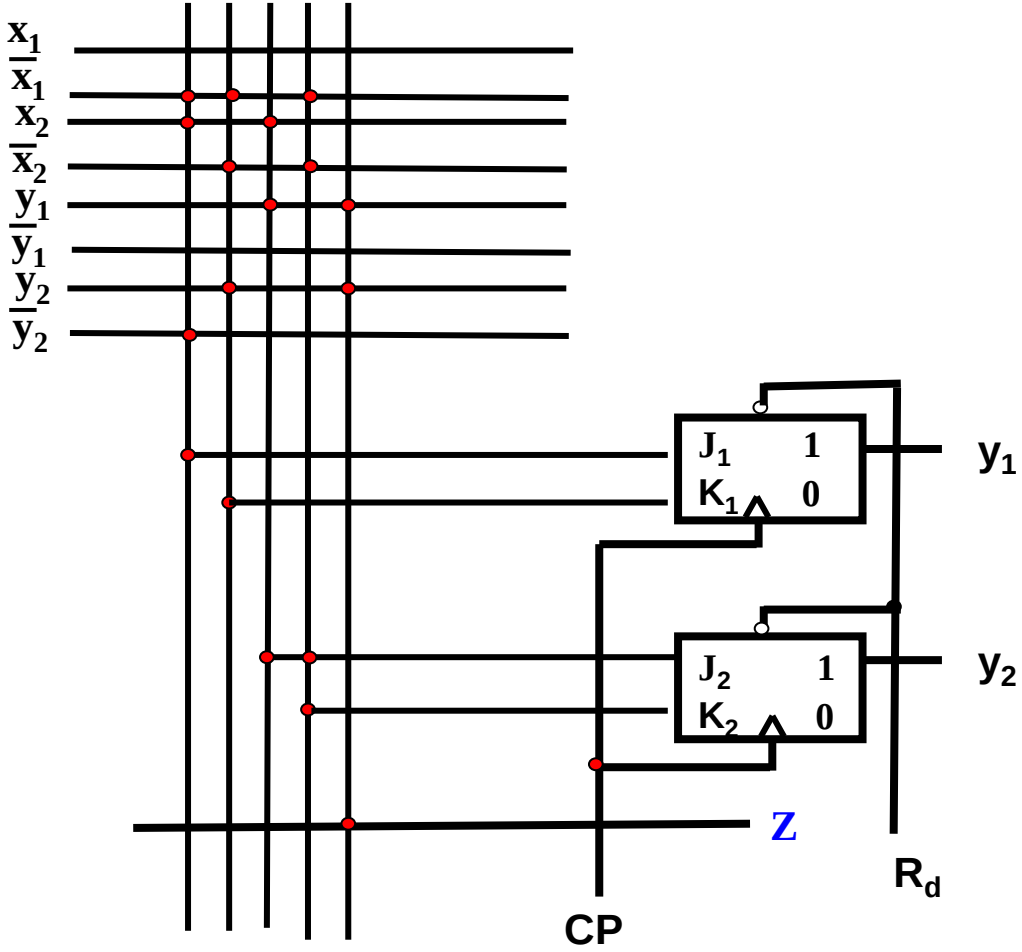
$$Z = Y_2Y_1$$

$$J_2 = X_2Y_1^n + X_1$$

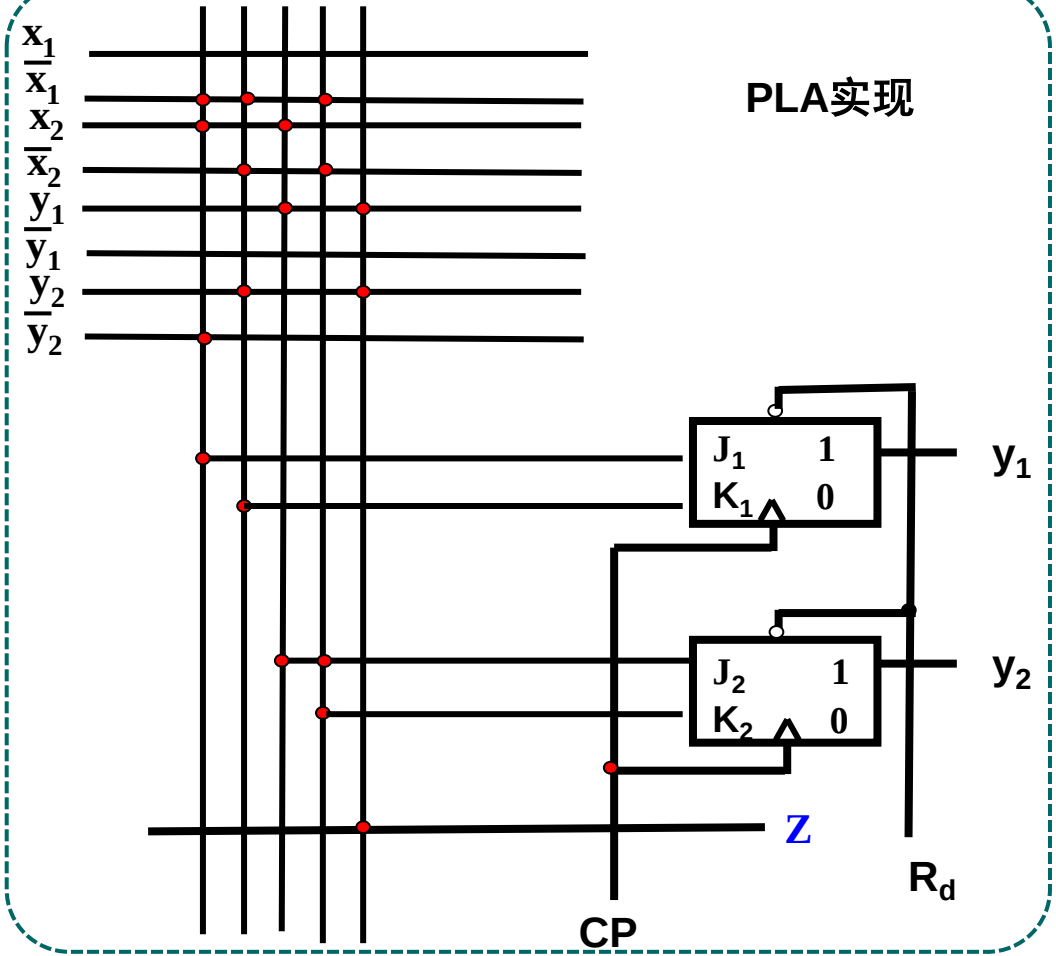
$$K_2 = \overline{X_1 + X_2} = \overline{X}_1\overline{X}_2$$

$$J_1 = \overline{X}_1X_2\overline{Y}_2^n$$

$$K_1 = \overline{X}_2 + \overline{X}_1 + Y_2^n$$



PLA实现



中规模芯片实现