arm Education

Embedded Systems Essentials with Arm: Getting Started

Module 6

KV2 (6): Timer operation modes

A typical standard timer may have three operation modes: compare, capture and pulse width modulation.

The main application of the compare-mode is to create a customized clock, as shown by this diagram. The compare register is preloaded with a desired value. The clock source is then provided as an input to the prescaler, which scales the clock frequency to a desired level. The timer register is then incremented or decremented automatically at a certain frequency, which is dictated by the prescaler. The value in the timer register is then compared with the value in the compare register. If the preset value in the compare register is equal to the value in the timer register, the comparator creates an interrupt and the timer is reset.

The main application for capture mode timers is the measurement of time intervals, as shown in this example. As in compare mode, the timer register is regularly incremented or decremented by the system clock. However, the capture register can be triggered by an external event source. The event source generates a sequence of pulses. There is the option for the prescaler to divide the frequency of such events.

Once the event occurs, the capture register takes a snapshot of the value in the timer register at that moment and submits an event.

This can be set up to generate an interrupt which notifies the processor to perform an action, such as reading the timer value from the capture register. The next event from the prescaler may result in a new reading. Its difference can be calculated into the time span between the two events.

A pulse width modulation uses the width of a pulse to modulate an amplitude and is typically used when a device cannot be controlled by amplitude, for example in the case of LEDs. It is mainly used to control the power supplied to devices. The amplitude is represented by on-off intervals or duty cycles, which describes the proportion of the “1” state in one pulse period. The cycle energy as a percentage of the maximum energy is given by the on time, represented by “t on”, divided by the period time, given by “t cycle”. This is illustrated in the diagram, as the “on time” proceeds from 25% to 50% to 75%, the amplitude increases and vice versa.

The PWM-mode is similar to the compare mode except that, in this instance, the timer is not automatically reset after reaching the compare value, but instead counts to the end or maximum value of the timer before it resets. For example, here, to generate a 50% power output the timer register is set to reset when it reaches 100 and the compare register is set to 50. This means that two interrupts are generated: one compare interrupt and one timer-overflow-interrupt. These two interrupts can be used to switch the PWM and its duty cycle on and off.