

## **SECOND ASSIGNMENT**

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### **ORGANIZATION AND ARCHITECTURE COMPUTER**



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**5.1 What are the key properties of semiconductor memory?**

Answer :

- A. It has two (semi)stable states which can be used to represent binary 1 and 0
- B. It supports read/write operations

**5.2 What are two interpretations of the term random-access memory?**

Answer :

- A. DRAM
- B. SRAM

**5.3 What is the difference between DRAM and SRAM in terms of application?**

Answer :

- A. SRAM is used for cache memory
- B. DRAM is used for main memory

**5.4 What is the difference between DRAM and SRAM in terms of characteristics such as speed, size, and cost?**

Answer :

- A. Speed: SRAM is faster
- B. Size: SRAM takes more space, DRAM is denser
- C. Cost: SRAM is more expensive than DRAM

**5.5 Explain why one type of RAM is considered to be analog and the other digital?**

Answer :

- A. DRAM: analog device because it stores charge and uses a threshold to determine the binary
- B. value SRAM: digital because it uses flip-flop logic gates

**5.6 What are some applications for ROM?**

Answer :

- A. Microprogramming
- B. Library subroutines for frequently wanted functions
- C. System programs
- D. Function tables

**5.7 What are the differences among EPROM, EEPROM, and flash memory?**

Answer :

- A. EPROM :
  - read/written electrically
  - before writing, all cells must be erased by exposure to UV light
  - price: \$
- B. EEPROM :
  - can be written to any time, without erasing contents
  - price: \$\$\$
- C. Flash memory :
  - electrical erasing (in seconds), faster than EPROM
  - price: \$\$

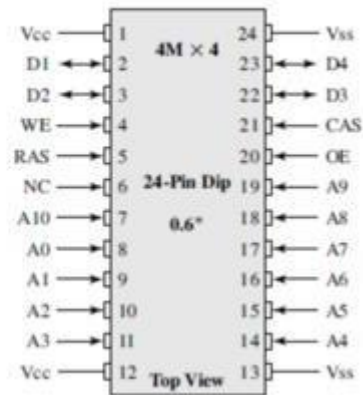
### 5.8 Explain the function of each pin in Figure 5.4b.

Answer :

Explain the function of each pin in Figure 5.4 (b).

- |     |         |   |
|-----|---------|---|
| 1.  | Vcc     | Power supply to chip.   |
| 2.  | D1 - D4 | Data pins - input/output, 4 lines.                                  |
| 4.  | WE      | Write enable - indicates write operation.                           |
| 5.  | RAS     | Row Address Select  |
| 6.  | NC      | No connect - to make even number of pins.                           |
| 7.  | A0-A10  | Address of word being accessed.<br>11 address pins reqd for 4M x 4. |
| 24. | Vss     | Ground pin.   |
| 21. | CAS     | Column Address Select.  |
| 20. | OE      | Output enable - indicates read operation.                           |

Fig 5.4 (b) 16 Mbit DRAM



### 5.9 What is a parity bit?

Answer :

A bit appended to an array of binary digits to make the sum of all the binary digits, including the parity bit, always odd (odd parity), or always even (even parity)

### 5.10 How is the syndrome for the Hamming code interpreted?

Answer :

Each bit of the syndrome is 0 or 1 according to if there is or is not a match in that bit position for the two inputs.

### 5.11 How does SDRAM differ from ordinary DRAM?

Answer :

- A. Synchronous, unlike traditional DRAM
- B. Synchronized with the system bus

### 5.12 What is DDR RAM?

Answer :

DDR RAM is double data-rate DRAM. The data transfer is synchronized to the rising and falling edge of the clock as opposed to just the rising edge. This doubles the data rate. DDR also utilizes a higher clock rate on the bus to further increase the transfer rate. A third advantage of DDR is that a buffering scheme is used. This buffering cycle essentially allows for the prefetch of two words. Every time a read or write operation is performed, it is done on two words of data and either inputs or outputs from the SDRAM on one clock cycle on both the rising and falling edges.

### 5.13 What is the difference between NAND and NOR flash memory?

Answer :

NAND reads and writes faster, uses less space, last longer, and cost less per bit

**5.14 List and briefly define three newer nonvolatile solid-state memory technologies.**

Answer :

- A. STT-RAM Spin-transfer torque magnetic random-access memory - The storage capability or programmability of MRAM arises from magnetic tunneling junction (MTJ), in which a thin tunneling dielectric is sandwiched between two ferromagnetic layers.
- B. PCRAM Phase-change random-access memory - The data storage capability is achieved from the resistance differences between an amorphous (high-resistance) and a crystalline (low-resistance) phase of the chalcogenide-based material.
- C. ReRAM Resistive random-access memory - Creates resistance rather than directly storing charge. An electric current is applied to a material, changing the resistance of that material. The resistance state can then be measured and a 1 or 0 is read as the result