MODUL 8

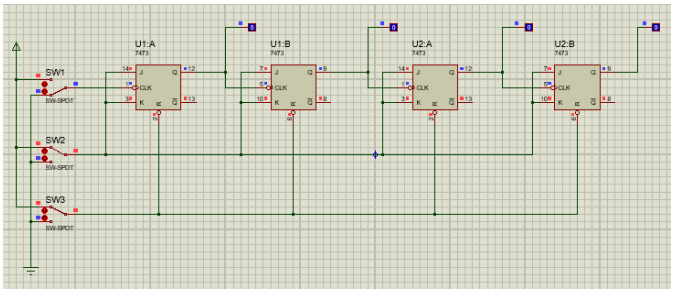
APLIKASI FLIP-FLOP

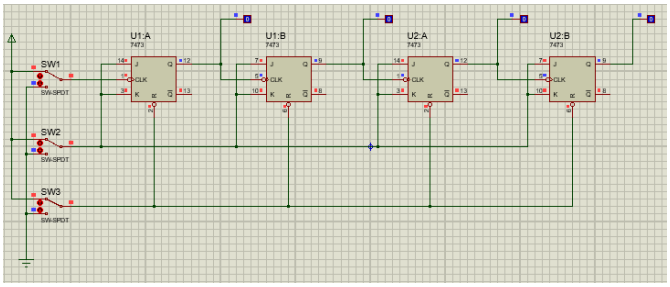
NAMA : RISKA PUTRI DAMAYANTI

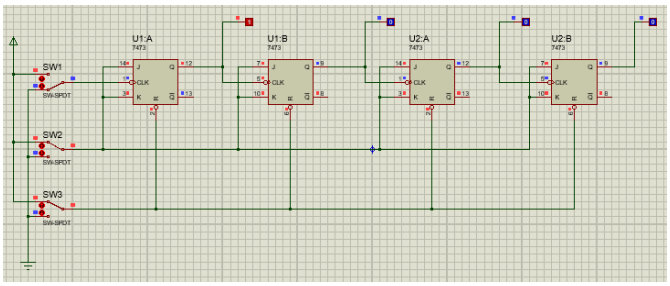
NIM : L200180209

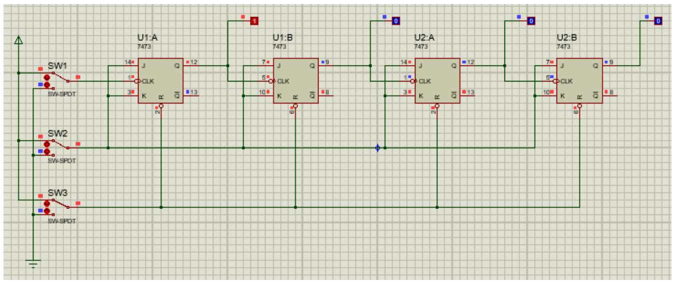
KELAS : G PRAKTIKUM

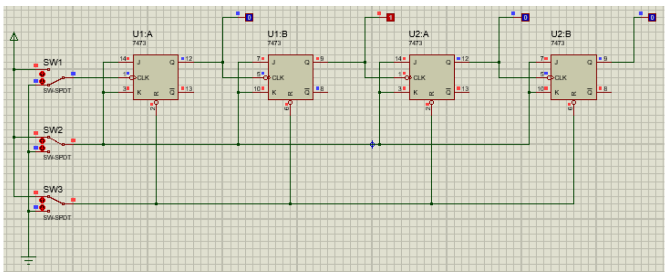
PERCOBAAN 1. MEMBUAT COUNTER JK-FF

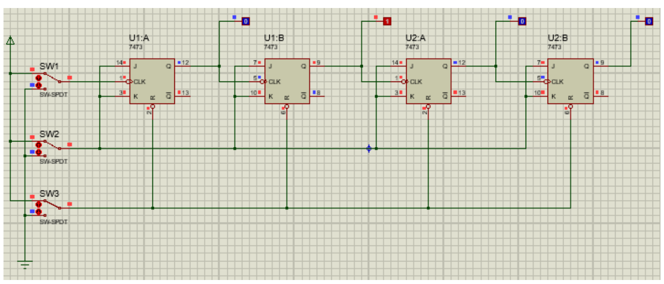


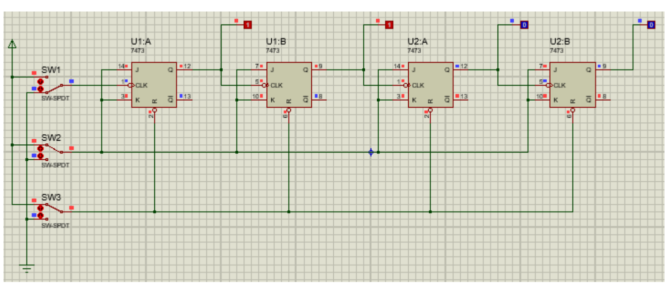


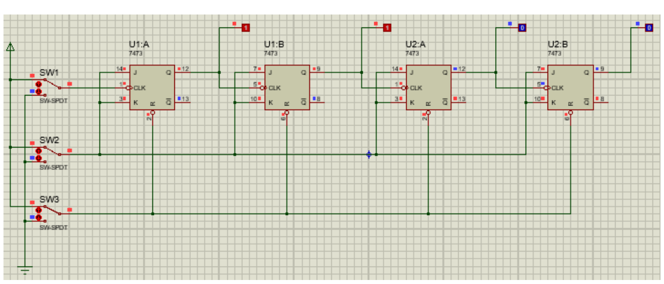


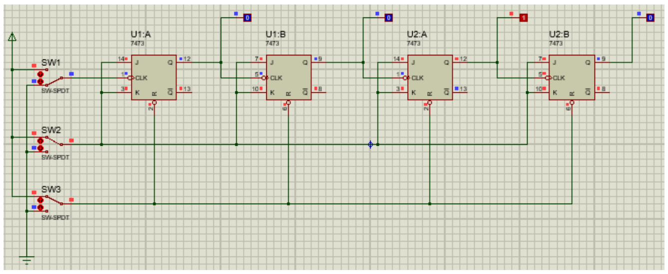

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

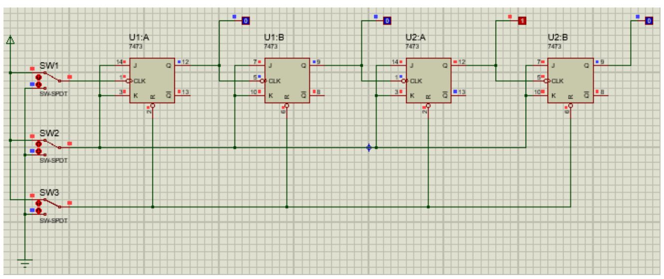

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

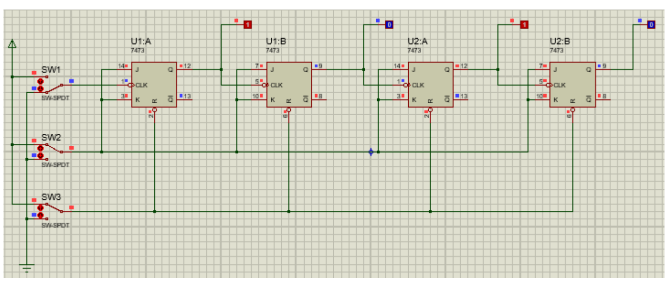

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

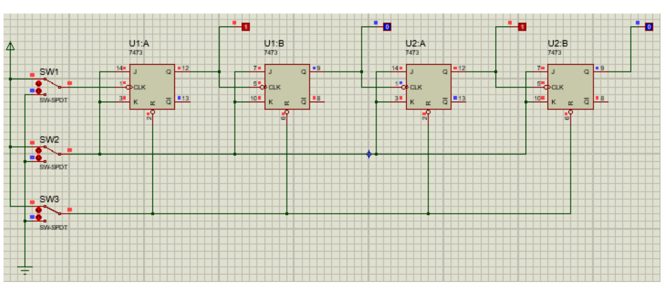

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

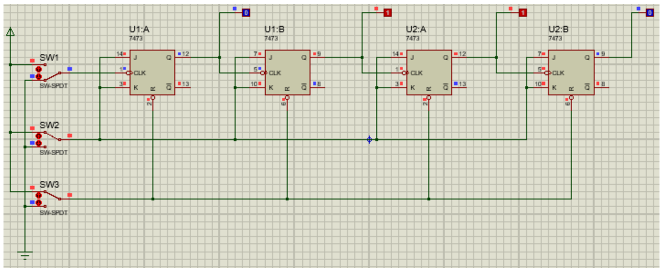

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

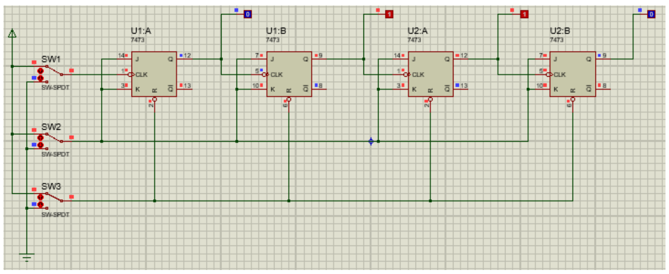

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

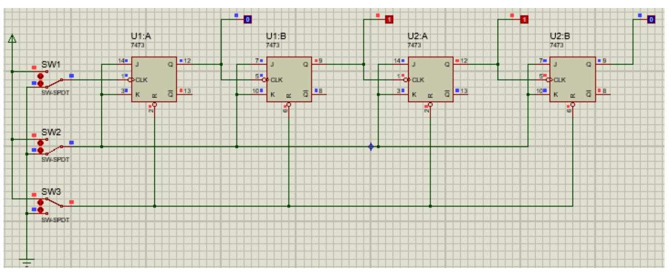

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

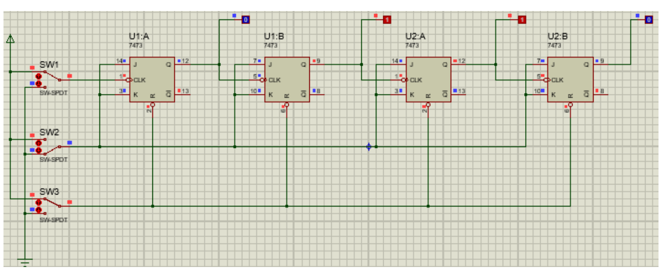

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

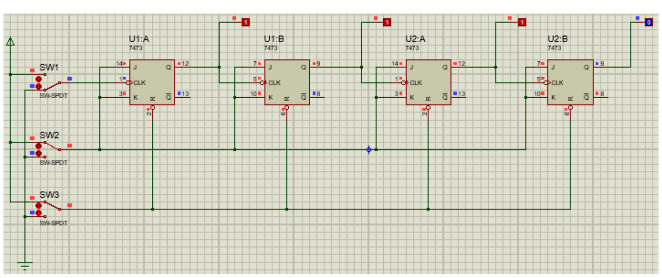

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

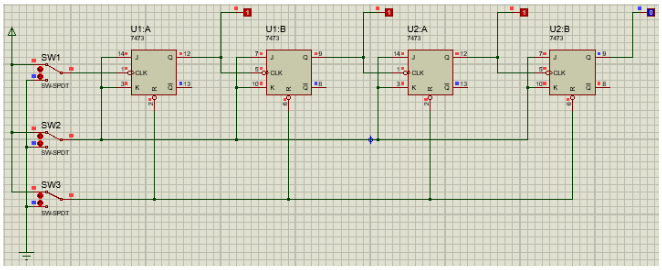

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

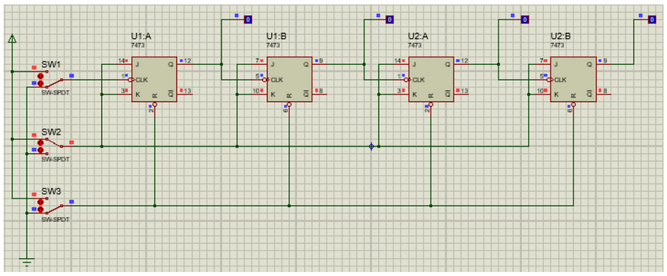

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT

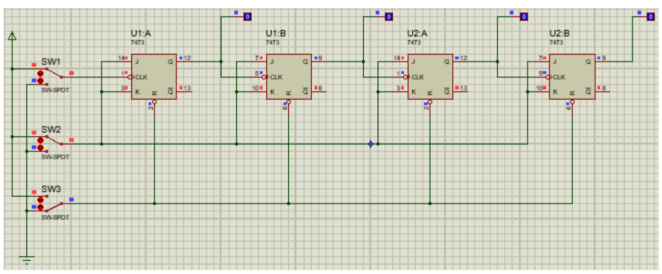

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT


U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT


U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT







	INPUT			OUTPUT			
	CLEAR	**JK**	**CLK**	**A**	**B**	**C**	**D**
1	1	1	0	0	0	0	0
2	1	1	1	0	0	0	0
3	1	1	0	0	0	0	1
4	1	1	1	0	0	0	1
5	1	1	0	0	0	1	0
6	1	1	1	0	0	1	0
7	1	1	0	0	0	1	1
8	1	1	1	0	0	1	1
9	1	1	0	0	1	0	0
10	1	1	1	0	1	0	0
11	1	1	0	0	1	0	1
12	1	1	1	0	1	0	1
13	1	1	0	0	1	1	0
14	1	1	1	0	1	1	0
15	1	0	0	0	1	1	0
16	1	0	1	0	1	1	0

17	1	1	0	0	1	1	1
18	1	1	1	0	1	1	1
19	0	1	0	0	0	0	0
20	0	1	1	0	0	0	0

1.) FUNGSI SWITCH CLK

Fungsinya adalah sebagai pengatur inputan/masukan

2.) FUNGSI SWITCH JK

Fungsinya adalah untuk mengendalikan masukan atau inputan

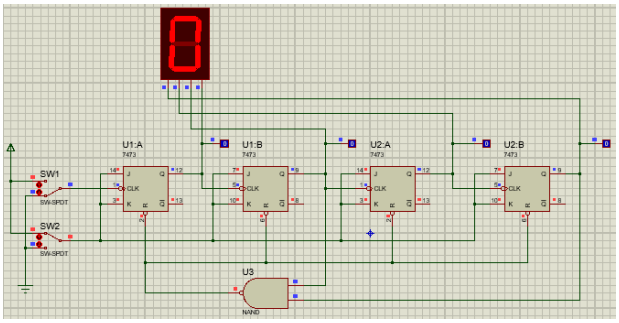
3.) FUNGSI SWITCH CLEAR

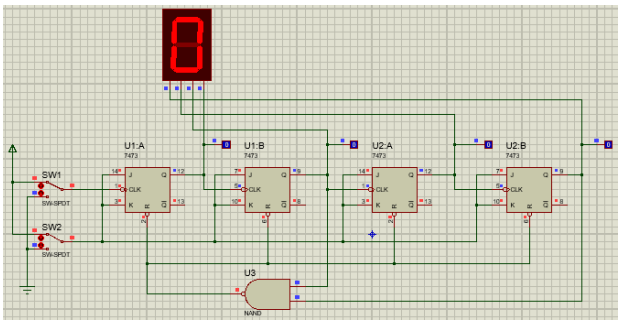
Fungsinya untuk mereset atau sebagai pereset

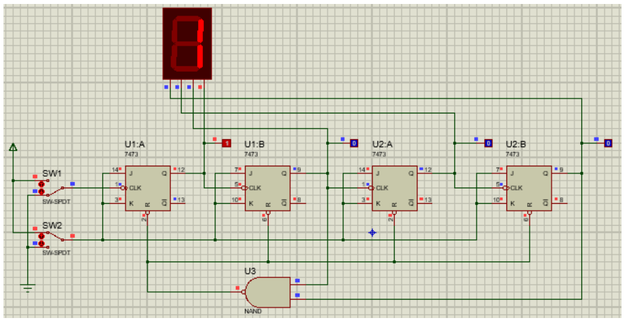
KESIMPULAN

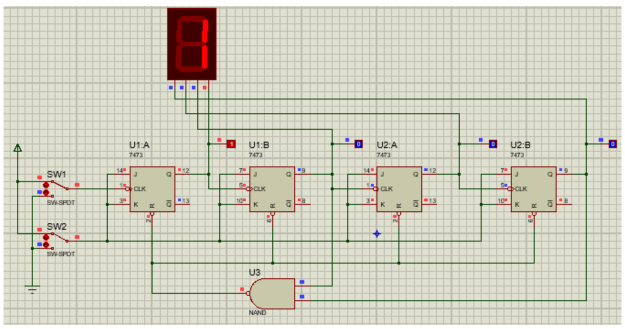
Rangkaian penghitung yang asinkron yang dimana hasilnya tergantung pada jumlah atau banyaknya clock.

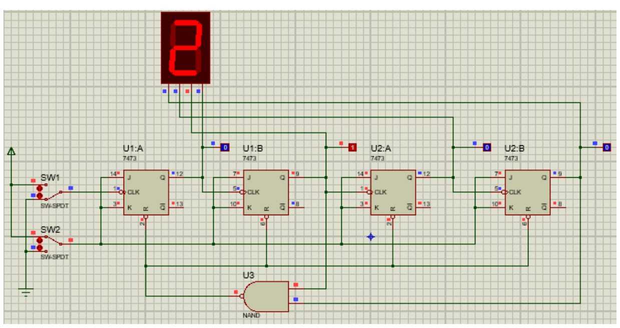
PERCOBAAN 2. COUNTER MOD 10

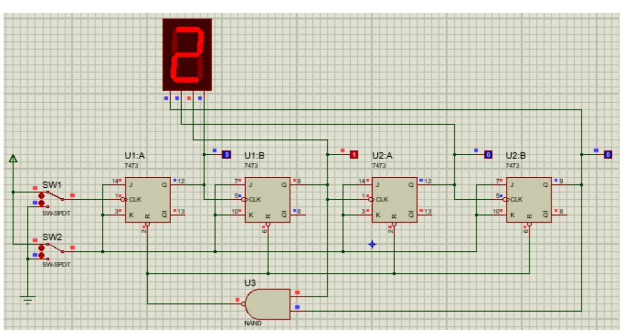


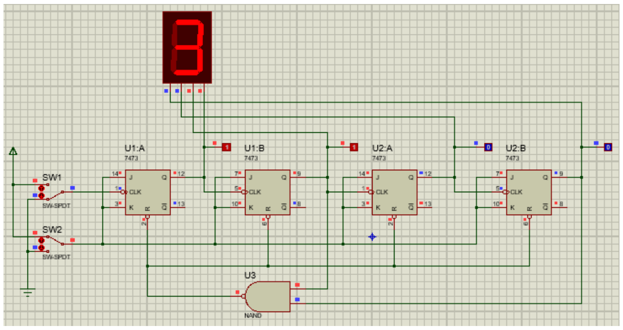


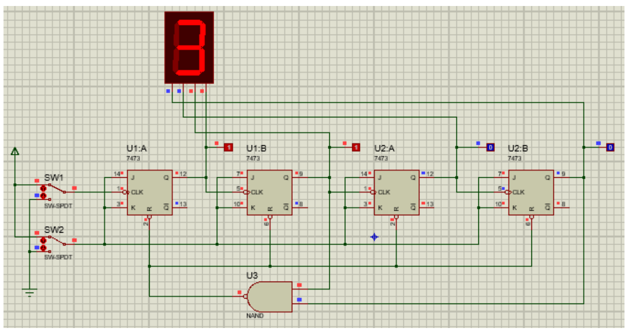

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND

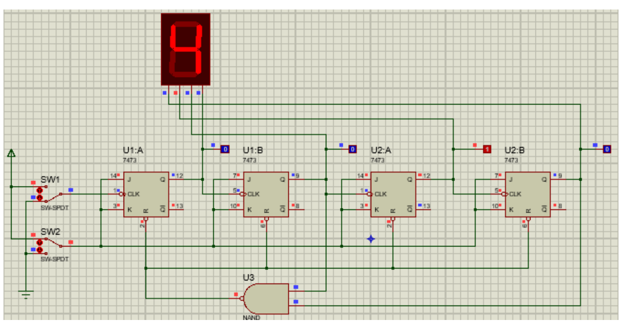

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND

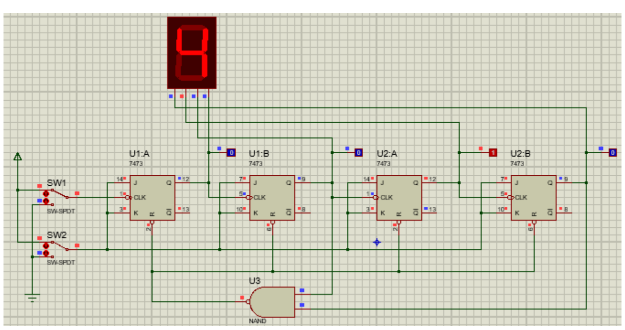

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND

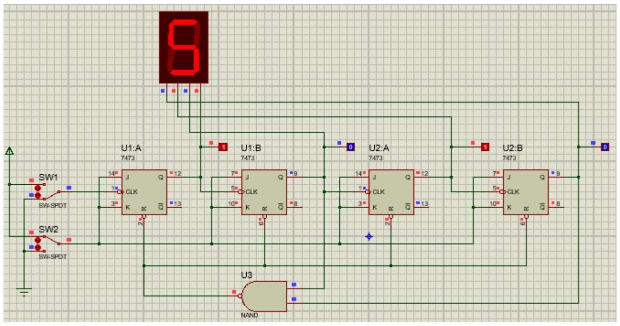

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND

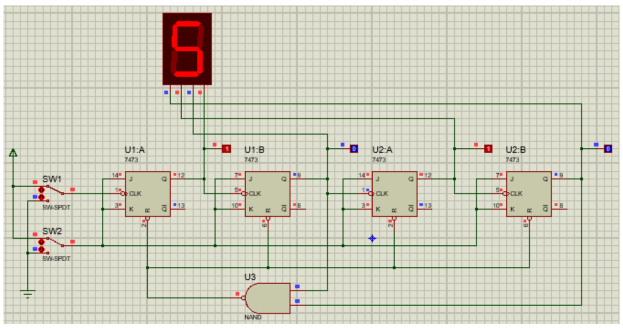

SW1
SW-SPDT
SW2
SW-SPDT
U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
U3
NAND

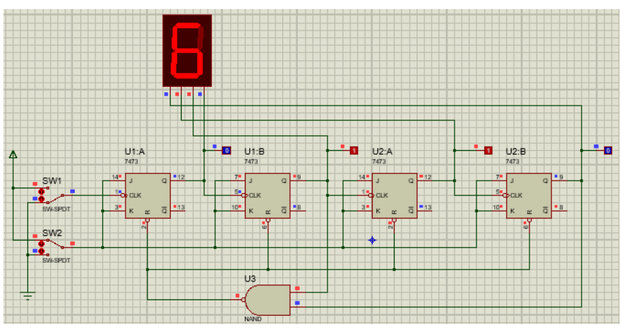

SW1
SW-SPDT
SW2
SW-SPDT
U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
U3
NAND

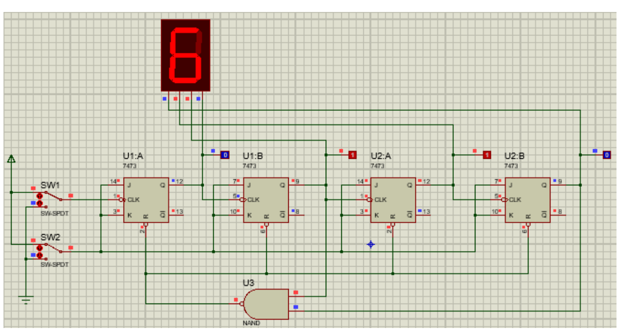

SW1
SW-SPDT
SW2
SW-SPDT
U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
U3
NAND

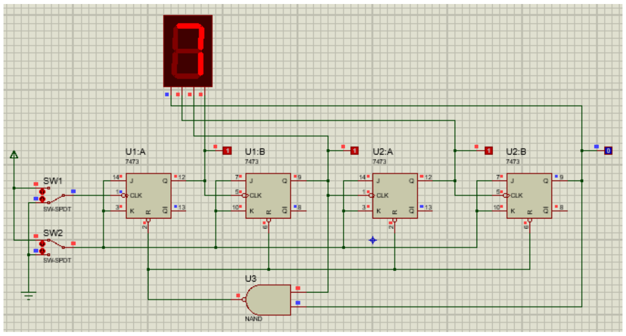

SW1
SW-SPDT
SW2
SW-SPDT
U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
U3
NAND

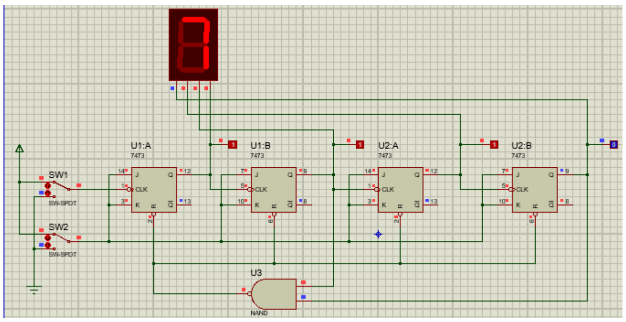

SW1
SW2
U1:A
U1:B
U2:A
U2:B
U3
NAND

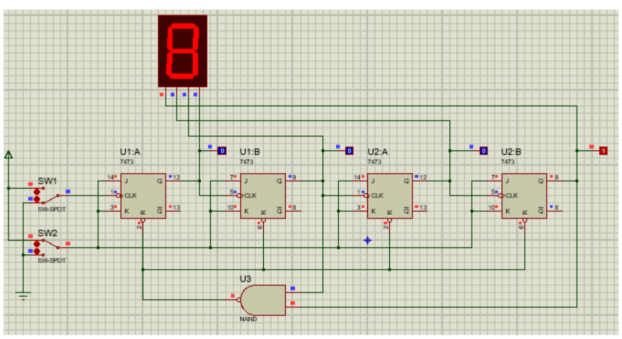

SW1
SW2
U1:A
U1:B
U2:A
U2:B
U3
NAND

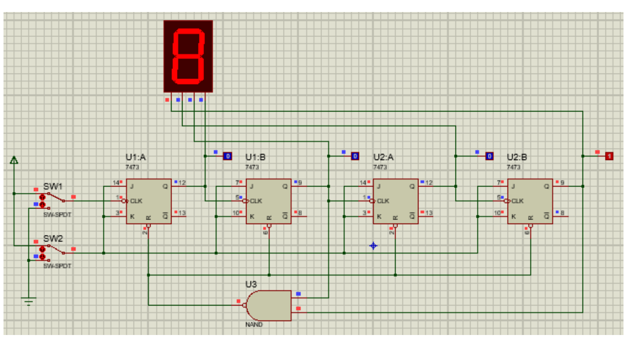

SW1
SW2
U1:A
U1:B
U2:A
U2:B
U3
NAND

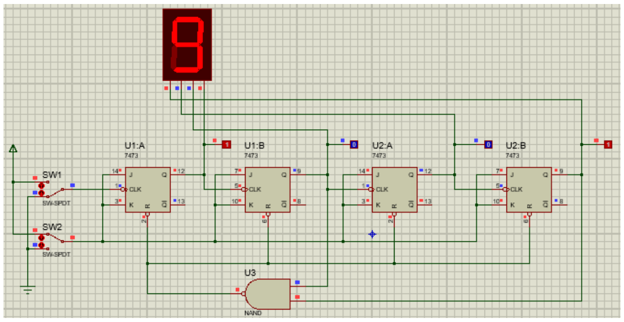

SW1
SW2
U1:A
U1:B
U2:A
U2:B
U3
NAND

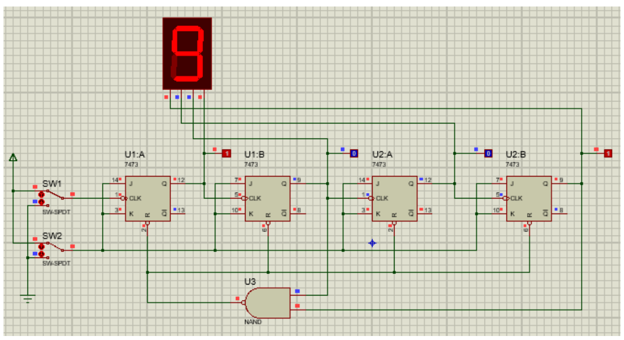

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND

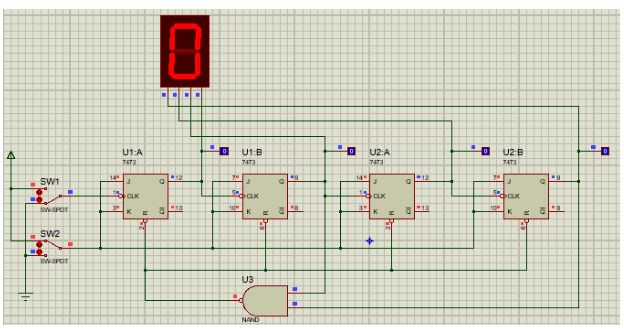

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND

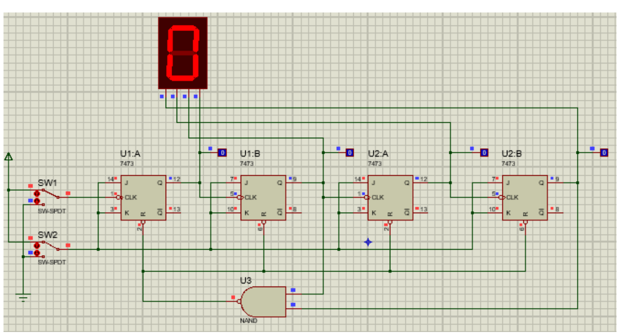

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND

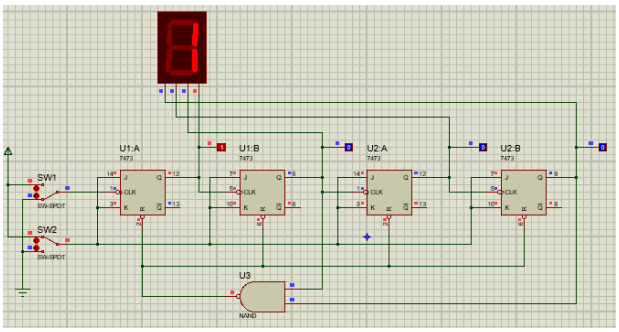

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND

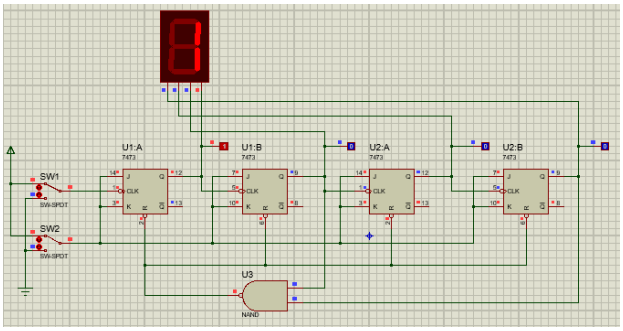

U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND


U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND


U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND


U1:A
7473
U1:B
7473
U2:A
7473
U2:B
7473
SW1
SW-SPDT
SW2
SW-SPDT
U3
NAND



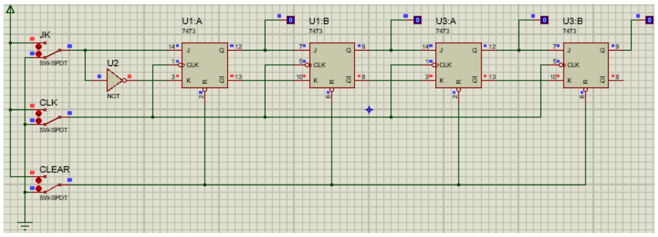


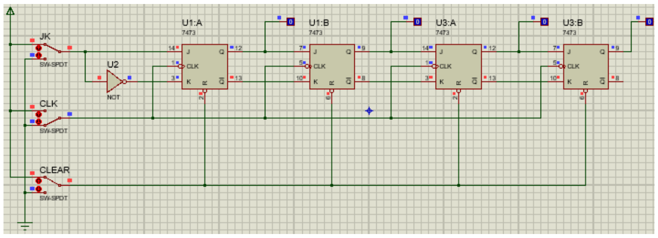
	INPUT		OUTPUT			
	JK	CLK	A	B	C	D
1	1	0	0	0	0	0
2	1	1	0	0	0	0
3	1	0	0	0	0	1
4	1	1	0	0	0	1
5	1	0	0	0	1	0
6	1	1	0	0	1	0
7	1	0	0	0	1	1
8	1	1	0	0	1	1
9	1	0	0	1	0	0
10	1	1	0	1	0	0
11	1	0	0	1	0	1
12	1	1	0	1	0	1
13	1	0	0	1	1	0
14	1	1	0	1	1	0
15	1	0	0	1	1	1
16	1	1	0	1	1	1
17	1	0	1	0	0	0
18	1	1	1	0	0	0
19	1	0	1	0	0	1
20	1	1	1	0	0	1
21	0	0	0	0	0	0
22	0	1	0	0	0	0
23	1	0	0	0	0	1
24	1	1	1	0	0	1

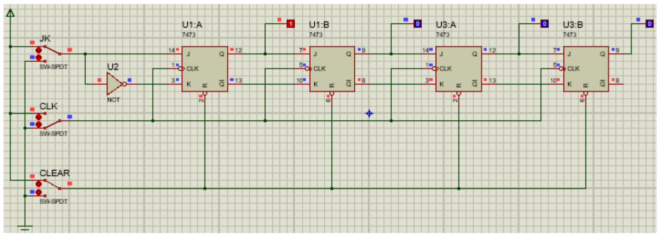
KESIMPULAN

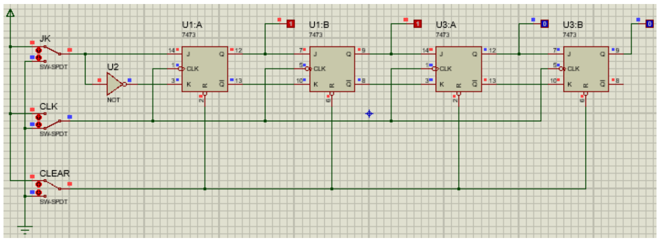
Jika JK bernilai 1 dan CLK bernilai 0 maka yang terjadi adalah nilainya akan berubah, dan jika JK bernilai 1 dan CLK bernilai 1 maka nilai akan tetap sama pada sebelumnya atau akan menyimpan nilai, dan jika JK bernilai 0 dan CLK bernilai 0 maupun 1 maka hasilnya akan bernilai 0.

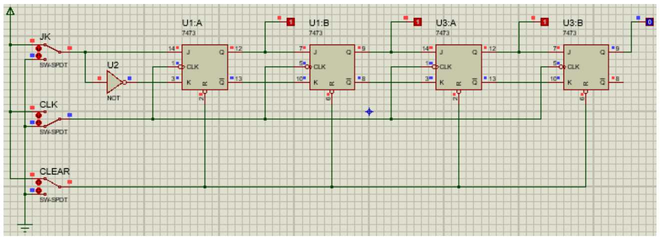
PERCOBAAN 3. MEMBUAT REGISTER JK-FF

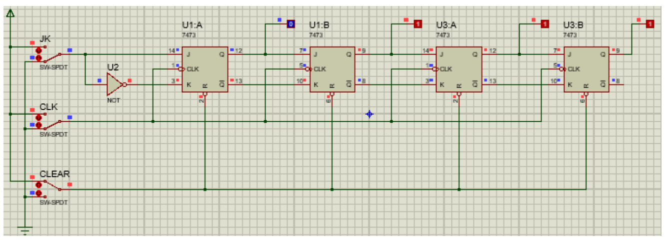


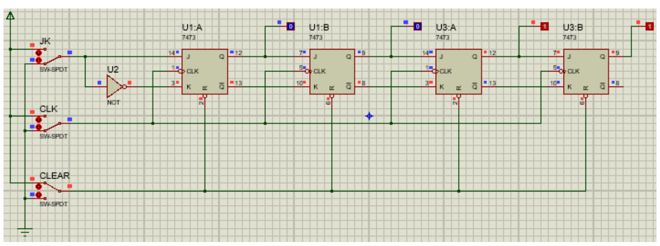


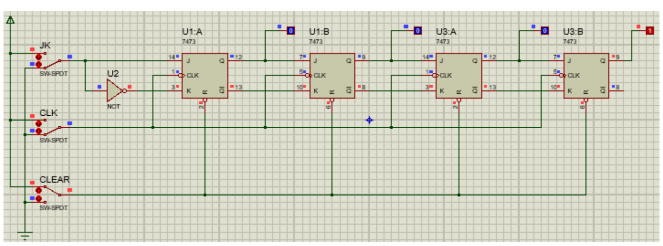


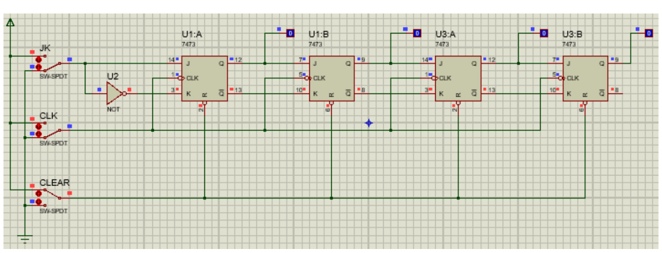


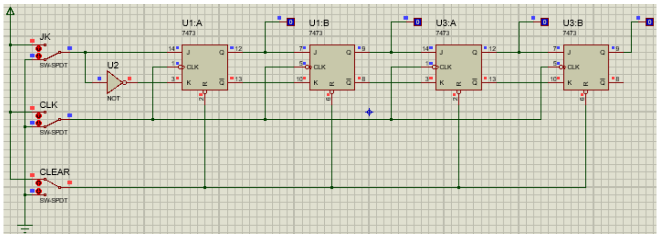

JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473

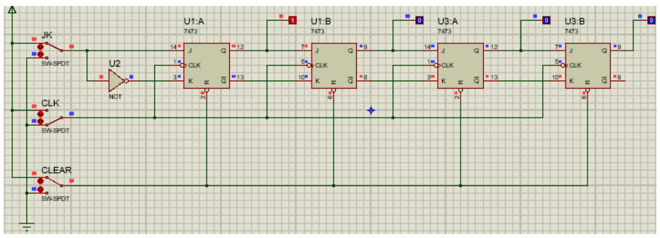

JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473

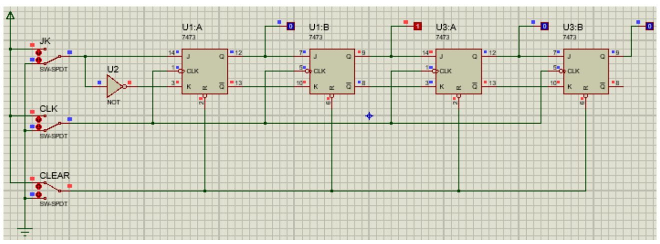

JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473

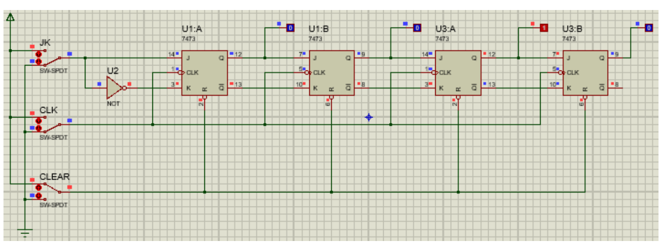

JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473

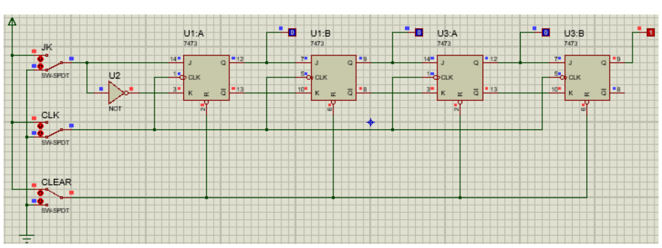

JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473

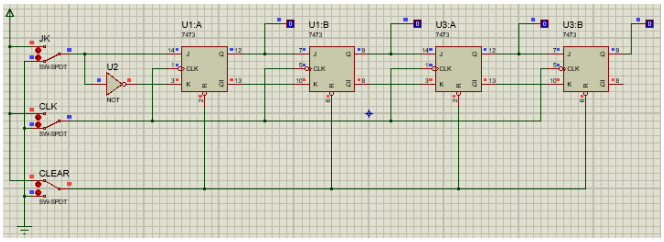

JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473
0
0
0
0


JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473
1
0
0
0


JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473
0
1
0
0


JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473
0
0
1
0


JK
SW-SPDT
CLK
SW-SPDT
CLEAR
SW-SPDT
U2
NOT
U1:A
7473
U1:B
7473
U3:A
7473
U3:B
7473
0
0
0
1



	CLR	JK	CLK	A	B	C	D
1	0	x	-	0	0	0	0
2	1	1	-	0	0	0	0
3	1	1	1	0	0	0	1
4	1	1	2	0	0	1	1
5	1	1	3	0	1	1	1
6	1	0	4	1	1	1	0
7	1	0	5	1	1	0	0
8	1	0	6	1	0	0	0
9	1	0	7	0	0	0	0
10	1	0	8	0	0	0	0
11	1	1	9	0	0	0	1
12	1	0	10	0	0	1	0
13	1	0	11	0	1	0	0
14	1	0	12	1	0	0	0
15	1	0	13	0	0	0	0

KESIMPULAN

Flip flop akan memulai menhitung saat CLK membuka gerbang, dan JK akan beroperasi sebagai masukan atau inputan dan mengatur keluaran atau output dari register.