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These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10–15) input conditions.

- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Typical power dissipation 140 mW
- Typical propagation delay 17 ns

Ordering Code:

Order Number	Package Number	Package Description
DM7442AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

www.fairchildsemi.com

13.11
31/05/2019

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Logic Diagram

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Logic Diagram

INPUT A (15) INPUT B (14) INPUT C (13) INPUT D (12)

OUTPUT 0 (1) OUTPUT 1 (2) OUTPUT 2 (3) OUTPUT 3 (4) OUTPUT 4 (5) OUTPUT 5 (6) OUTPUT 6 (7) OUTPUT 7 (8) OUTPUT 8 (9) OUTPUT 9 (10) OUTPUT 9 (11)

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DM7442A

Function Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = HIGH Level
L = LOW Level

Logic Diagram