LAB WORK

DIGITAL SYSTEM

SEMESTER GENAP

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PROGRAM STUDI INFORMATIKA

FAKULTAS KOMUNIKASI DAN INFORMATIKA

MUHAMMADIYAH UNIVERSITY OF SURAKARTA

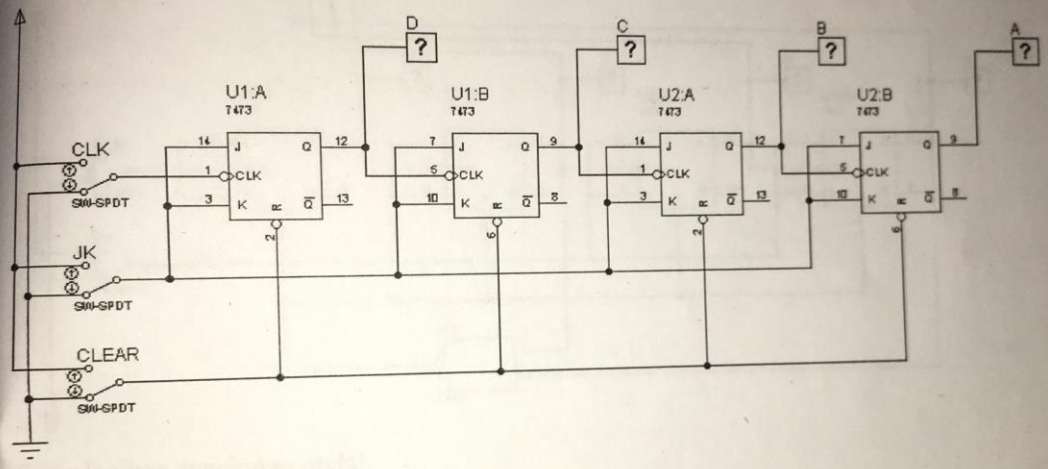
0			
0	1	1	X
1	0	X	1
1	1	X	0

0	0	0
0	1	1
1	0	1
1	1	0

EGIATAN PRAKTIKUM

Percobaan 1. Membuat Counter JK-FF

Buat kombinasi flip-flop JK seperti pada gambar!



2. Simulasikan rangkaian anda!

Klik pada switch berdasarkan pada tabel dan isi kolom kosong pada tabel!

	INPUT			OUTPUT			
	CLEAR	JK	CLK	A	B	C	D
1	1	1	0	0	0	0	0
2	1	1	1	0	0	0	0
3	1	1	0	0	0	0	1
4	1	1	1	0	0	0	1
5	1	1	0	0	0	1	0
6	1	1	1	0	0	1	0
7	1	1	0	0	0	1	1
8	1	1	1	0	0	1	1
9	1	1	0	0	1	0	0
10	1	1	1	0	1	0	0
11	1	1	0	0	1	0	1
12	1	1	1	0	1	0	1
13	1	1	0	0	1	1	0
14	1	1	1	0	1	1	0
15	1	0	0	0	1	1	0
16	1	0	1	0	1	1	0
17	1	1	0	0	1	1	1
18	1	1	1	0	1	1	1
19	0	1	0	0	0	0	0
20	0	1	1	0	0	0	0

3. Apa fungsi dari :

a. Switch CLK : sebagai reset 0 jadi berubah kalau 1 tetap sama

b. Switch JK : sebagai set

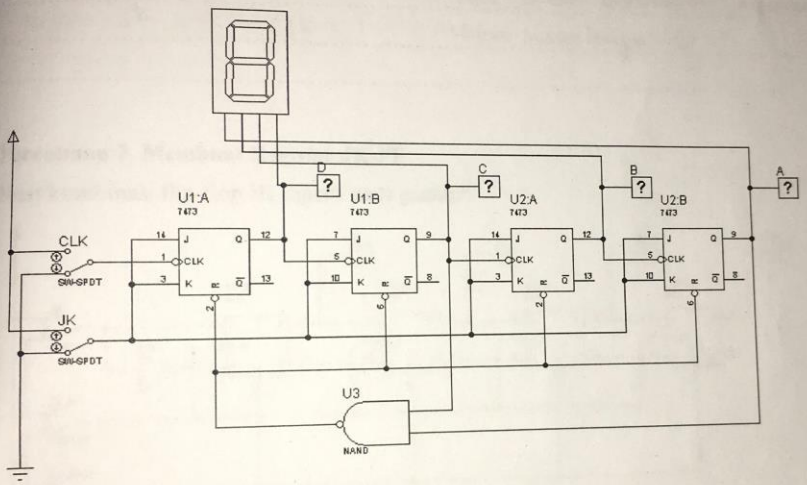
c. Switch CLEAR : sebagai reset

4. Kesimpulan:

rangkaian counter asinkron modul 16. digunakan untuk menyalurkan data Qnot

Percobaan2. Counter Mod 10

1. Buat kombinasi flip-flop JK seperti pada gambar!



2. Simulasikan rangkaian anda!

Klik pada switch berdasarkan pada tabel dan isi kolom kosong pada tabel!

	INPUT		OUTPUT			
	JK	CLK	A	B	C	D
1	1	0	0	0	0	0
2	1	1	0	0	0	0
3	1	0	0	0	0	1
4	1	1	0	0	0	1
5	1	0	0	0	1	0
6	1	1	0	0	1	0
7	1	0	0	0	1	1
8	1	1	0	0	1	1
9	1	0	0	1	0	0
10	1	1	0	1	0	0
11	1	0	0	1	0	1
12	1	1	0	1	0	1

13	1	0	0	1	1	0
14	1	1	0	1	1	0
15	1	0	0	1	1	1
16	1	1	0	1	1	1
17	1	0	1	0	0	0
18	1	1	1	0	0	0
19	1	0	1	0	0	1
20	1	1	1	0	0	1
21	0	0	0	0	0	0
22	0	1	0	0	0	0
23	1	0	0	0	0	0
24	1	1	0	0	0	0

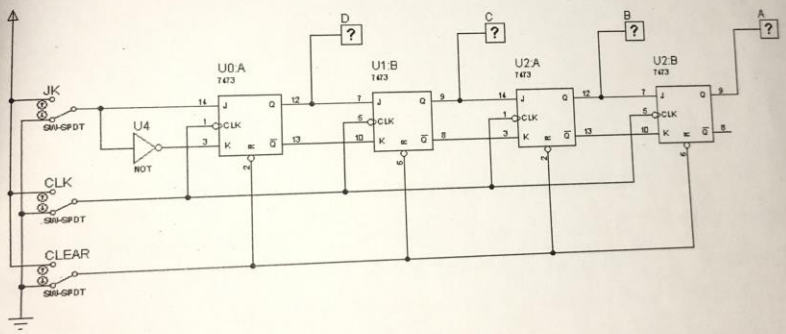
Klik pada switch berdasarkan pada tabel dan isi kolom kosong pada tabel!

3. Kesimpulan:

saat Jk = 1 Clk = 1 maka akan menyimpan variabel sblmnya
Jk = 1 Clk = 0 maka nilai berubah menjadi 1
Jk = 0 Clk = 1 maka hasilnya 0

Percobaan 3. Membuat Register JK-FF

1. Buat kombinasi flip-flop JK seperti pada gambar!



2. Simulasikan rangkaian anda!

Klik pada switch berdasarkan pada tabel dan isi kolom kosong pada tabel

	CLR	JK	CLK	A	B	C	D
1	0	x	-	0	0	0	0
2	1	1	-	0	0	0	0
3	1	1	1	0	0	0	1
4	1	1	2	0	0	1	1
5	1	1	3	0	1	1	1
6	1	0	4	1	1	1	0
7	1	0	5	1	1	0	0
8	1	0	6	1	0	0	0
9	1	0	7	0	0	0	0
10	1	0	8	0	0	0	0

11	1	1	9	0	0	0	1
12	1	0	10	0	0	1	0
13	1	0	11	0	1	0	0
14	1	0	12	1	0	0	0
15	1	0	13	0	0	0	0
16							

3. Kesimpulan : Clear sebagai reset
Selama JK kebalikannya 1 maka dapat mengulang terjadi pertukaran nilai jika 2x klik.
Clear 0 JK 0 jadi 0
Clear 1 JK 1 jadi 0

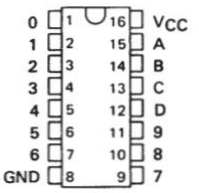
catatan :

1. Flip-flop adalah elemen dasar untuk membuat counter dan register, yang merupakan fundamental building block sangat penting pada sistem elektronik digital yang digunakan dalam sistem komputer.

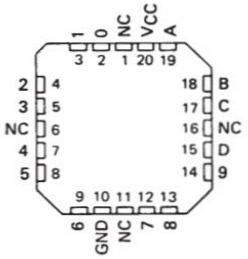
- **All Outputs Are High for Invalid Input Conditions**
- **Also for Application as**
  4-Line-to-16-Line Decoders
  3-Line-to-8-Line Decoders
- **Diode-Clamped Inputs**

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A	140 mW	17 ns
'LS42	35 mW	17 ns

SN5442A, SN54LS42 . . . J OR W PACKAGE
SN7442A . . . N PACKAGE
SN74LS42 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS42 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

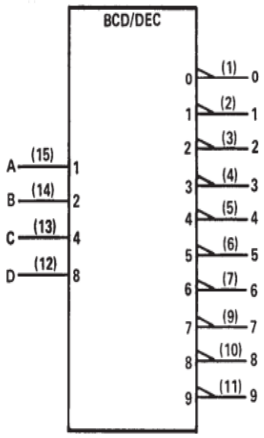
description

These monolithic BCD-to-decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A and 'LS42 feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

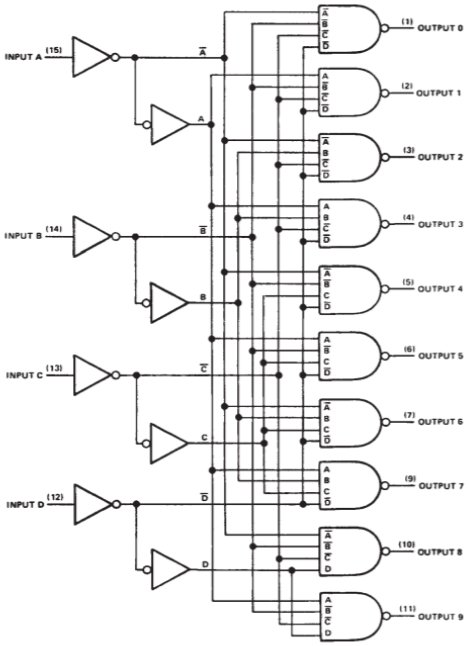
The SN5442A and SN54LS42 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7442A and SN74LS42 are characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

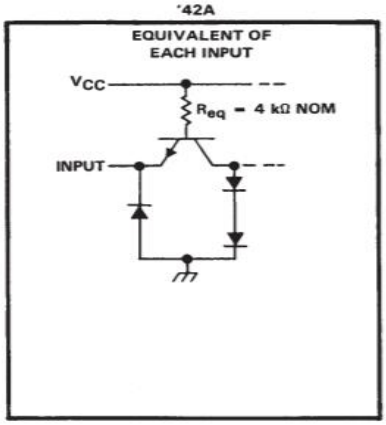
logic diagram (positive logic)



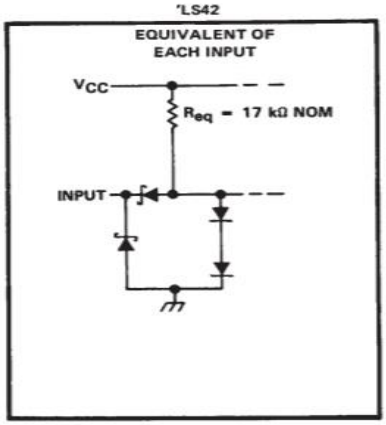
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

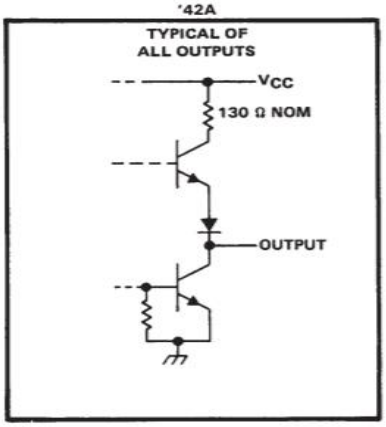
'42A



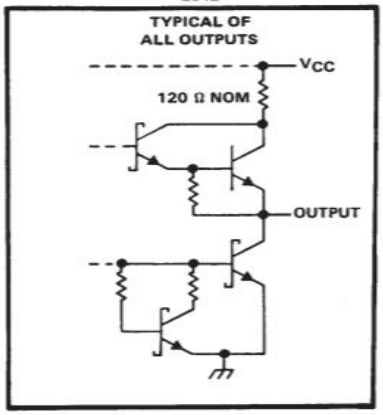
'LS42



'42A



'LS42



FUNCTION TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '42A . . . . . 5.5 V
'LS42 . . . . . 7 V
Operating free-air temperature range: SN5442A, SN54LS42 . . . . . −55°C to 125°C
SN7442A, SN74LS42 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.