DIGITAL SYSTEM

PRACTICUM REPORT 7 : FLIP FLOP DASAR

NIM : **L200183094**

NAME : **FARAH HUSNA PARAMADINA**

INFORMATION TECHNOLOGY

FACULTY OF COMMUNICATION AND INFORMATICS

MUHAMMADIYAH UNIVERSITY OF SURAKARTA

2019

NIM **: L200183094**

NAME **: FARAH HUSNA PARAMADINA**

CLASS **: X**

ASSISTANT **: SALSA SASMITA MUKTI**

DATE OF PRACTICUM **: Friday, May 3rd 2019**

- **ASSIGNMENT 1**

2)

	S(Set)	R(Reset)	Output	
			Q	Q’
1	0	1	0	1
2	0	0	0	1
3	1	0	1	0
4	0	0	1	0
5	1	1	0	0

3) a. So, the output is same, so, it can called as memory

b. Because the output between Q andQ’ is same

- **ASSIGNMENT 2**

2)

	S(Set)	R(Reset)	Output	
			Q	Q’
1	0	1	1	0
2	1	1	1	0
3	1	0	0	1
4	1	1	0	1
5	0	0	1	1

3) a. So, the output is same, so, it can called as memory

b. Because the output between Q andQ’ is same

c. the output will be same if change the input S=R=1, and the output will be change, if change from 1 to 0, 0 to 1.

- **ASSIGNMENT 3**

2)

	S(Set)	**R(Reset)**	**CLOCK**	**Output**	
				Q	**Q'**
1	0	0	0		
2	0	0	1		
3	0	1	0		
4	0	1	1	0	1
5	1	0	0	0	1
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	0

3) - logic race condition detected during transient analysis

- because, CLOCK=S=R+1 is given same. Output Q=Q'=0 and it is forbiden. So, if we change clock will bw error.

4) 00 → mengunci nilai sebelumnya

01 → mengganti nilai Q jadi Q'

10 → mengganti nilai Q jadi Q'

11 → kondisi terlarang yang menyebabkan eror.

- **ASSIGNMENT 4**

2)

	D	CLOCK	Output	
			Q	Q’
1	0	0		
2	0	1	0	1
3	1	0	0	1
4	1	1	1	0
5	0	0	1	0
6	0	1	0	1
7	1	0	0	1
8	1	1	1	0

3) If input D Change 0 → 1 or 1→ 0, output will be same with before. But if input D same with before the output will bw change.

4) Untuk mengatasi kondisi terlarang / forbidden state

- **ASSIGNMENT 5**

2)

	J	K	CLOCK	Output	
				Q	Q’
1	0	0	0	0	1
2	0	0	1	0	1
3	0	1	0	0	1
4	0	1	1	0	1
5	1	0	0	0	1
6	1	0	1	1	0
7	1	1	0	1	0
8	1	1	1	0	1

3) **a.** Nilai clock akan berubah,tapi tidak akan merubah nilai Q dan Q’

b. clock = 1, nilai Q dan Q’ akan berubah

clock = 0, akan menyimpan nilai Q dan Q’

4) Prinsip kerja hampir sama dengan Flipflop RS, tetapi kondisi terlarang (JK = 1 1, clock rise up) sudah hilang.